LT1806/LT1807

325MHz, Single/Dual, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps

FEATURES

- **Gain Bandwidth Product: 325MHz**
- **Slew Rate: 140V/µs**
- **Wide Supply Range: 2.5V to 12.6V**
- **Large Output Current: 85mA**
- **Low Distortion, 5MHz: –80dBc**
- **Low Voltage Noise: 3.5nV/√Hz**
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Input Offset Voltage (Rail-to-Rail): 550µV Max
- Common Mode Rejection: 106dB Typ
- Power Supply Rejection: 105dB Typ
- Unity-Gain Stable
- Power Down Pin (LT1806)
- Single in SO-8 and 6-Pin SOT-23 Packages
- Dual in SO-8 and 8-Pin MSOP Packages
- Operating Temperature Range: –40°C to 85°C

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Line Driver

DESCRIPTION

The LT®1806/LT1807 are single/dual low noise rail-to-rail input and output unity-gain stable op amps that feature a 325MHz gain-bandwidth product, a 140V/µs slew rate and a 85mA output current. They are optimized for low voltage, high performance signal conditioning systems.

The LT1806/LT1807 have a very low distortion of –80dBc at 5MHz, a low input referred noise voltage of 3.5nV/√Hz and a maximum offset voltage of 550µV that allows them to be used in high performance data acquisition systems.

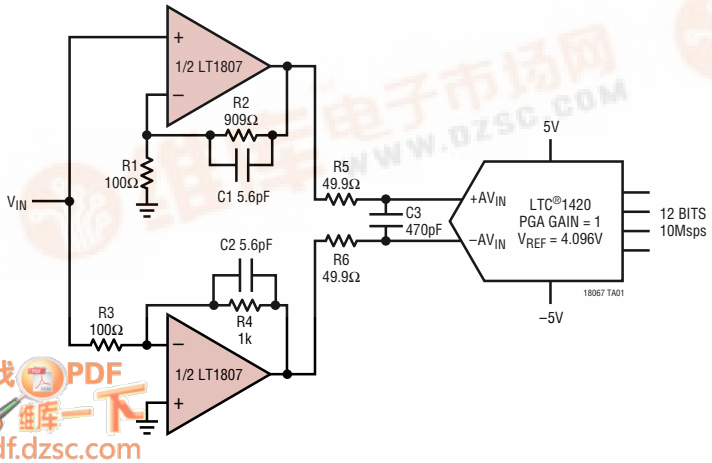
The LT1806/LT1807 have an input range that includes both supply rails and an output that swings within 20mV of either supply rail to maximize the signal dynamic range in low supply applications.

The LT1806/LT1807 maintain their performance for supplies from 2.5V to 12.6V and are specified at 3V, 5V and ±5V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

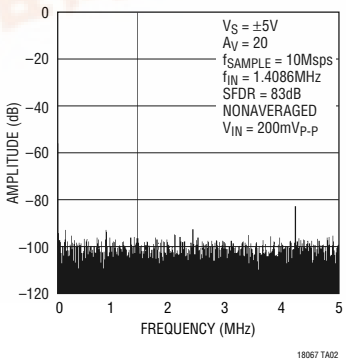
The LT1806 is available in an 8-pin SO package with the standard op amp pinout and a 6-pin SOT-23 package. The LT1807 features the standard dual op amp pinout and is available in 8-pin SO and MSOP packages.These devices can be used as plug-in replacements for many op amps to improve input/output range and performance.

TYPICAL APPLICATION

Gain of 20 Differential A/D Driver



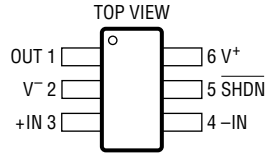
4096 Point FFT Response



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Voltage (Note 2) ..... $\pm V_S$
Input Current (Note 2) ..... ±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

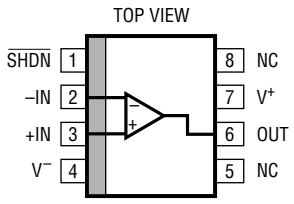
PACKAGE/ORDER INFORMATION



S6 PACKAGE
6-LEAD PLASTIC SOT-23

T_{JMAX} = 150°C, θ_{JA} = 160°C/W (Note 9)

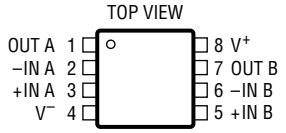
ORDER PART NUMBER
LT1806CS6 LT1806IS6
S6 PART MARKING
LTNK LTNL



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (Note 9)

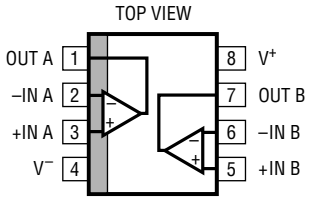
ORDER PART NUMBER
LT1806CS8 LT1806IS8
S8 PART MARKING
1806 1806I



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 135°C/W (Note 9)

ORDER PART NUMBER
LT1807CMS8 LT1807IMS8
MS8 PART MARKING
LTTT LTTV



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (Note 9)

ORDER PART NUMBER
LT1807CS8 LT1807IS8
S8 PART MARKING
1807 1807I

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V^+ V_{CM} = V^- V_{CM} = V^+ (LT1806 SOT-23) V_{CM} = V^- (LT1806 SOT-23)		100 100 100 100	550 550 700 700	µV µV µV µV
ΔV_{OS}	Input Offset Voltage Shift	V_{CM} = V^- to V^+ V_{CM} = V^- to V^+ (LT1806 SOT-23)		50 100	550 700	µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	V_{CM} = V^- to V^+		200	1000	µV
I_B	Input Bias Current	V_{CM} = V^+ V_{CM} = V^- + 0.2V	 –13	1 –5	4	µA µA
ΔI_B	Input Bias Current Shift	V_{CM} = V^- to V^+		6	17	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	V_{CM} = V^+ V_{CM} = V^- + 0.2V		0.03 0.05	1.2 3.0	µA µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$		0.03 0.05	0.6 1.5	µA µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.2V$ to V^+		0.08	2.1	µA
	Input Noise Voltage	0.1Hz to 10Hz		800		nV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		3.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		1.5		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to $V_S/2$ V_S = 5V, V_O = 1V to 4V, R_L = 100 to $V_S/2$ V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to $V_S/2$	75 9 60	220 22 150		V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+	79 74	100 95		dB dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+	73 68	100 95		dB dB
	Input Common Mode Range		V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	90	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V_S = 2.5V to 10V, V_{CM} = 0V	84	105		dB
	Minimum Supply Voltage (Note 6)			2.3	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA		8 50 170	50 130 375	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA		15 85 350	65 180 650	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	±35 ±30	±85 ±65		mA mA
I_S	Supply Current per Amplifier			9	13	mA
	Disable Supply Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V		0.40 0.22	0.9 0.7	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V		150 100	350 300	µA µA
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V		0.1	75	µA
V_L	$\overline{SHDN}$ Pin Input Voltage LOW				0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage HIGH		$V^+ – 0.5$			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω		50		ns
GBW	Gain Bandwidth Product	Frequency = 6MHz		325		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V		125		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, V_{OUT} = $4V_{P-P}$		10		MHz
HD	Harmonic Distortion	V_S = 5V, A_V = 1, R_L = 1k, V_O = $2V_{P-P}$, f_C = 5MHz		–78		dBc
t_S	Settling Time	0.01%, V_S = 5V, V_{STEP} = 2V, A_V = 1, R_L = 1k		60		ns
ΔG	Differential Gain (NTSC)	V_S = 5V, A_V = 2, R_L = 150		0.015		%
Δθ	Differential Phase (NTSC)	V_S = 5V, A_V = 2, R_L = 150		0.05		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C < T_A < 70°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$	●		200	700	µV
		$V_{CM} = V^-$	●		200	700	µV
		$V_{CM} = V^+$ (LT1806 SOT-23)	●		200	850	µV
		$V_{CM} = V^-$ (LT1806 SOT-23)	●		200	850	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	$V_{CM} = V^+$	●		1.5	5	µV/°C
		$V_{CM} = V^-$	●		1.5	5	µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		100	700	µV
		$V_{CM} = V^-$ to V^+ (LT1806 SOT-23)	●		100	850	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$, $V_{CM} = V^+$	●		300	1200	µV
I_B	Input Bias Current	$V_{CM} = V^+ – 0.2V$	●		1	5	µA
		$V_{CM} = V^- + 0.4V$	●	–15	–5		µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		6	20	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+ – 0.2V$	●		0.03	1.5	µA
		$V_{CM} = V^- + 0.4V$	●		0.05	3.5	µA
I_{OS}	Input Offset Current	$V_{CM} = V^+ – 0.2V$	●		0.03	0.75	µA
		$V_{CM} = V^- + 0.4V$	●		0.05	1.80	µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		0.08	2.55	µA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2	●	60	175		V/mV
		V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2	●	7.5	20		V/mV
		V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to V_S/2	●	45	140		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^-$ to V^+	●	77	94		dB
		V_S = 3V, $V_{CM} = V^-$ to V^+	●	72	89		dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_S = 5V, $V_{CM} = V^-$ to V^+	●	71	94		dB
		V_S = 3V, $V_{CM} = V^-$ to V^+	●	66	89		dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	88	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V_S = 2.5V to 10V, V_{CM} = 0V	●	82	105		dB
	Minimum Supply Voltage (Note 6)	$V_{CM} = V_O$ = 0.5V	●		2.3	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		12	60	mV
		I_{SINK} = 5mA	●		60	140	mV
		I_{SINK} = 25mA	●		180	425	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		30	120	mV
		I_{SOURCE} = 5mA	●		110	220	mV
		I_{SOURCE} = 25mA	●		360	700	mV
I_{SC}	Short-Circuit Current	V_S = 5V	●	±30	±65		mA
		V_S = 3V	●	±25	±55		mA
I_S	Supply Current per Amplifier		●		10	14	mA
	Disable Supply Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V	●		0.40	1.1	mA
		V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	●		0.22	0.9	mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V	●		160	400	µA
		V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	●		110	350	µA
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		1		µA
V_L	$\overline{SHDN}$ Pin Input Voltage LOW		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage HIGH		●	$V^+ – 0.5$			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω	●		50		ns
GBW	Gain Bandwidth Product	Frequency = 6MHz	●		300		MHz
SR	Slew Rate	V_S = 5V, A_V = –1, R_L = 1k, V_O = 4V	●		100		V/µs
FPBW	Full Power Bandwidth	V_S = 5V, $V_O = 4V_{P-P}$	●		8		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = 5V, 0V; V_S = 3V, 0V; $V_{\overline{SHDN}}$ = open; V_{CM} = V_{OUT} = half supply, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$ $V_{CM} = V^+$ (LT1806 SOT-23) $V_{CM} = V^-$ (LT1806 SOT-23)	● ● ● ●		200 200 200 200	800 800 950 950	µV µV µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		1.5 1.5	5 5	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ $V_{CM} = V^-$ to V^+ (LT1806 SOT-23)	● ●		100 100	800 950	µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+$, $V_{CM} = V^-$	●		200	1400	µV
I_B	Input Bias Current	$V_{CM} = V^+ – 0.2V$ $V_{CM} = V^- + 0.4V$	● ●	 –16	1 –5	6	µA µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		6	22	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+ – 0.2V$ $V_{CM} = V^- + 0.4V$	● ●		0.02 0.05	1.8 4.0	µA µA
I_{OS}	Input Offset Current	$V_{CM} = V^+ – 0.2V$ $V_{CM} = V^- + 0.4V$	● ●		0.02 0.05	0.9 2.1	µA µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		0.07	3	µA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 0.5V to 4.5V, R_L = 1k to V_S/2 V_S = 5V, V_O = 1V to 4V, R_L = 100Ω to V_S/2 V_S = 3V, V_O = 0.5V to 2.5V, R_L = 1k to V_S/2	● ● ●	50 6 35	140 16 100	 	V/mV V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+	● ●	75 71	94 89	 	dB dB
	CMRR Match (Channel-to-Channel) (Note 10)	V_S = 5V, V_{CM} = V^- to V^+ V_S = 3V, V_{CM} = V^- to V^+	● ●	69 65	94 89	 	dB dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V_S = 2.5V to 10V, V_{CM} = 0V	●	86	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V_S = 2.5V to 10V, V_{CM} = 0V	●	80	105		dB
	Minimum Supply Voltage (Note 6)	$V_{CM} = V_O$ = 0.5V	●		2.3	2.5	V
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		15 65 170	70 150 400	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		30 110 350	130 240 700	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	● ●	±22 ±20	±45 ±40	 	mA mA
I_S	Supply Current per Amplifier		●		11	16	mA
	Disable Supply Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3.V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	● ●		0.4 0.3	1.2 1.0	mA mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	V_S = 5V, $V_{\overline{SHDN}}$ = 0.3V V_S = 3V, $V_{\overline{SHDN}}$ = 0.3V	● ●		170 120	450 400	µA µA
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		1.2		µA
V_L	$\overline{SHDN}$ Pin Input Voltage LOW		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage HIGH		●	$V^+ – 0.5$			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω	●		50		ns
GBW	Gain Bandwidth Product	Frequency = 6MHz	●		250		MHz
SR	Slew Rate	V_S= 5V, A_V = –1, R_L= 1k, V_O = 4V	●		80		V/µV
FPBW	Full Power Bandwidth	V_S = 5V, V_O = $4V_{P-P}$	●		6		MHz

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = ±5V, $V_{\overline{SHDN}}$ = open; V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$ $V_{CM} = V^+$ (LT1806 SOT-23) $V_{CM} = V^-$ (LT1806 SOT-23)		100 100 100 100	700 700 750 750	µV µV µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+ $V_{CM} = V^-$ to V^+ (LT1806 SOT-23)		50 50	700 750	µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$, $V_{CM} = V^+$		200	1200	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$	 –14	1 –5	5	µA µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.2V$ to V^+		6	19	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$		0.03 0.05	1.4 3.2	µA µA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^- + 0.2V$		0.03 0.04	0.7 1.6	µA µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.2V$ to V^+		0.07	2.3	µA
	Input Noise Voltage	0.1Hz to 10Hz		800		nV_{P-P}
e_n	Input Noise Voltage Density	f = 10kHz		3.5		$nV/\sqrt{Hz}$
i_n	Input Noise Current Density	f = 10kHz		1.5		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 100kHz		2		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –2.5V to 2.5V, R_L = 100Ω	100 10	300 27		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	83	106		dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$ to V^+	77	106		dB
	Input Common Mode Range		V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 10V, V^- = 0V	90	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V^+ = 2.5V to 10V, V^- = 0V	84	105		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 25mA		14 55 180	60 140 450	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 25mA		20 90 360	70 200 700	mV mV mV
I_{SC}	Short-Circuit Current		±40	±85		mA
I_S	Supply Current per Amplifier			11	16	mA
	Disable Supply Current	$V_{\overline{SHDN}}$ = 0.3V		0.4	1.2	mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V		150	350	µA
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V		0.3	75	µA
V_L	$\overline{SHDN}$ Pin Input Voltage LOW				0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage HIGH		V^+ – 0.5			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω		50		ns
GBW	Gain Bandwidth Product	Frequency = 6MHz	170	325		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±3V	70	140		V/µs
FPBW	Full Power Bandwidth	$V_O = 8V_{P-P}$		5.5		MHz
HD	Harmonic Distortion	A_V = 1, R_L = 1k, $V_O = 2V_{P-P}$, f_C = 5MHz		–80		dBc
t_S	Settling Time	0.01%, V_{STEP} = 8V, A_V = 1, R_L = 1k		120		ns
ΔG	Differential Gain (NTSC)	A_V = 2, R_L = 150		0.01		%
Δθ	Differential Phase (NTSC)	A_V = 2, R_L = 150		0.01		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the 0°C < T_A < 70°C temperature range. V_S = ±5V, $V_{\overline{SHDN}}$ = open; V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$	●		200	800	µV
		$V_{CM} = V^-$	●		200	800	µV
		$V_{CM} = V^+$ (LT1806 SOT-23)	●		200	900	µV
		$V_{CM} = V^-$ (LT1806 SOT-23)	●		200	900	µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	$V_{CM} = V^+$	●		1.5	5	µV/°C
		$V_{CM} = V^-$	●		1.5	5	µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+	●		100	800	µV
		$V_{CM} = V^-$ to V^+ (LT1806 SOT-23)	●		100	900	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$, $V_{CM} = V^+$	●		300	1400	µV
I_B	Input Bias Current	$V_{CM} = V^+ – 0.2V$	●		1	6	µA
		$V_{CM} = V^- + 0.4V$	●	–15	–6		µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		7	21	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+ – 0.2V$	●		0.03	1.8	µA
		$V_{CM} = V^- + 0.4V$	●		0.04	3.8	µA
I_{OS}	Input Offset Current	$V_{CM} = V^+ – 0.2V$	●		0.03	0.9	µA
		$V_{CM} = V^- + 0.4V$	●		0.04	1.9	µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		0.07	2.8	µA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k	●	80	250		V/mV
		V_O = –2.5V to 2.5V, R_L = 100Ω	●	8	25		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	81	100		dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$ to V^+	●	75	100		dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 10V, V^- = 0V	●	88	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)	V^+ = 2.5V to 10V, V^- = 0V	●	82	106		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load	●		18	80	mV
		I_{SINK} = 5mA	●		60	160	mV
		I_{SINK} = 25mA	●		185	500	mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load	●		40	140	mV
		I_{SOURCE} = 5mA	●		110	240	mV
		I_{SOURCE} = 25mA	●		360	750	mV
I_{SC}	Short-Circuit Current		●	±35	±75		mA
I_S	Supply Current per Amplifier		●		14	20	mA
	Disable Supply Current	$V_{\overline{SHDN}}$ = 0.3V	●		0.4	1.4	mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		160	400	µA
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		1		µA
V_L	$\overline{SHDN}$ Pin Input Voltage LOW		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage HIGH		●	$V^+ – 0.5$			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω	●		50		ns
GBW	Gain Bandwidth Product	Frequency = 6MHz	●	150	300		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measure at V_O = ±3V	●	60	120		V/µs
FPBW	Full Power Bandwidth	$V_O = 8V_{P-P}$	●		4.5		MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C < T_A < 85°C temperature range. V_S = ±5V, $V_{\overline{SHDN}}$ = open; V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$ $V_{CM} = V^+$ (LT1806 SOT-23) $V_{CM} = V^-$ (LT1806 SOT-23)	● ● ● ●		200 200 200 200	900 900 975 975	µV µV µV µV
V_{OS} TC	Input Offset Voltage Drift (Note 8)	$V_{CM} = V^+$ $V_{CM} = V^-$	● ●		1.5 1.5	5 5	µV/°C µV/°C
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+ $V_{CM} = V^-$ to V^+ (LT1806 SOT-23)	● ●		100 100	900 975	µV µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$ to V^+	●		300	1600	µV
I_B	Input Bias Current	$V_{CM} = V^+ – 0.2V$ $V_{CM} = V^- + 0.4V$	● ●	 –16	1.2 –5	7	µA µA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		6	23	µA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^+ – 0.2V$ $V_{CM} = V^- + 0.4V$	● ●		0.03 0.04	2.0 4.5	µA µA
I_{OS}	Input Offset Current	$V_{CM} = V^+ – 0.2V$ $V_{CM} = V^- + 0.4V$	● ●		0.03 0.04	1.0 2.2	µA µA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^- + 0.4V$ to $V^+ – 0.2V$	●		0.07	3.2	µA
A_{VOL}	Large-Signal Voltage Gain	V_O = –4V to 4V, R_L = 1k V_O = –2V to 2V, R_L =100Ω	● ●	60 7	175 17		V/mV V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	●	80	100		dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{CM} = V^-$ to V^+	●	74	100		dB
	Input Common Mode Range		●	V^-		V^+	V
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 10V, V^- = 0V	●	86	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)		●	80	105		dB
V_{OL}	Output Voltage Swing LOW (Note 7)	No Load I_{SINK} = 5mA I_{SINK} = 20mA	● ● ●		20 65 200	100 170 500	mV mV mV
V_{OH}	Output Voltage Swing HIGH (Note 7)	No Load I_{SOURCE} = 5mA I_{SOURCE} = 20mA	● ● ●		50 115 360	160 260 700	mV mV mV
I_{SC}	Short-Circuit Current		●	±25	±55		mA
I_S	Supply Current		●		15	22	mA
	Disable Supply Current	$V_{\overline{SHDN}}$ = 0.3V	●		0.45	1.5	mA
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$ = 0.3V	●		170	450	µA
	Shutdown Output Leakage Current	$V_{\overline{SHDN}}$ = 0.3V	●		1.2		µA
V_L	$\overline{SHDN}$ Pin Input Voltage LOW		●			0.3	V
V_H	$\overline{SHDN}$ Pin Input Voltage HIGH		●	$V^+ – 0.5$			V
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ = 0.3V to 4.5V, R_L = 100Ω	●		80		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ = 4.5V to 0.3V, R_L = 100Ω	●		50		ns
GBW	Gain Bandwidth Product	Frequency = 6MHz	●	125	290		MHz
SR	Slew Rate	A_V = –1, R_L = 1k, V_O = ±4V, Measured at V_O = ±3V	●	50	100		V/µs
FPBW	Full Power Bandwidth	$V_O = 8V_{P-P}$	●		4		MHz

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

ELECTRICAL CHARACTERISTICS

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1806C/LT1806I and LT1807C/LT1807I are guaranteed functional over the temperature range of –40°C and 85°C.

Note 5: The LT1806C/LT1807C are guaranteed to meet specified performance from 0°C to 70°C. The LT1806C/LT1807C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1806I/LT1807I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

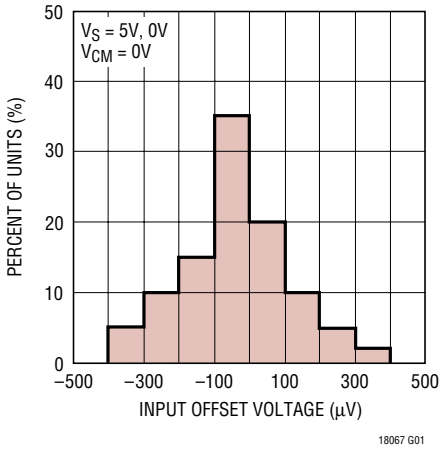
Note 8: This parameter is not 100% tested.

Note 9: Thermal resistance varies depending upon the amount of PC board metal attached to the V^- pin of the device. θ_{JA} is specified for a certain amount of 2oz copper metal trace connecting to the V^- pin as described in the thermal resistance tables in the Applications Information section.

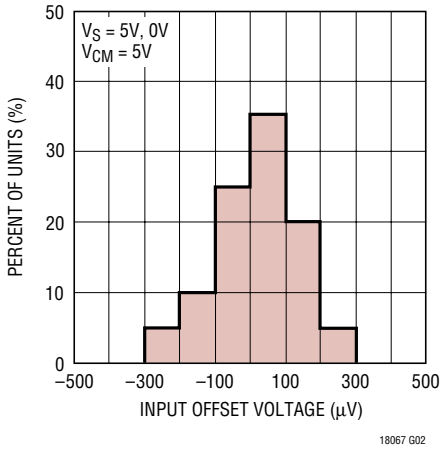
Note 10: Matching parameters are the difference between the two amplifiers of the LT1807.

TYPICAL PERFORMANCE CHARACTERISTICS

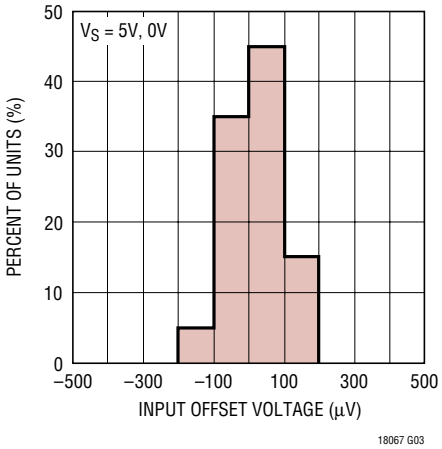
V_{OS} Distribution, V_{CM} = 0V (PNP Stage)



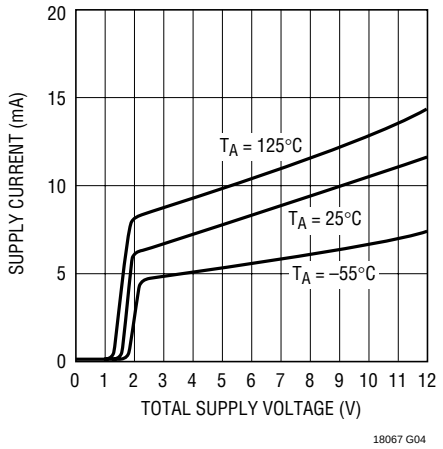
V_{OS} Distribution, V_{CM} = 5V (NPN Stage)



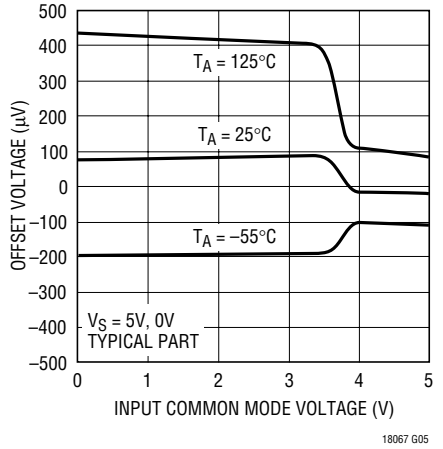
ΔV_{OS} Shift for V_{CM} = 0V to 5V



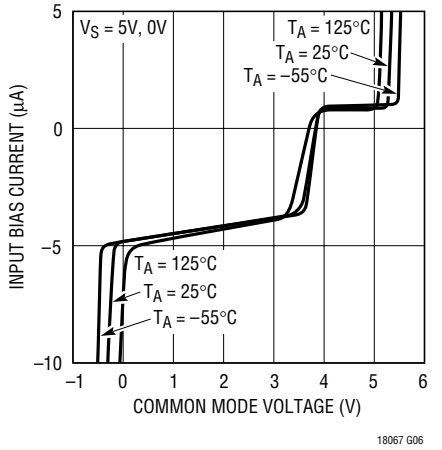
Supply Current per Amp vs Supply Voltage



Offset Voltage vs Input Common Mode

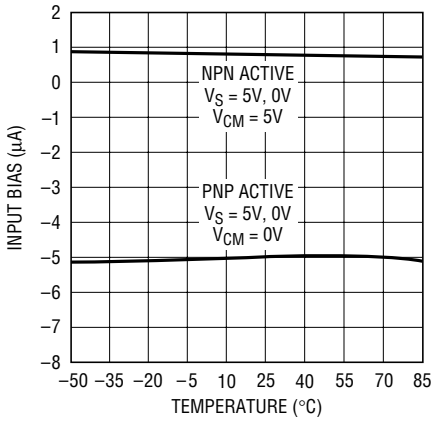


Input Bias Current vs Common Mode Voltage

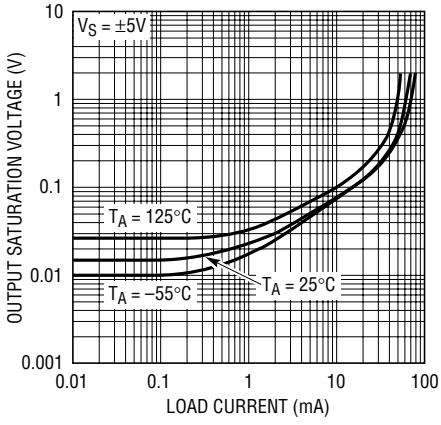


TYPICAL PERFORMANCE CHARACTERISTICS

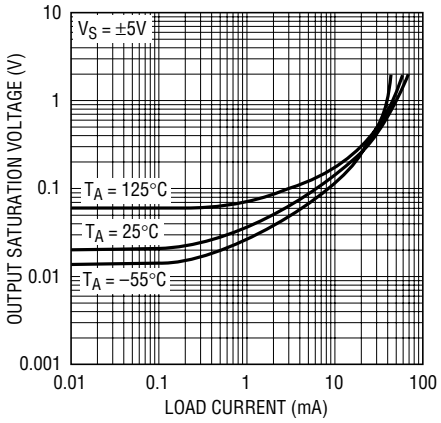
Input Bias Current vs Temperature



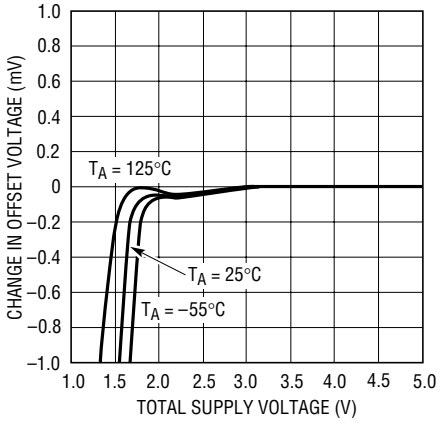
Output Saturation Voltage vs Load Current (Output Low)



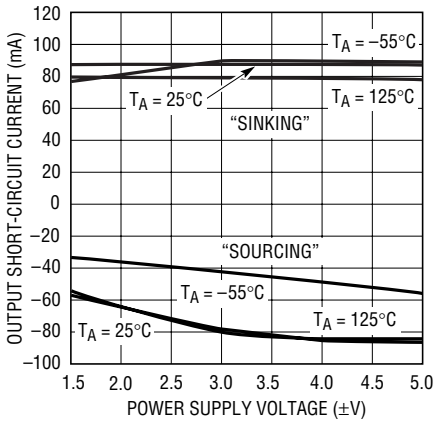
Output Saturation Voltage vs Load Current (Output High)



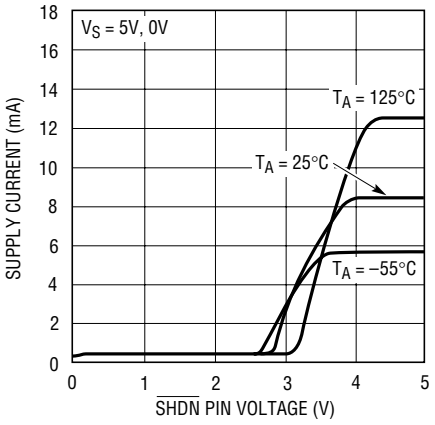
Minimum Supply Voltage



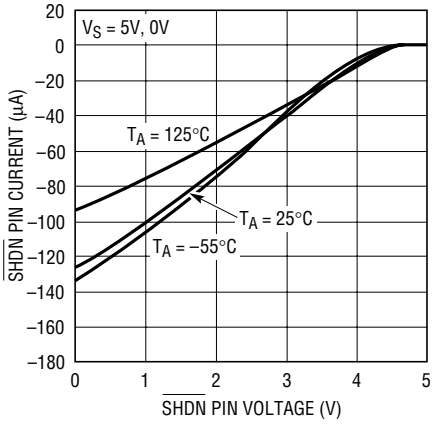
Output Short-Circuit Current vs Power Supply Voltage



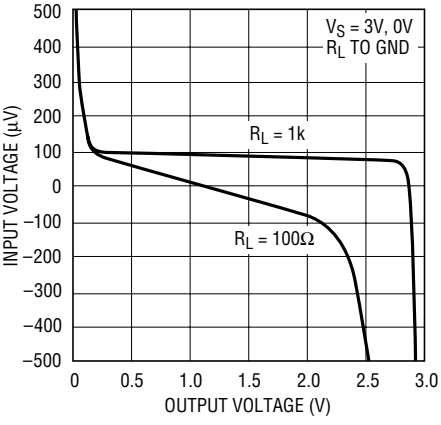
Supply Current vs $\overline{\text{SHDN}}$ Pin Voltage



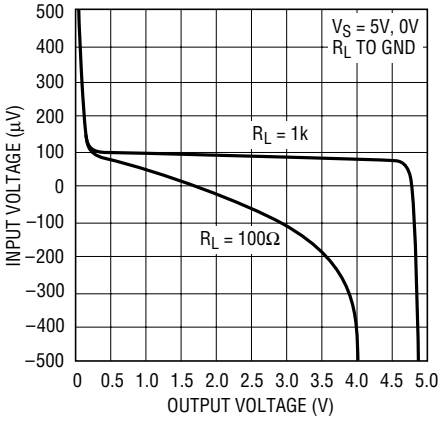
$\overline{\text{SHDN}}$ Pin Current vs $\overline{\text{SHDN}}$ Pin Voltage



Open-Loop Gain

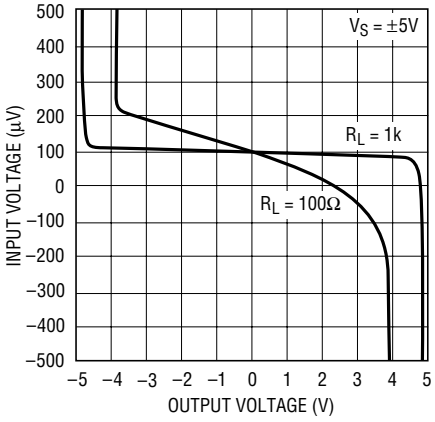


Open-Loop Gain



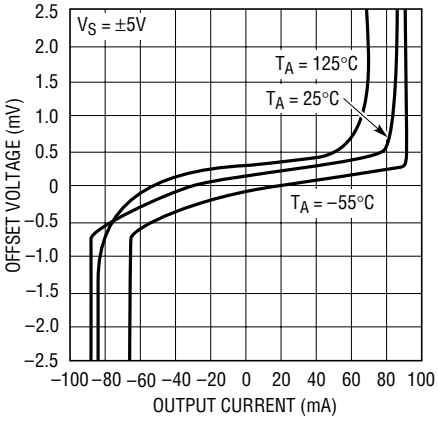
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain



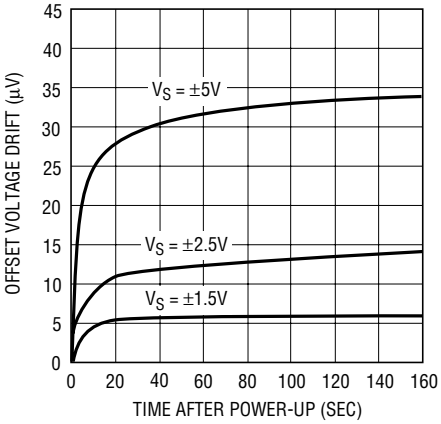
18067 G16

Offset Voltage vs Output Current



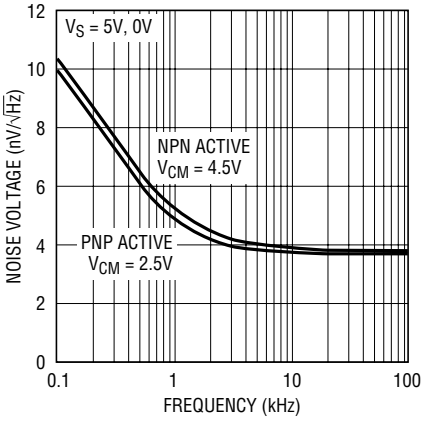
18067 G17

Warm-Up Drift vs Time (LT1806S8)



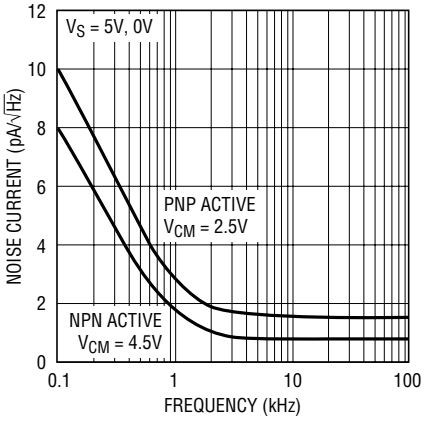
18067 G18

Input Noise Voltage vs Frequency



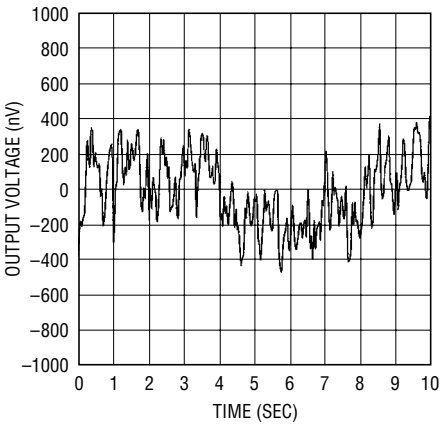
18067 G19

Input Noise Current vs Frequency



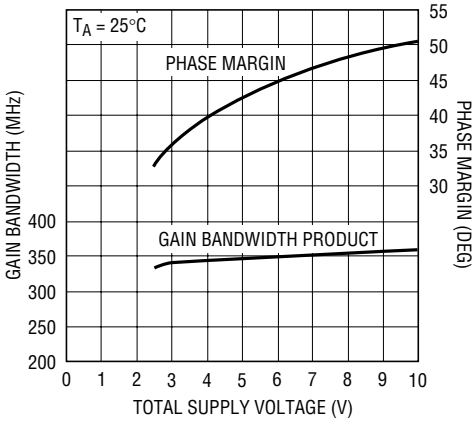
18067 G19

0.1Hz to 10Hz Output Voltage Noise



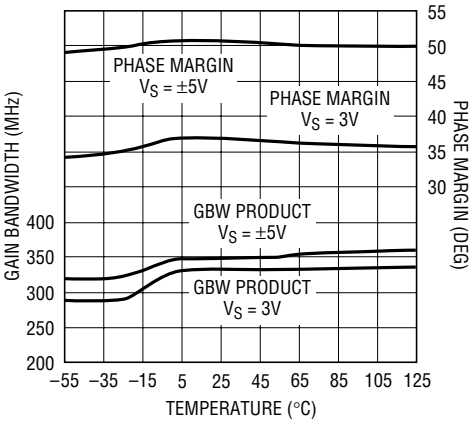
18067 G21

Gain Bandwidth and Phase Margin vs Supply Voltage



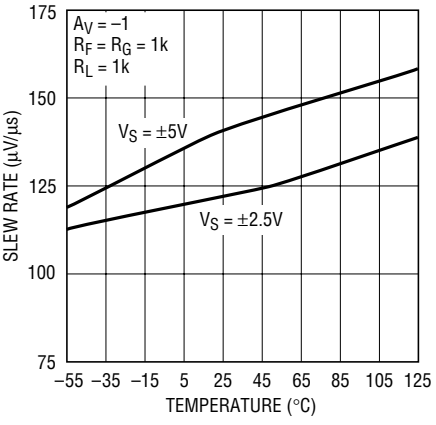
18067 G22

Gain Bandwidth and Phase Margin vs Temperature



18067 G23

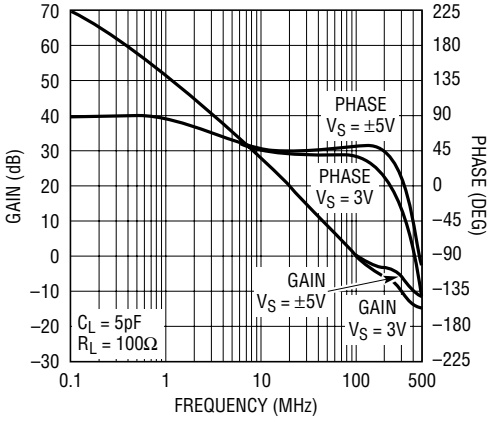
Slew Rate vs Temperature



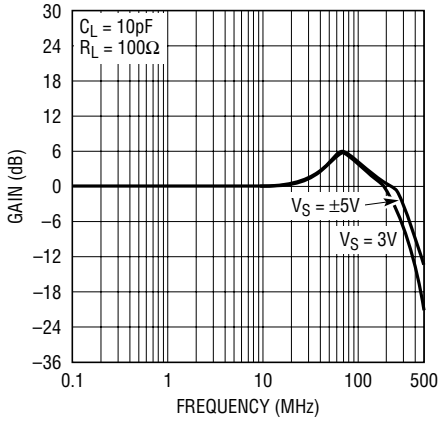
18067 G24

TYPICAL PERFORMANCE CHARACTERISTICS

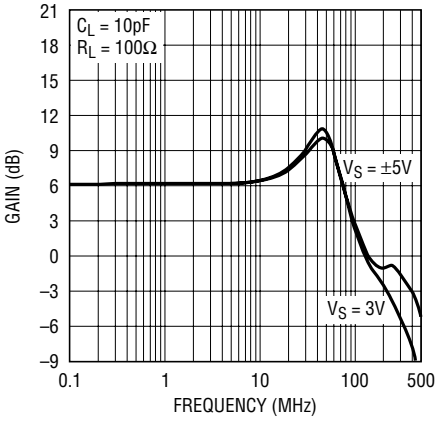
Gain and Phase vs Frequency



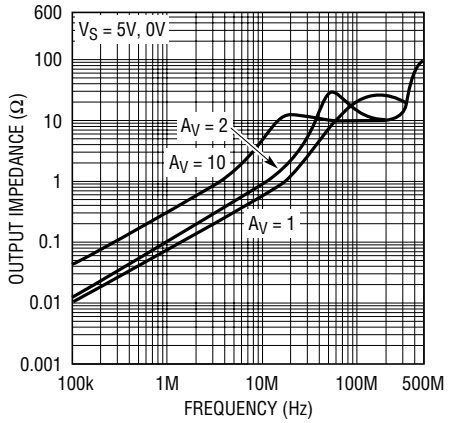
Gain vs Frequency (A_V = 1)



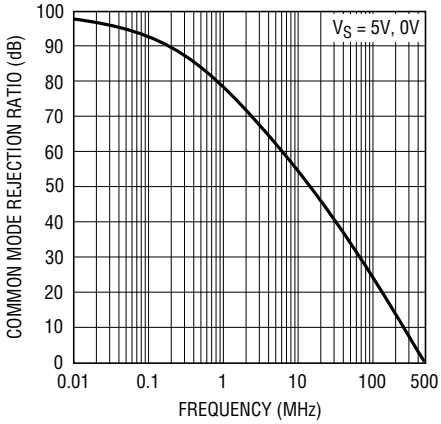
Gain vs Frequency (A_V = 2)



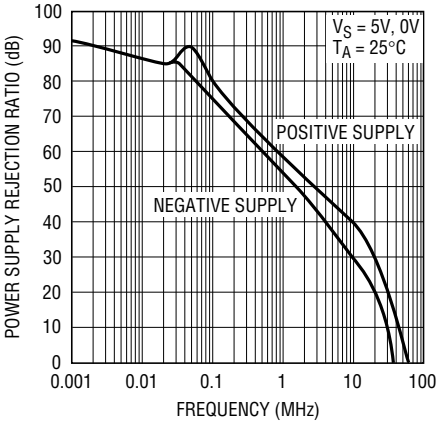
Output Impedance vs Frequency



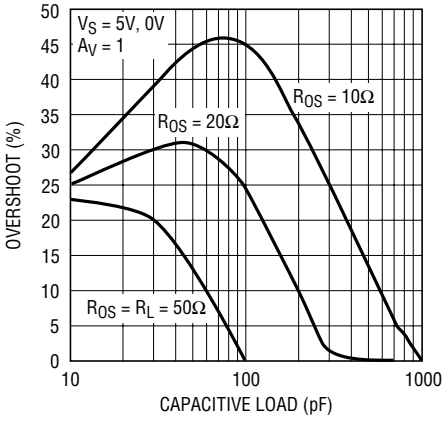
Common Mode Rejection Ratio vs Frequency



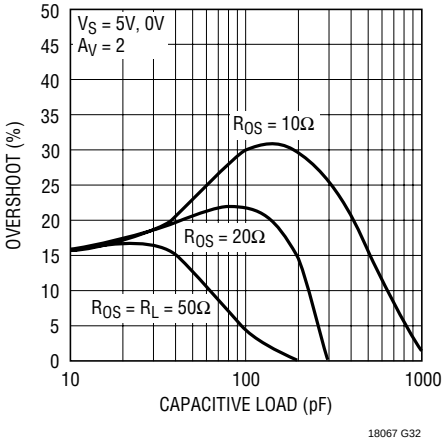
Power Supply Rejection Ratio vs Frequency



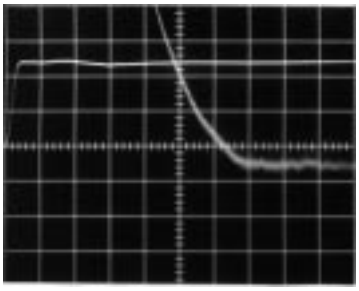
Series Output Resistor vs Capacitive Load



Series Output Resistor vs Capacitive Load



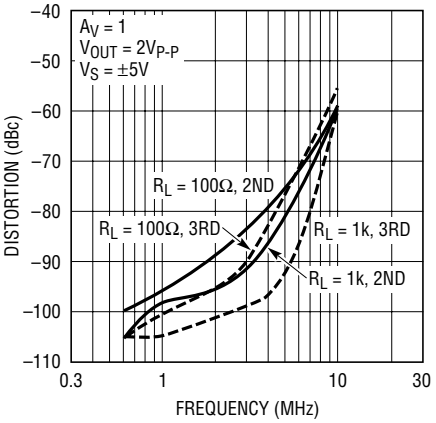
0.01% Settling Time



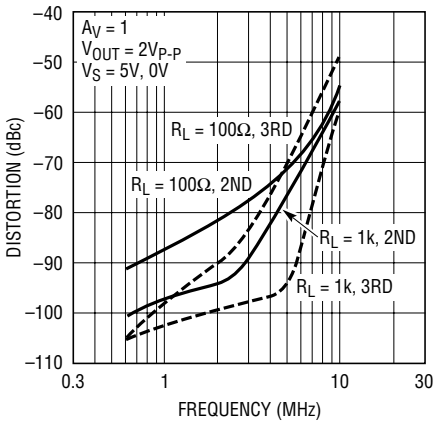
VS = ±5V 20ns/DIV
VOUT = ±4V
RL = 500Ω
tS = 120ns (SETTLING TIME)

TYPICAL PERFORMANCE CHARACTERISTICS

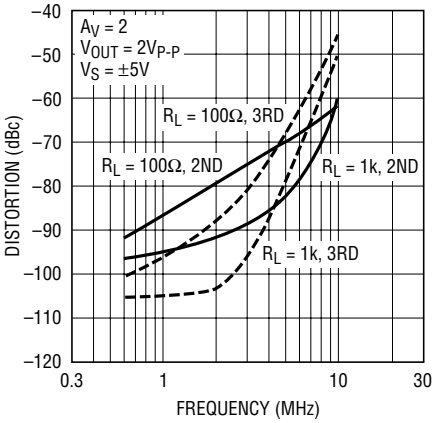
Distortion vs Frequency



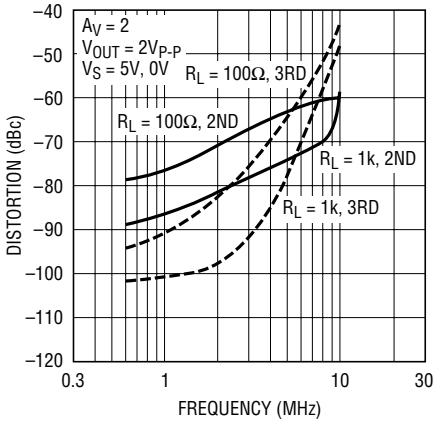
Distortion vs Frequency



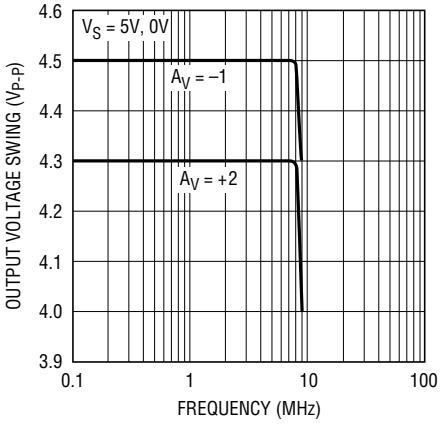
Distortion vs Frequency



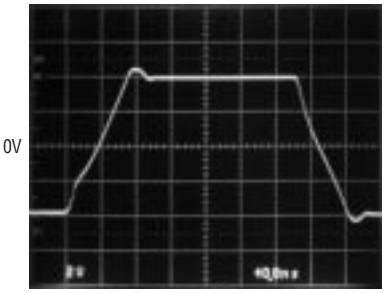
Distortion vs Frequency



Maximum Undistorted Output Signal vs Frequency

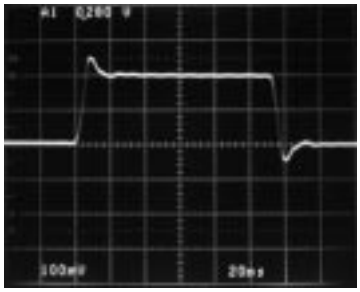


±5V Large-Signal Response



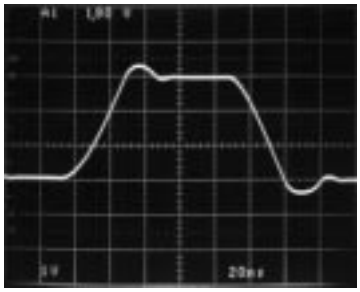
V_S = ±5V 40ns/DIV
FREQ = 1.92MHz
A_V = 1
R_L = 1k

±5V Small-Signal Response



V_S = ±5V 20ns/DIV
FREQ = 4.48MHz
A_V = 1
R_L = 1k

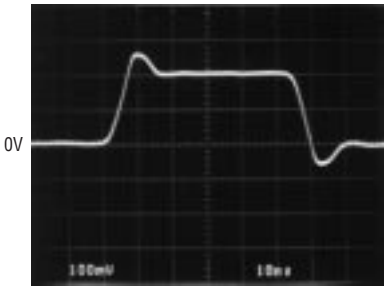
5V Large-Signal Response



V_S = 5V, 0V 20ns/DIV
FREQ = 5.29MHz
A_V = 1
R_L = 1k

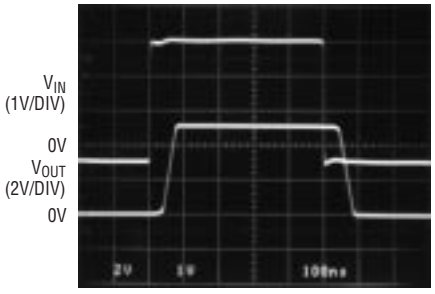
TYPICAL PERFORMANCE CHARACTERISTICS

5V Small-Signal Response



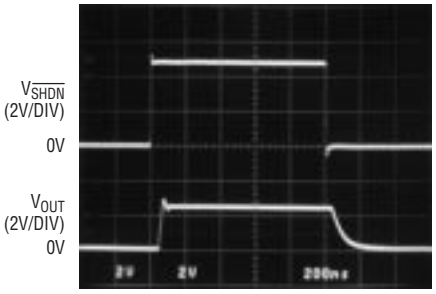
V_S = 5V, 0V 10ns/DIV 18067 G42
A_V = 1
R_L = 1k

Output Overdriven Recovery



V_S = 5V, 0V 100ns/DIV 18067 G43
A_V = 2
R_L = 1k

Shutdown Response



V_S = 5V, 0V 200ns/DIV 18067 G44
A_V = 2
R_L = 100Ω

APPLICATIONS INFORMATION

Rail-to-Rail Characteristics

The LT1806/LT1807 have input and output signal range that covers from negative power supply to positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and a NPN stage Q3/Q4 that are active over different ranges of common mode input voltage. The PNP differential pair is active between the negative supply to approximately 1.5V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair. The PNP pair becomes inactive for the rest of the input common mode range up to the positive supply.

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail to rail constructs the output stage. The capacitors C1 and C2 form the local feedback loops that lower the output

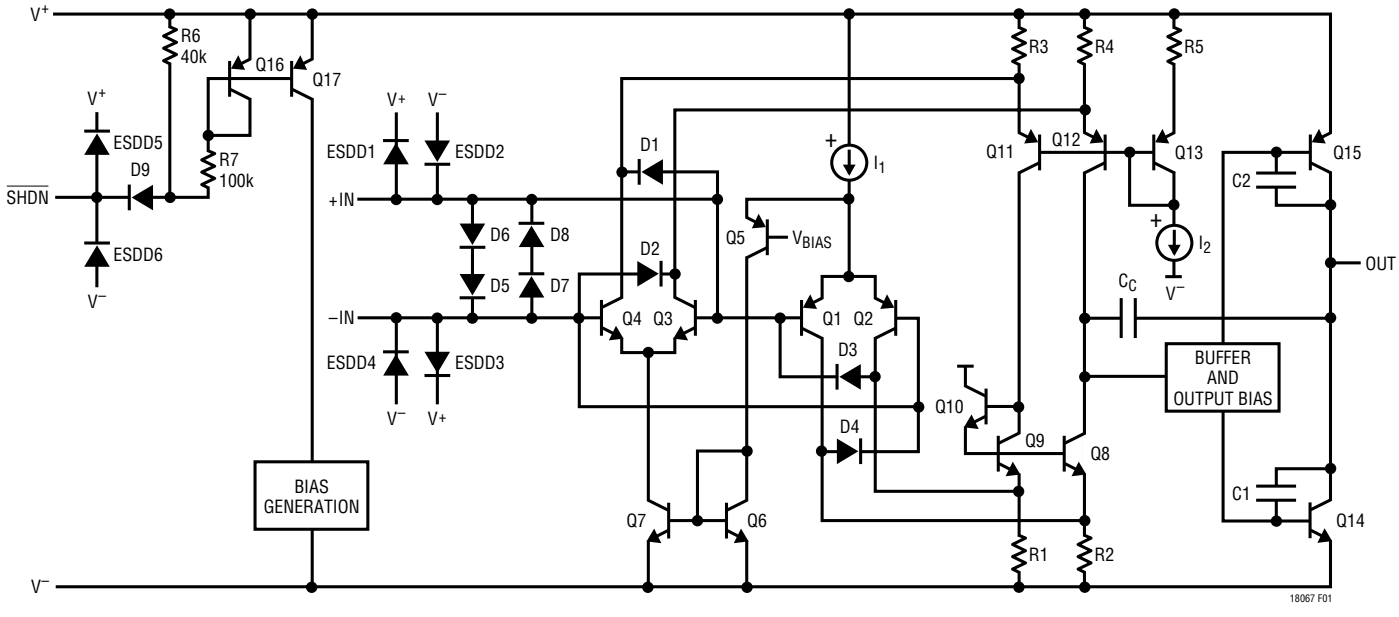


Figure 1. LT1806 Simplified Schematic Diagram

APPLICATIONS INFORMATION

impedance at high frequency. These devices are fabricated on Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT1806/LT1807 amplifiers combine high speed with large output current in a small package, so there is a need to ensure that the die's junction temperature does not exceed 150°C. The LT1806 is housed in an SO-8 package or a 6-lead SOT-23 package and the LT1807 is in an SO-8 or 8-lead MSOP package. All packages have the V^- supply pin fused to the lead frame to enhance the thermal conductance when connecting to a ground plane or a large metal trace. Metal trace and plated through-holes can be used to spread the heat generated by the device to the backside of the PC board. For example, on a 3/32" FR-4 board with 2oz copper, a total of 660 square millimeters connects to Pin 4 of LT1807 in an SO-8 package (330 square millimeters on each side of the PC board) will bring the thermal resistance, θ_{JA}, to about 85°C/W. Without extra metal trace beside the power line connecting to the V^- pin to provide a heat sink, the thermal resistance will be around 105°C/W. More information on thermal resistance for all packages with various metal areas connecting to the V^- pin is provided in Tables 1, 2 and 3.

Table 1. LT1806 6-Lead SOT-23 Package

COPPER AREA TOPSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
270	2500	135°C/W
100	2500	145°C/W
20	2500	160°C/W
0	2500	200°C/W

Device is mounted on topside.

Table 2. LT1806/LT1807 SO-8 Package

COPPER AREA TOPSIDE (mm^2)	COPPER AREA BACKSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
1100	1100	2500	65°C/W
330	330	2500	85°C/W
35	35	2500	95°C/W
35	0	2500	100°C/W
0	0	2500	105°C/W

Device is mounted on topside.

Table 3. LT1807 8-Lead MSOP Package

COPPER AREA TOPSIDE (mm^2)	COPPER AREA BACKSIDE (mm^2)	BOARD AREA (mm^2)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
540	540	2500	110°C/W
100	100	2500	120°C/W
100	0	2500	130°C/W
30	0	2500	135°C/W
0	0	2500	140°C/W

Device is mounted on topside.

Junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum quiescent supply current and at the output voltage which is half of either supply voltage (or the maximum swing if it is less than 1/2 the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + (V_S/2)^2/R_L$$

Example: An LT1807 in SO-8 mounted on a 2500mm^2 area of PC board without any extra heat spreading plane connected to its V^- pin has a thermal resistance of 105°C/W, θ_{JA}. Operating on ±5V supplies with both amplifiers simultaneously driving 50Ω loads, the worst-case power dissipation is given by:

$$P_{D(MAX)} = 2 \bullet (10 \bullet 14mA) + 2 \bullet (2.5)^2/50$$
$$= 0.28 + 0.25 = 0.53W$$

The maximum ambient temperature that the part is allowed to operate is:

$$T_A = T_J - (P_{D(MAX)} \bullet 105°C/W)$$
$$= 150°C - (0.53W \bullet 105°C/W) = 94°C$$

To operate the device at higher ambient temperature, connect more metal area to the V^- pin to reduce the thermal resistance of the package as indicated in Table 2.

APPLICATIONS INFORMATION

Input Offset Voltage

The offset voltage will change depending upon which input stage is active and the maximum offset voltage is guaranteed to less than 550μV. To maintain the precision characteristics of the amplifier, the change of V_{OS} over the entire input common mode range (CMRR) is limited to be less than 550μV on a single 5V and 3V supply.

Input Bias Current

The input bias current polarity depends on a given input common voltage at which the input stage is operating. When the PNP input stage is active, the input bias currents flow out of the input pins. When the NPN input stage is activated, the input bias current flows into the input pins. Because the input offset current is less than the input bias current, matching the source resistances at the input pins will reduce total offset error.

Output

The LT1806/LT1807 can deliver a large output current, so the short-circuit current limit is set around 90mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is continuously short-circuited. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

Overdrive Protection

When the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 5mA. If the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

The LT1806/LT1807's input stages are also protected against large differential input voltages of 1.4V or higher by a pair of back-to-back diodes, D5/D8, that prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worst-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes, ESDD1 to ESDD6, on each pin that are connected to the power supplies as shown in Figure 1.

Capacitive Load

The LT1806/LT1807 are optimized for high bandwidth and low distortion applications. They can drive a capacitive load of about 20pF in a unity-gain configuration, and more for higher gain. When driving a larger capacitive load, a resistor of 10Ω to 50Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads indicate the transient response of the amplifier when driving the capacitive load with a specified series resistor.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1806/LT1807 in a noninverting gain of 2, set up with two 1k resistors and a capacitance of 3pF (part plus PC board) will probably ring in transient response. The pole is formed at 106MHz that will reduce phase margin by 34 degrees when the crossover frequency of the amplifier is around 70MHz. A capacitor of 3pF or higher connected across the feedback resistor will eliminate any ringing or oscillation.

APPLICATIONS INFORMATION

$\overline{\text{SHDN}}$ Pin

The LT1806 has a $\overline{\text{SHDN}}$ pin to reduce the supply current to less than 0.9mA. When the $\overline{\text{SHDN}}$ pin is pulled low, it will generate a signal to power down the device. If the pin is left unconnected, an internal pull-up resistor of 40k will keep the part fully operating as shown in Figure 1. The output will be high impedance during shutdown, and the turn-on and turn-off time is less than 100ns. Because the input is protected by a pair of back to back diodes, the input signal will feed through to the output during shutdown mode if the amplitude of signal between the inputs is larger than 1.4V.

TYPICAL APPLICATIONS

Driving A/D Converter

The LT1806/LT1807 have 60ns settling time to 0.01% on a 2V step signal, and 20Ω output impedance at 100MHz, that makes them ideal for driving high speed A/D converters. With the rail-to-rail input and output, and low supply voltage operation, the LT1806/LT1807 are also desirable for single supply applications. As shown in the application on the front page of this data sheet, the LT1807 drives a 10Msps, 12-bit, LTC1420 ADC in a gain of 20. Driving the LTC1420 differentially will optimize the signal-to-noise ratio, SNR, and the total harmonic distortion, THD, of the A/D converter. The lowpass filter, R5, R6 and C3 reduce noise or distortion products that might come from the input signal. High quality capacitors and resistors, NPO chip capacitor and metal film surface mount resistors, should be used since these components can add to distortion. The voltage glitch of the converter, due to its sampling nature is buffered by the LT1807, and the ability of the amplifier to settle it quickly will affect the spurious free dynamic range of the system. Figure 2 depicts the LT1806 driving LTC1420 at noninverting gain of 2 configuration. The FFT responses show a better than 92dB of spurious free dynamic range, SFDR.

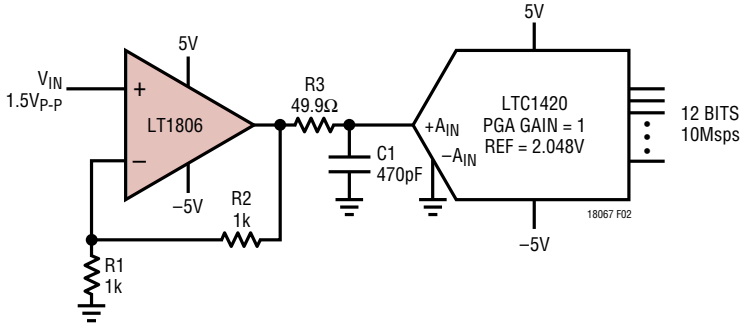


Figure 2. Noninverting A/D Driver

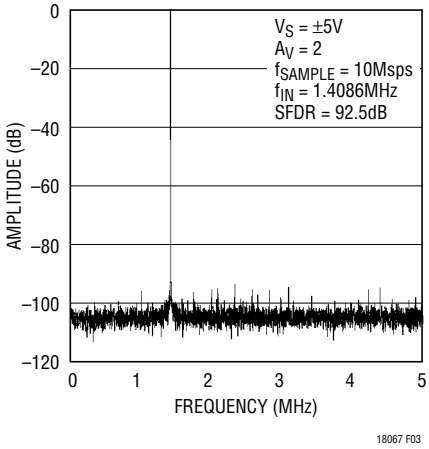


Figure 3. 4096 Point FFT Response

TYPICAL APPLICATIONS

Single Supply Video Line Driver

The LT1806/LT1807 are wideband rail-to-rail op amps with large output current that allows them to drive video signals in low supply applications. Figure 4 depicts a single supply video line driver with AC coupling to minimize the quiescent power dissipation. Resistors R1 and R2 are used to level-shift the input and output to provide the largest signal swing. The gain of 2 is set up with R3 and R4 to restore the signal at V_{OUT}, which is attenuated by 6dB due to the matching of the 75Ω line with the back-terminated resistor, R5. The back termination will eliminate any reflection of the signal that comes from the load. The input termination resistor, R_T, is optional—it is used only if matching of the incoming line is necessary. The values of C1, C2 and C3 are selected to minimize the droop of the luminance signal. In some less stringent requirements, the value of capacitors could be reduced. The –3dB bandwidth of the driver is about 90MHz on 5V supply, and the amount of peaking will vary upon the value of capacitor C4.

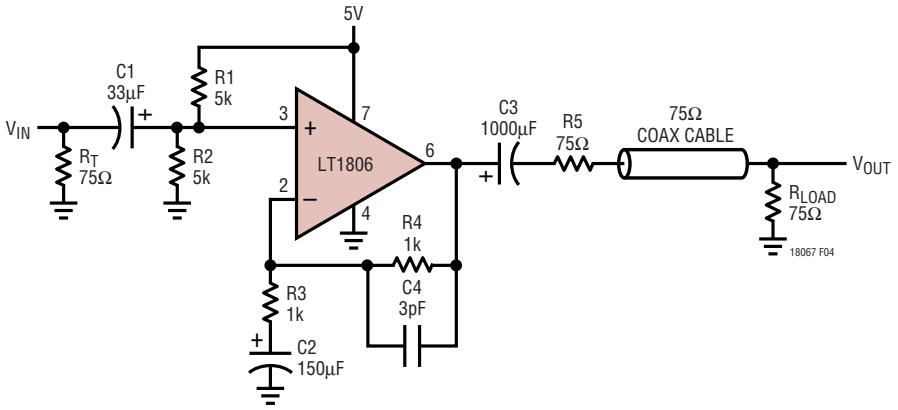


Figure 4. 5V Single Supply Video Line Driver

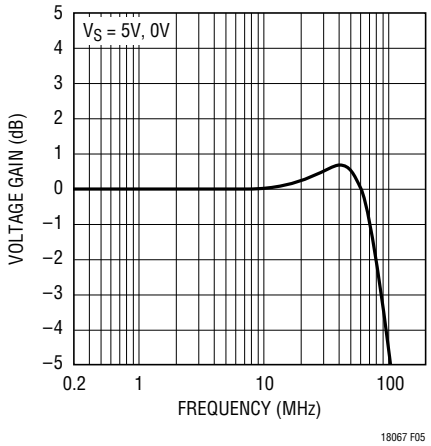


Figure 5. Video Line Driver Frequency Response

TYPICAL APPLICATIONS

Single 3V Supply, 4MHz, 4th Order Butterworth Filter

Benefiting from a low voltage supply operation, low distortion and rail-to-rail output of LT1806/LT1807, a low distortion filter that is suitable for antialiasing can be built as shown in Figure 6.

On a 3V supply, the filter built with LT1807 has a passband of 4MHz with 2.5V_{P-P} signal and stopband that is greater than 70dB to frequency of 100MHz. As an option to minimize the DC offset voltage at the output, connect a series resistor of 365Ω and a bypass capacitor at the noninverting inputs of the amplifiers as shown in Figure 6.

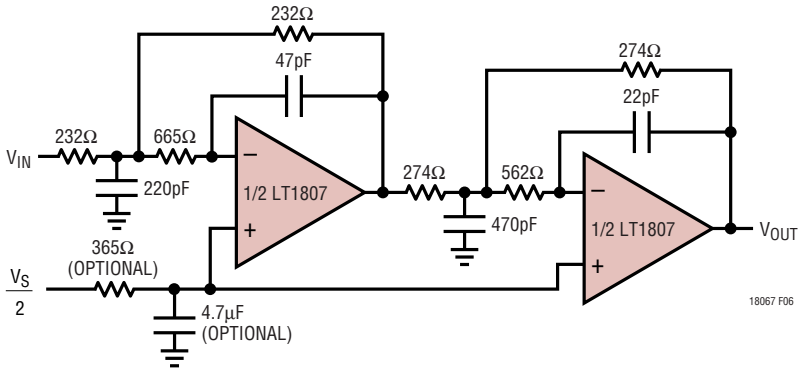


Figure 6. Single 3V Supply, 4MHz, 4th Order Butterworth Filter

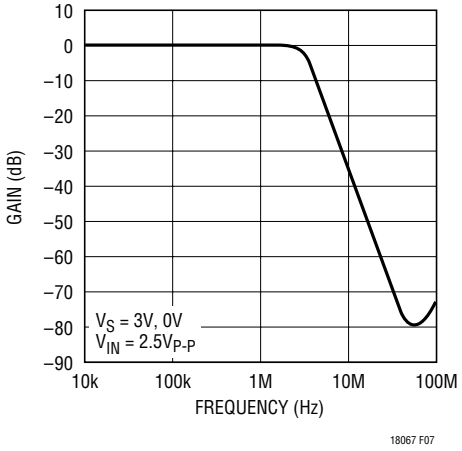


Figure 7. Filter Frequency Response

TYPICAL APPLICATIONS

1MHz Series Resonant Crystal Oscillator with Square and Sinusoid Outputs

Figure 8 shows a classic 1MHz series resonant crystal oscillator. At series resonance, the crystal is a low impedance and the positive feedback connection is what brings about oscillation at the series resonance frequency. The RC feedback around the other path ensures that the circuit does not find a stable DC operating point and refuse to oscillate. The comparator output is a 1MHz square wave with a measured jitter of $28ps_{RMS}$ with a 5V supply and $40ps_{RMS}$ with a 3V supply. On the other side of the crystal, however, is an excellent looking sine wave except for the fact of the small high frequency glitch caused by the fast edge and the crystal capacitance (middle trace of Figure 9). Sinusoid amplitude stability is maintained by the fact that the sine wave is basically a filtered version of the square wave; the usual amplitude control loops associated with sinusoidal oscillators are not immediately necessary.[1] One can make use of this sine wave by buffering and filtering it, and this is the combined task of the LT1806. It is configured as a bandpass filter with a Q of 5 and does a good job of cleaning up and buffering the sine wave. Distortion was measured at –70dBc and –60dBc on the second and third harmonics.

[1]Amplitude will be a linear function of comparator output swing, which is supply dependent and therefore controllable. The important difference here is that any added amplitude stabilization loop will not be faced with the classical task of avoiding regions of nonoscillation versus clipping.

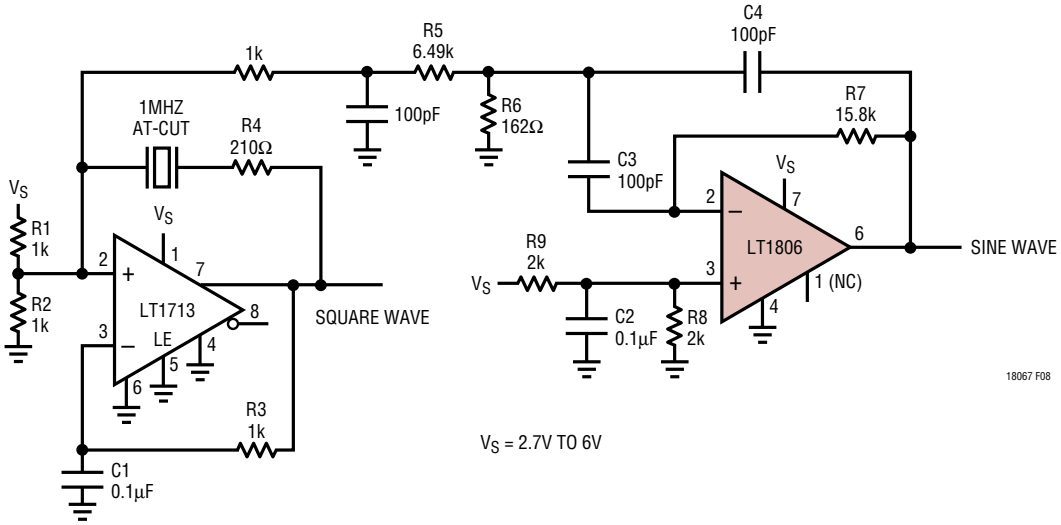


Figure 8. LT1713 Comparator is Configured as a Series Resonant Crystal Oscillator. The LT1806 Op Amp is Configured in a Q = 5 Bandpass Filter with f_C = 1MHz

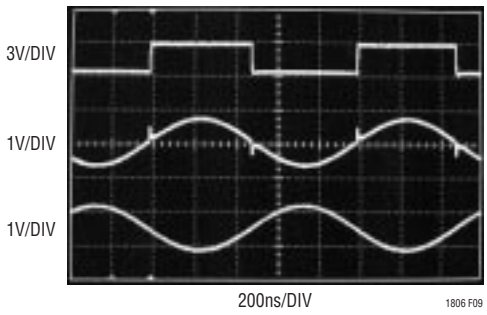


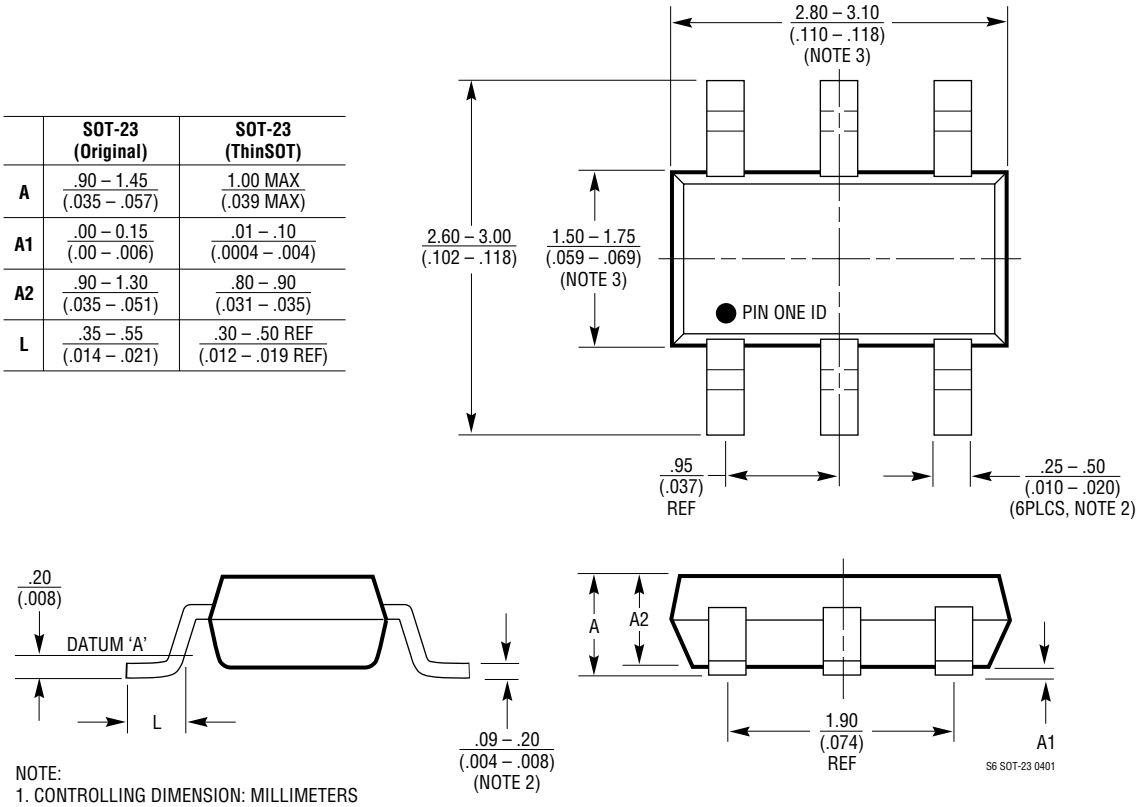
Figure 9. Oscillator Waveforms with V_S = 3V. Top Trace is Comparator Output. Middle Trace is Crystal Feedback to Pin 2 at LT1713. Bottom Trace is Buffered, Inverted and Bandpass Filtered with a Q of 5 by the LT1806

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S6 Package
6-Lead Plastic SOT-23
(Reference LTC DWG # 05-08-1634)
(Reference LTC DWG # 05-08-1636)

	SOT-23 (Original)	SOT-23 (ThinSOT)
A	.90 – 1.45 (.035 – .057)	1.00 MAX (.039 MAX)
A1	.00 – 0.15 (.00 – .006)	.01 – .10 (.0004 – .004)
A2	.90 – 1.30 (.035 – .051)	.80 – .90 (.031 – .035)
L	.35 – .55 (.014 – .021)	.30 – .50 REF (.012 – .019 REF)

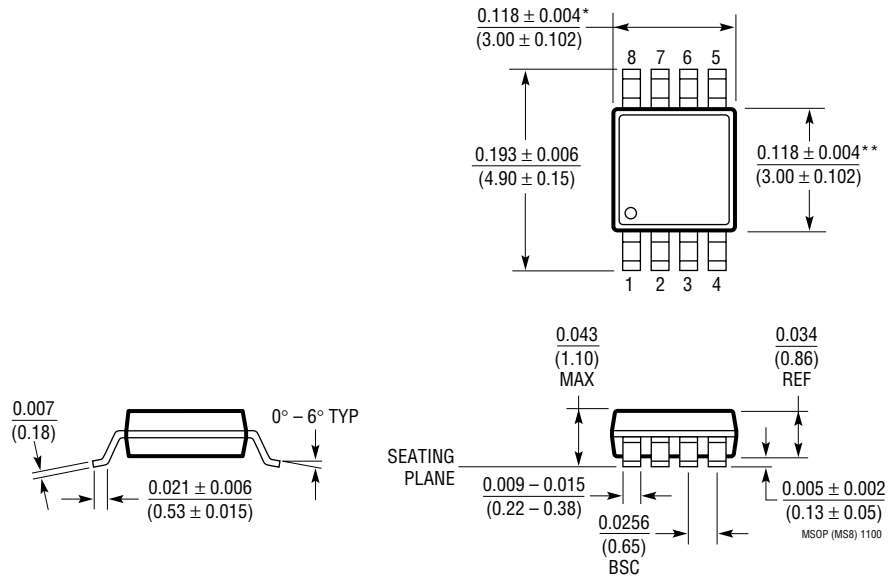


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. DIMENSIONS ARE INCLUSIVE OF PLATING
5. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
6. MOLD FLASH SHALL NOT EXCEED .254mm
7. PACKAGE EIAJ REFERENCE IS:
   SC-74A (EIAJ) FOR ORIGINAL
   JEDEC MO-193 FOR THIN

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660)



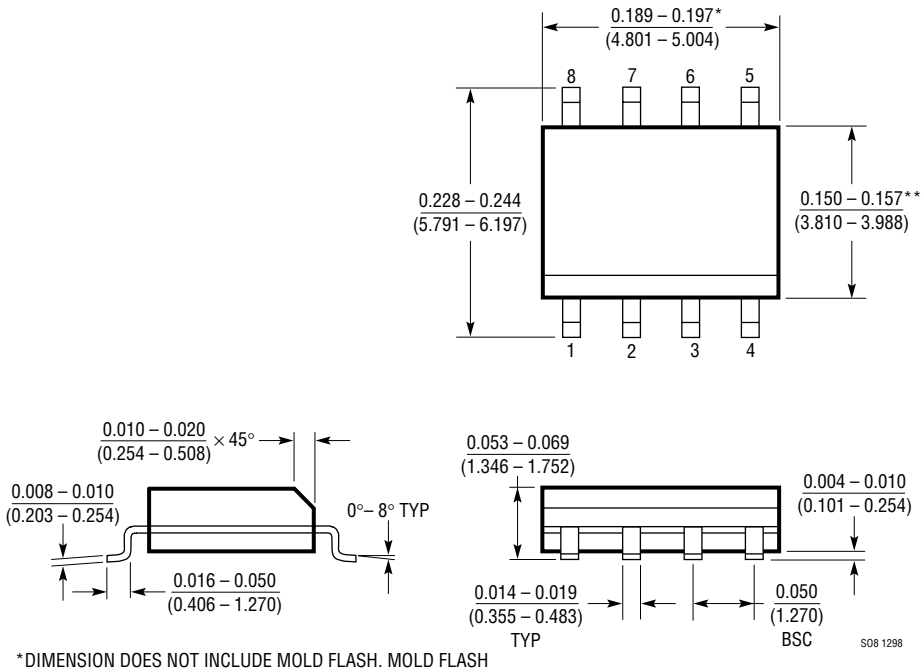
* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

FET Input, Fast, High Gain Photodiode Amplifier

Figure 10 shows a fast, high gain transimpedance amplifier applied to a photodiode. A JFET buffer is used for its extremely low input bias current and high speed. The LT1097 and 2N3904 keep the JFET biased at I_{DSS} for zero offset and lowest voltage noise. The JFET then drives the LT1806, with R_F closing the high speed loop back to the JFET input and setting the transimpedance gain. C4 helps improve the phase margin of the fast loop. Output voltage noise density was measured as $9nV/\sqrt{Hz}$ with R_F short circuited. With R_F varied from 100k to 1M, total output noise was below $1mV_{RMS}$ measured over a 10MHz bandwidth. Table 4 shows results achieved with various values of R_F and Figure 11 shows the time domain response with R_F = 499k.

Table 4. Results Achieved for Various R_F, 1.2V Output Step

R_F	10% to 90% RISE TIME	–3dB BANDWIDTH
100k	64ns	6.8MHz
200k	94ns	4.6MHz
499k	154ns	3MHz
1M	263ns	1.8MHz

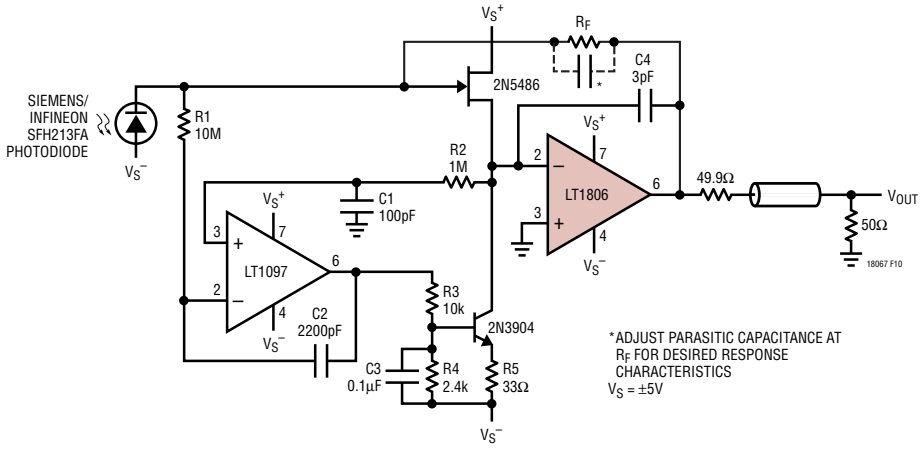


Figure 10. Fast, High Gain Photodiode Amplifier

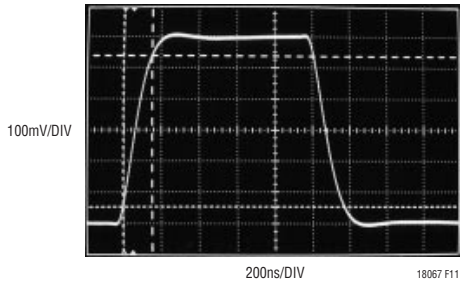


Figure 11. Step Response with R_F = 499k

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1395	400MHz Current Feedback Amplifier	800V/µs Slew Rate, Shutdown
LT1399	Triple 300MHz Current Feedback Amplifier	0.1dB Gain Flatness to 150MHz, Shutdown
LT1632/LT1633	Dual/Quad 45MHz, 45V/µs Rail-to-Rail Input and Output Amplifiers	High DC Accuracy 1.35mV $V_{OS(MAX)}$, 70mA Output Current, Max Supply Current 5.2mA/Amp
LT1809/LT1810	Single/Dual 180MHz Input and Output Rail-to-Rail Amplifiers	350V/µs Slew Rate, Shutdown, Low Distortion –90dBc at 5MHz