5-Bit Programmable Synchronous Switching Regulator Controller for Pentium® II Processor

FEATURES

- **5-Bit Digitally Programmable 1.8V to 3.5V Fixed Output Voltage**
- **Provides All Features Required by the *Intel Pentium® II Processor VRM 8.2 DC/DC Converter Specification***
- Flags for Power Good, Over-Temperature and Overvoltage Fault
- 19A Output Current Capability from a 5V or 12V Supply
- Dual N-Channel MOSFET Synchronous Driver
- Initial Output Accuracy: ±1.5%
- Excellent Output Accuracy: ±2% Typ Over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Adjustable Current Limit Without External Sense Resistors
- Fast Transient Response
- Available in 20-Lead SSOP and SW Packages

APPLICATIONS

- Power Supply for Pentium II, SPARC, ALPHA and PA-RISC Microprocessors
- High Power 5V or 12V to 1.8V-3.5V Regulators

DESCRIPTION

The LTC®1553 is a high power, high efficiency switching regulator controller optimized for 5V or 12V input to 1.8V-3.5V output applications. It features a digitally programmable output voltage, a precision internal reference and an internal feedback system that provides output accuracy of ±1.5% at room temperature and typically ±2% over-temperature, load current and line voltage shifts. The LTC1553 uses a synchronous switching architecture with two external N-channel output devices, providing high efficiency and eliminating the need for a high power, high cost P-channel device. Additionally, it senses the output current across the on-resistance of the upper N-channel FET, providing an adjustable current limit without an external low value sense resistor.

The LTC1553 free-runs at 300kHz and can be synchronized to a faster external clock if desired. It includes all the inputs and outputs required to implement a power supply conforming to the *Intel Pentium® II Processor VRM 8.2 DC/DC Converter Specification*.

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Pentium is a registered trademark of Intel Corporation.

TYPICAL APPLICATION

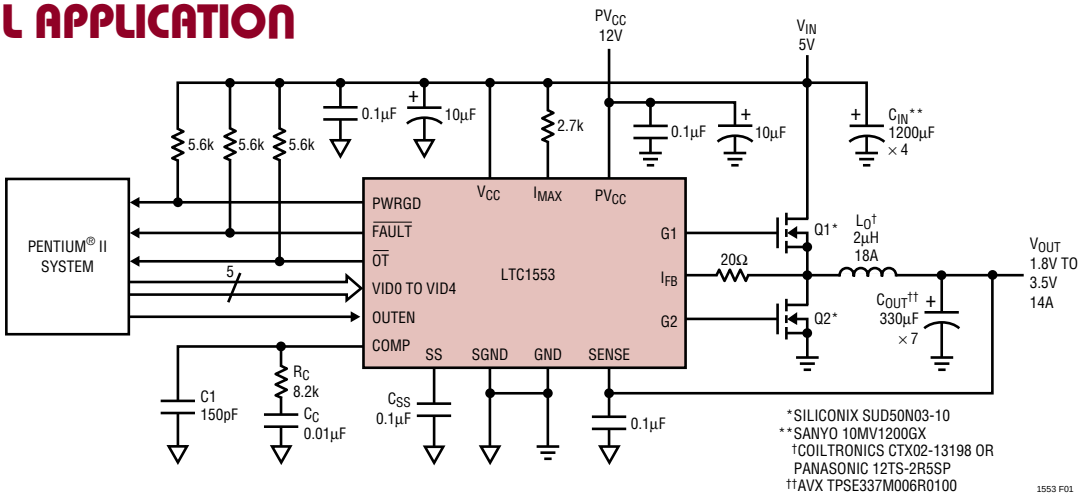


Figure 1. 5V to 1.8V-3.5V Supply Application

ABSOLUTE MAXIMUM RATINGS

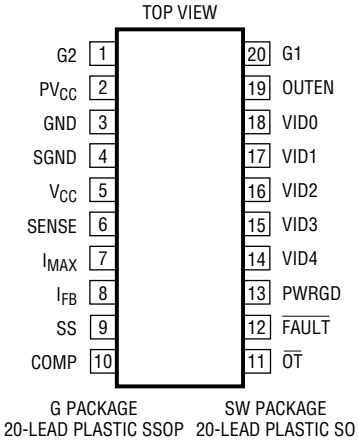
(Note 1)

Supply Voltage
- V_{CC} 9V
- PV_{CC} 20V

Input Voltage
- I_{FB} (Note 2) ..... PV_{CC} + 0.3V
- I_{MAX} ..... –0.3V to 13V
- All Other Inputs ..... –0.3V to V_{CC} + 0.3V

Digital Output Voltage ..... –0.3V to 13V
I_{FB} Input Current (Notes 2, 3) ..... –100mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
20-LEAD PLASTIC SSOP

SW PACKAGE
20-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (SW)

ORDER PART NUMBER

LTC1553CG
LTC1553CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, PV_{CC} = 12V, T_A = 25°C, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		8	V
PV_{CC}	Supply Voltage for G1, G2		●			18	V
V_{FB}	Internal Feedback Voltage	(Note 4)			1.265		V
V_{OUT}	1.8V Initial Output Voltage	With Respect to Rated Output Voltage (Figure 2)		– 27 (–1.5%)		27 (+1.5%)	mV
	2.8V Initial Output Voltage			– 42 (–1.5%)		42 (+1.5%)	mV
	3.5V Initial Output Voltage			– 52 (–1.5%)		52 (+1.5%)	mV
	1.8V Initial Output Voltage		●	– 36 (–2%)		36 (+2%)	mV
	2.8V Initial Output Voltage		●	– 56 (–2%)		56 (+2%)	mV
	3.5V Initial Output Voltage		●	– 70 (–2%)		70 (+2%)	mV
ΔV_{OUT}	Output Load Regulation	I_{OUT} = 0 to 14A (Note 4) (Figure 2)			–5		mV
	Output Line Regulation	V_{IN} = 4.75V to 5.25V, I_{OUT} = 0 (Note 4)(Figure 2)			±1		mV
V_{PWRGD}	Positive Power Good Trip Point	% Above Output Voltage (Figure 2)	●		5	7	%
	Negative Power Good Trip Point	% Below Output Voltage (Figure 2)	●	–7	–5		%
V_{FAULT}	$\overline{FAULT}$ Trip Point	% Above Output Voltage (Figure 2)	●	12	15	20	%
I_{CC}	Operating Supply Current	OUTEN = V_{CC} = 5V (Note 5) (Figure 3)	●		800	1200	µA
	Shutdown Supply Current	OUTEN = 0, VID0 to VID4 Floating (Figure 3)	●		130	250	µA
I_{PVCC}	Supply Current	PV_{CC} = 12V, OUTEN = V_{CC} (Note 6) (Figure 3)			15		mA
		PV_{CC} = 12V, OUTEN = 0, VID0 to VID4 Floating			1		µA
f_{OSC}	Internal Oscillator Frequency	(Figure 4)	●	250	300	350	kHz
V_{SAWL}	V_{COMP} at Minimum Duty Cycle	(Note 4)			1.8		V
V_{SAWH}	V_{COMP} at Maximum Duty Cycle	(Note 4)			2.8		V
G_{ERR}	Error Amplifier Open-Loop DC Gain	(Note 7)	●	40	53		dB
g_{mERR}	Error Amplifier Transconductance	(Note 7)	●	0.9	1.6	2.3	millimho
BW_{ERR}	Error Amplifier –3dB Bandwidth	COMP = Open (Note 4)			400		kHz

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, PV_{CC} = 12V, T_A = 25°C, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IMAX}	I_{MAX} Sink Current	$V_{IMAX} = V_{CC}$	●	150	180	220	µA
I_{SS}	Soft Start Source Current	V_{SS} = 0V, V_{IMAX} = 0V, $V_{IFB} = V_{CC}$	●	–13	–10	–7	µA
I_{SSIL}	Maximum Soft Start Sink Current Under Current Limit	$V_{SENSE} = V_{OUT}$, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V (Notes 8, 9), $V_{SS} = V_{CC}$	●	30	60	150	µA
I_{SSHIL}	Soft Start Sink Current Under Hard Current Limit	V_{SENSE} = 0V, $V_{IMAX} = V_{CC}$, V_{IFB} = 0V	●	20	45		mA
t_{SSHIL}	Hard Current Limit Hold Time	V_{SENSE} = 0V, V_{IMAX} = 4V, $V_{IFB}\downarrow$ from 5V (Note 4)			500		µs
t_{PWRGD}	Power Good Response Time↑	$V_{SENSE}\uparrow$ from 0V to Rated V_{OUT}	●	0.5	1	2	ms
t_{PWRBAD}	Power Good Response Time↓	$V_{SENSE}\downarrow$ from Rated V_{OUT} to 0V	●	200	500	1000	µs
t_{FAULT}	$\overline{FAULT}$ Response Time	$V_{SENSE}\uparrow$ from Rated V_{OUT} to V_{CC}	●	200	500	1000	µs
t_{OT}	$\overline{OT}$ Response Time	OUTEN↓, VID0 to VID4 = 0 (Note 10) (Figure 3)	●	15	40	60	µs
V_{OT}	Over-Temperature Trip Point	OUTEN↓, VID0 to VID4 = 0 (Note 10) (Figure 3)	●	1.9	2	2.12	V
V_{OTDD}	Over-Temperature Driver Disable	OUTEN↓, VID0 to VID4 = 0 (Note 10) (Figure 3)	●	1.6	1.7	1.8	V
V_{SHDN}	Shutdown	OUTEN↓, VID0 to VID4 = 0 (Note 10) (Figure 3)	●			0.8	V
t_r, t_f	Driver Rise and Fall Time	(Figure 4)	●		90	150	ns
t_{NOL}	Driver Nonoverlap Time	(Figure 4)	●	30	100		ns
DC_{MAX}	Maximum G1 Duty Cycle	(Figure 4)	●	77	84	88	%
V_{IH}	VID0 to VID4 Input High Voltage		●	2			V
V_{IL}	VID0 to VID4 Input Low Voltage		●			0.8	V
R_{IN}	VID0 to VID4 Internal Pull-Up Resistance		●	10	20		kΩ
I_{SINK}	Digital Output Sink Current		●	10			mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: When I_{FB} is taken below GND, it will be clamped by an internal diode. This pin can handle input currents greater than 100mA below GND without latchup. In the positive direction, it is not clamped to V_{CC} or PV_{CC}.

Note 3: All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: This parameter is guaranteed by correlation and is not tested directly.

Note 5: The LTC1553 goes into the shutdown mode if VID0 to VID4 are floating. Due to the internal pull-up resistors, there will be an additional 0.25mA/pin if any of the VID0 to VID4 pins are pulled low.

Note 6: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC1553 operating frequency, supply voltage and the external FETs used.

Note 7: The open-loop DC gain and transconductance from the SENSE pin to COMP pin will be $(G_{ERR})(1.265/3.3)$ and $(g_{mERR})(1.265/3.3)$ respectively.

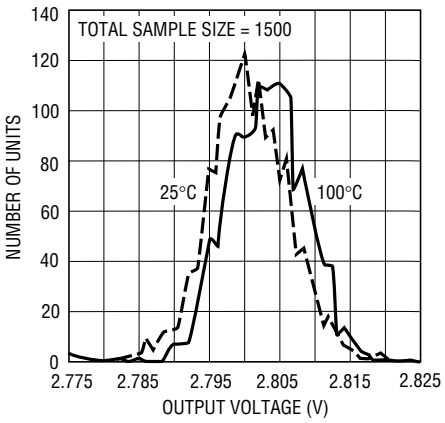
Note 8: The current limiting amplifier can sink but cannot source current. Under normal (not current limited) operation, the output current will be zero.

Note 9: Under typical soft current limit, the net soft start discharge current will be 60µA (I_{SSIL}) + [–10µA(I_{SS})] = 50µA. The soft start sink-to-source current ratio is designed to be 6:1.

Note 10: When VID0 to VID4 are all HIGH, the LTC1553 will be forced to shut down internally. The OUTEN trip voltages are guaranteed by design for all other input codes.

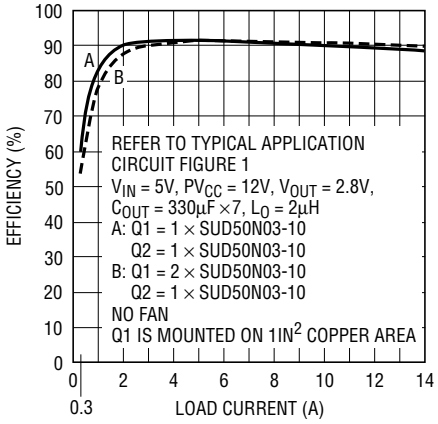
TYPICAL PERFORMANCE CHARACTERISTICS

Typical 2.8V V_{OUT} Distribution



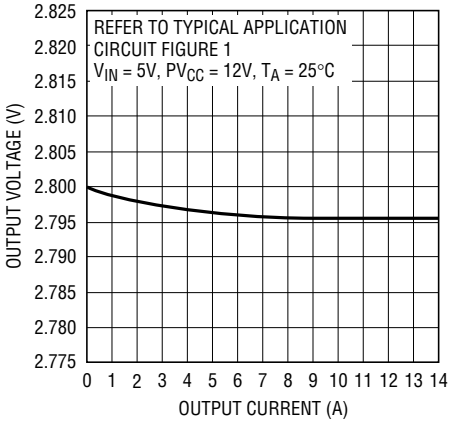
1553 G01

Efficiency vs Load Current



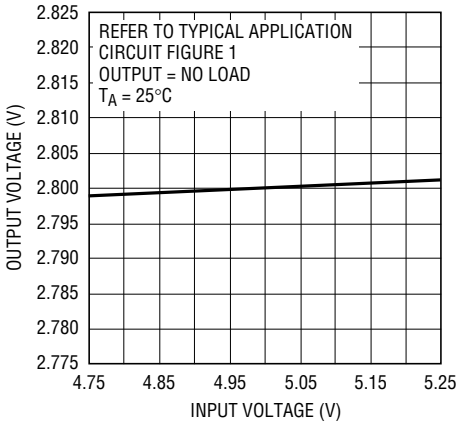
1533 G02

Load Regulation



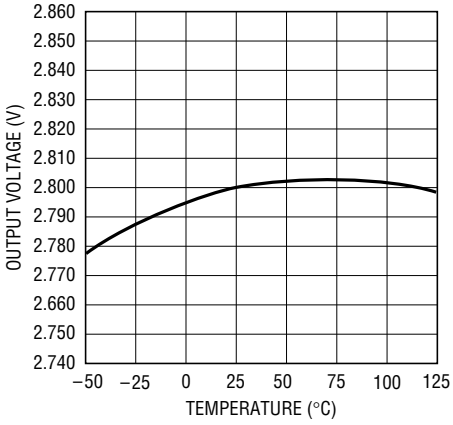
1533 G03

Line Regulation



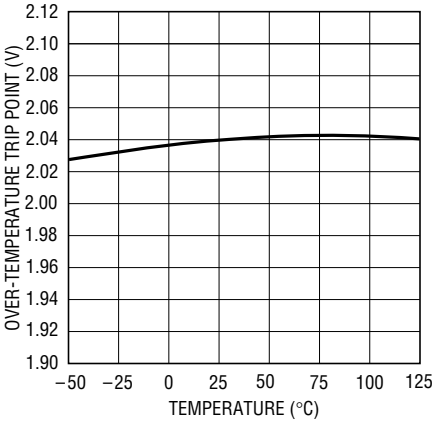
1553 G04

Output Temperature Drift



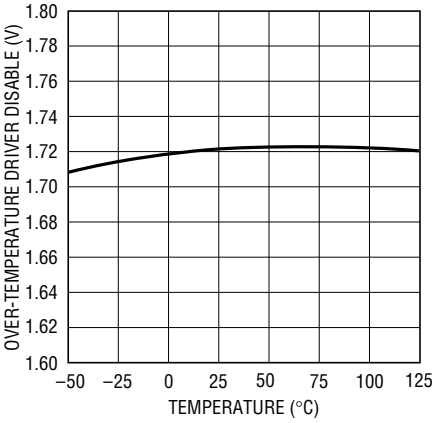
1553 G05

Over-Temperature Trip Point vs Temperature



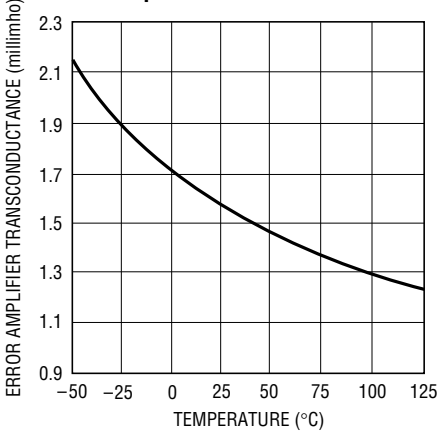
1553 G06

Over-Temperature Driver Disable vs Temperature



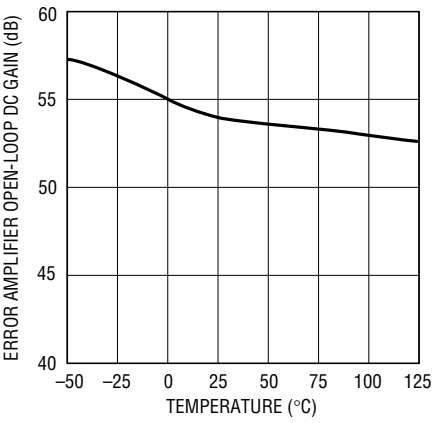
1553 G07

Error Amplifier Transconductance vs Temperature



1553 G08

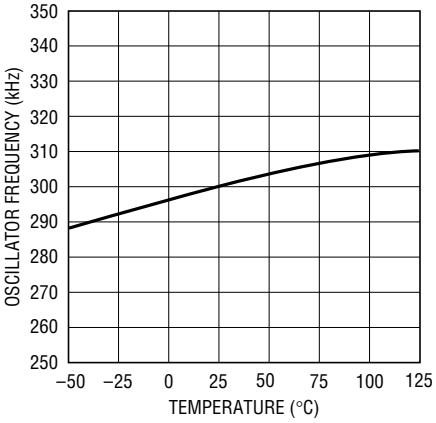
Error Amplifier Open-Loop DC Gain vs Temperature



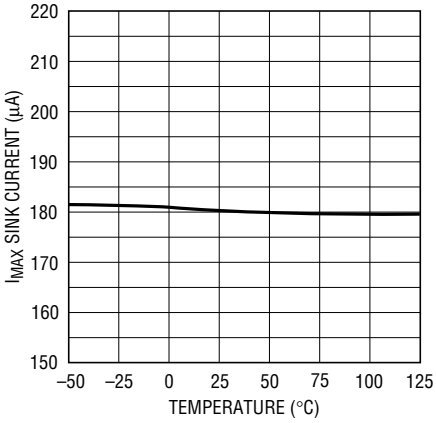
1553 G09

TYPICAL PERFORMANCE CHARACTERISTICS

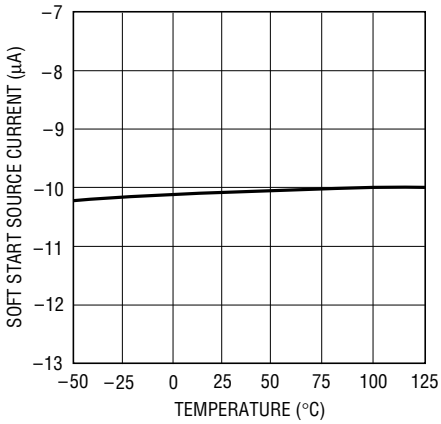
Oscillator Frequency vs Temperature



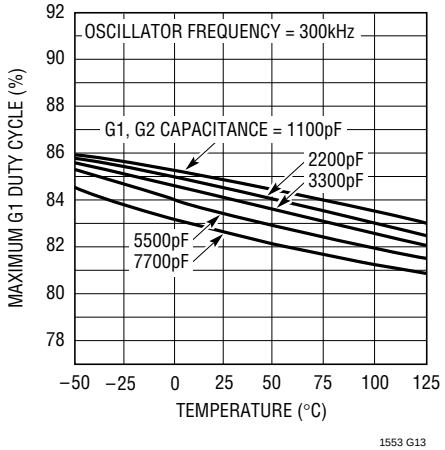
I_{MAX} Sink Current vs Temperature



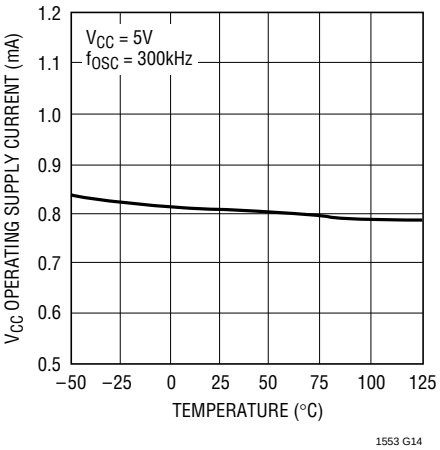
Soft Start Source Current vs Temperature



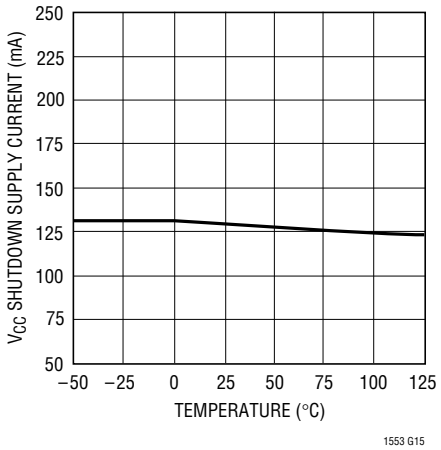
Maximum G1 Duty Cycle vs Temperature



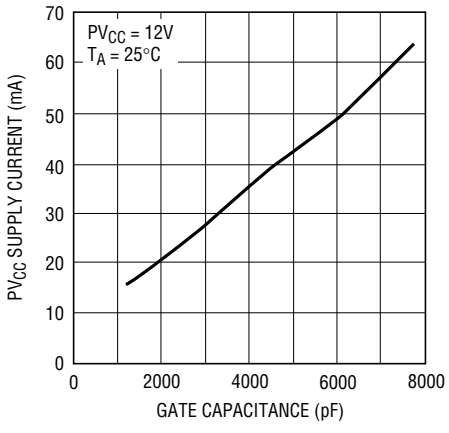
V_{CC} Operating Supply Current vs Temperature



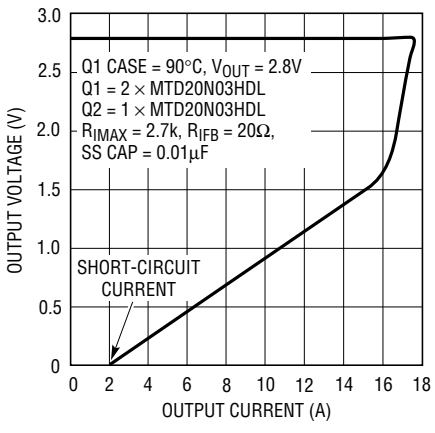
V_{CC} Shutdown Supply Current vs Temperature



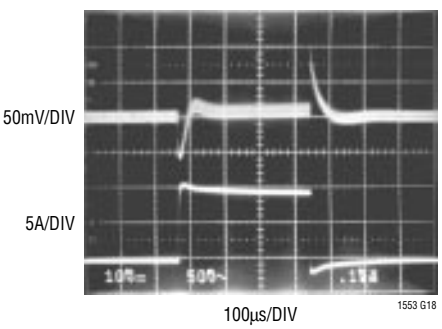
PV_{CC} Supply Current vs Gate Capacitance



Output Over Current Protection



Transient Response



PIN FUNCTIONS

G2 (Pin 1): Gate Drive for the Lower N-Channel MOSFET, Q2. This output will swing from PV_{CC} to GND. It will always be low when G1 is high or when the output is disabled. To prevent undershoot during a soft start cycle, G2 is held low until G1 first goes high.

PV_{CC} (Pin 2): Power Supply for G1 and G2. PV_{CC} must be connected to a potential of at least V_{IN} + $V_{GS(ON)Q1}$. If V_{IN} = 5V, PV_{CC} can be generated using a simple charge pump connected to the switching node between Q1 and Q2 (see Figure 7), or it can be connected to an auxiliary 12V supply if one exists. For applications where V_{IN} = 12V, PV_{CC} can be generated using a 17V charge pump (see Figure 9).

GND (Pin 3): Power Ground. GND should be connected to a low impedance ground plane in close proximity to the source of Q2.

SGND (Pin 4): Signal Ground. SGND is connected to the low power internal circuitry and should be connected to the negative terminal of the output capacitor where it returns to the ground plane. GND and SGND should be shorted right at the LTC1553.

V_{CC} (Pin 5): Power Supply. Power for the internal low power circuity. V_{CC} should be wired separately from the drain of Q1 if they share the same supply. A 10µF bypass capacitor is recommended from this pin to SGND.

SENSE (Pin 6): Output Voltage Pin. Connect to the positive terminal of the output capacitor. There is an internal 120k resistor connected from this pin to SGND. SENSE is a very sensitive pin; for optimum performance, connect an external 0.1µF capacitor from this pin to SGND. By connecting a small external resistor between the output capacitor and the SENSE pin, the initial output voltage can be raised slightly. Since the internal divider has a nominal impedance of 120kΩ, a 1200Ω series resistor will raise the nominal output voltage by 1%. If an external resistor is used, the value of the 0.1µF capacitor on the SENSE pin must be greatly reduced or loop phase margin will suffer. Set a time constant for the RC combination of approximately 0.1µs. So, for example, with a 1200Ω resistor, set C = 83pF. Use a standard 100pF capacitor.

I_{MAX} (Pin 7): Current Limit Threshold. Current limit is set by the voltage drop across an external resistor connected between the drain of Q1 and I_{MAX}. There is a 180µA internal pull-down at I_{MAX}.

I_{FB} (Pin 8): Current Limit Sense Pin. Connect to the switching node between the source of Q1 and the drain of Q2. If I_{FB} drops below I_{MAX} when G1 is on, the LTC1553 will go into current limit. The current limit circuit can be disabled by floating I_{MAX} and shorting I_{FB} to V_{CC} through an external 10k resistor. For V_{IN} = 12V, a 15V Zener diode from I_{FB} to GND is recommended to prevent the voltage spike at I_{FB} from exceeding the maximum voltage rating.

SS (Pin 9): Soft Start. Connect to an external capacitor to implement a soft start function. During moderate overload conditions, the soft start capacitor will be discharged slowly in order to reduce the duty cycle. In hard current limit, the soft start capacitor will be forced low immediately and the LTC1553 will rerun a complete soft start cycle. C_{SS} must be selected such that during power-up the current through Q1 will not exceed the current limit value.

COMP (Pin 10): External Compensation. The COMP pin is connected directly to the output of the error amplifier and the input of the PWM comparator. An RC + C network is used at this node to compensate the feedback loop to provide optimum transient response.

$\overline{OT}$ (Pin 11): Over-Temperature Fault. $\overline{OT}$ is an open-drain output and will be pulled low if OUTEN is less than 2V. If OUTEN = 0, $\overline{OT}$ pulls low.

$\overline{FAULT}$ (Pin 12): Overvoltage Fault. $\overline{FAULT}$ is an open-drain output. If V_{OUT} reaches 15% above the nominal output voltage, $\overline{FAULT}$ will go low and G1 and G2 will be disabled. Once triggered, the LTC1553 will remain in this state until the power supply is recycled or the OUTEN pin is toggled. If OUTEN = 0, $\overline{FAULT}$ floats or is pulled high by an external resistor.

PWRGD (Pin 13): Power Good. This is an open-drain signal to indicate validity of output voltage. A high indicates that the output has settled to within ±5% of the rated output for more than 1ms. PWRGD will go low if the output is out of regulation for more than 500µs. If OUTEN = 0, PWRGD pulls low.