19-3016; Rev 1; 1/04

MAXIM

Quad Low-Power, 500Mbps ATE Driver/Comparator

MAX9965/MAX9966

General Description

The MAX9965/MAX9966 four-channel, low-power, high-speed pin electronics driver and comparator ICs include for each channel a three-level pin driver, comparator, and variable clamps. The MAX9965/MAX9966 are similar to the MAX9963/MAX9964, but with even lower window comparator dispersion for enhanced accuracy. The driver features a wide voltage range and high-speed operation, includes high-Z and active termination (3rd-level drive) modes, and is highly linear even at low-voltage swings. The dual bipolar-input comparator provides very low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed DUT waveforms when the device is configured as a high-impedance receiver. High-speed, differential control inputs compatible with ECL, LVPECL, LVDS, and GTL levels are provided for each channel. ECL/LVPECL or flexible open-collector outputs are available for the comparators.

The A-grade version provides tight matching of gain and offset for the driver and comparator, allowing reference levels to be shared across multiple channels in cost-sensitive systems. For system designs that incorporate independent reference levels for each channel, the B-grade version is available at reduced cost.

Optional internal resistors at the high-speed inputs provide differential termination of LVDS inputs, while optional internal resistors provide the pullup voltage and source termination for open-collector comparator outputs. These features significantly reduce the discrete component count on the circuit board.

The MAX9965/MAX9966 operating range is -1.5V to +6.5V, with power dissipation of only 975mW per channel.

These devices are available in a 100-pin, 14mm x 14mm body, 0.5mm pitch TQFP with an exposed 8mm x 8mm die pad on the top (MAX9965) or bottom (MAX9966) of the package for efficient heat removal. The MAX9965/MAX9966 are specified to operate with an internal die temperature of +60°C to +100°C, and feature a die temperature monitor output.

Applications

Memory Testers

Low-Cost Mixed-Signal/System-on-Chip Testers

Structural Testers

Pattern/Data Generators

Features

- ♦ Small Footprint: Four Channels in 0.4in^2
- ♦ Low Power Dissipation: 975mW/Channel (typ)
- ♦ High Speed: 500Mbps at $3V_{P-P}$
- ♦ Very Low Timing Dispersion
- ♦ Wide Operating Range: -1.5V to +6.5V
- ♦ Active Termination (3rd-Level Drive)
- ♦ Low-Leakage Mode: 15nA Maximum
- ♦ Integrated Clamps
- ♦ Interface Easily with Most Logic Families
- ♦ Digitally Programmable Slew Rate
- ♦ Internal Logic Termination Resistors
- ♦ Low Gain and Offset Error

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9965ADCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965AKCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965AGCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965AHCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965AJCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965BDCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965BKCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965BGCCQ	0°C to +70°C	100 TQFP-EPR***
MAX9965BHCCQ*	0°C to +70°C	100 TQFP-EPR***
MAX9965BJCCQ	0°C to +70°C	100 TQFP-EPR***
MAX9966ADCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966AKCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966AGCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966AHCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966AJCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966BDCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966BKCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966BGCCQ	0°C to +70°C	100 TQFP-EP**
MAX9966BHCCQ*	0°C to +70°C	100 TQFP-EP**
MAX9966BJCCQ*	0°C to +70°C	100 TQFP-EP**

*Future product—contact factory for availability.
**EP = Exposed pad.
***EPR = Exposed pad reversed.

Pin Configurations and Selector Guide appear at end of data sheet.

Quad Low-Power, 500Mbps ATE Driver/Comparator

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +11.5V
V_{EE} to GND ....-7.0V to +0.3V
All Other Pins ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
V_{CC} - V_{EE} ....-0.3V to +18V
DUT_ to GND ....-2.5V to +7.5V
DATA_, NDATA_, RCV_, NRCV_ to GND ....-2.5 to +5.0V
DATA_ to NDATA_ ....±1.5V
RCV_ to NRCV_ ....±1.5V
$V_{CCO\_\ \_}$ to GND ....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$ to GND ....-1.0V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_ to GND ....-2.5V to +7.5V
CPHV_ to GND ....-2.5V to +8.5V
CPLV_ to GND ....-3.5V to +7.5V
DHV_ to DLV_ ....±10V
DHV_ to DTV_ ....±10V
DLV_ to DTV_ ....±10V
CHV_ or CLV_ to DUT_ ....±10V
CH_, NCH_, CL_, NCL_ to GND ....-2.5V to +5V
Current into DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_ ....±10mA
Current into TEMP ....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V ....Continuous
Power Dissipation (T_A = +70°C)
MAX9965__CCQ (derate 167mW/°C above +70°C) 13.3W*
MAX9966__CCQ (derate 47.6mW/°C above +70°C) 3.8W*
Storage Temperature Range ....-65°C to +150°C
Junction Temperature ....+125°C
Lead Temperature (soldering, 10s) ....+300°C

**Dissipation wattage values are based on still air with no heat sink for the MAX9965 and slug soldered to board copper for the MAX9966. Actual maximum power dissipation is a function of users' heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_\ \_}$ = 2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-6.5	-5.25	-4.5	V
Positive Supply	I_{CC}	(Note 2)		200	225	mA
Negative Supply	I_{EE}	(Note 2)		-370	-425	mA
Power Dissipation	P_D	(Notes 2, 3)		3.9	4.5	W
DUT_ CHARACTERISTICS						
Operating Voltage Range Max	V_{DUT}	(Note 4)	-1.5		+6.5	V
Leakage Current in High-Z Mode	I_{DUT}	LLEAK = 0, 0 ≤ $V_{DUT\_}$ ≤ 3V			±2	µA
		LLEAK = 0, $V_{DUT\_}$ = -1.5V, 6.5V			±5	
Leakage Current in Low-Leakage Mode	I_{DUT}	LLEAK = 1, 0 ≤ $V_{DUT\_}$ ≤ 3V, T_J < +90°C			±15	nA
		LLEAK = 1, $V_{DUT\_}$ = -1.5V, T_J < +90°C			±30	
		LLEAK = 1, $V_{DUT\_}$ = 6.5V, T_J < +90°C			±30	
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		3		pF
		Driver in high-Z mode		5		
Low-Leakage Enable Time		(Notes 5, 7)		20		µs
Low-Leakage Disable Time		(Notes 6, 7)		20		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Note 7)		10		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_\ \_}$ = 2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling Time		To 5mV		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)						
Input High Voltage	V_{IH}		-1.6		+3.5	V
Input Low Voltage	V_{IL}		-2.0		+3.1	V
Differential Input Voltage	V_{DIFF}		±0.15		±1.0	V
Input Resistor		MAX996_ _GCCQ, MAX996_ _JCCQ, between signal and complement	96		104	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, $\overline{RST}$, SCLK, DIN)						
Input High Voltage	V_{IH}		1.6		3.5	V
Input Low Voltage	V_{IL}		-0.1		+0.9	V
SERIAL INTERFACE TIMING (Figure 5)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse Width High	t_{CH}		8			ns
SCLK Pulse Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		3.5			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		3.5			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}		20			ns
TEMPERATURE MONITOR (TEMP)						
Nominal Voltage		T_J = +70°C, R_L ≥ 10MΩ		3.43		V
Temperature Coefficient				+10		mV/°C
Output Resistance				15		kΩ
DRIVERS (Note 8)						
DC OUTPUT CHARACTERISTICS (R_L ≥ 10MΩ)						
DHV_, DLV_, DTV_, Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$= 3V, $V_{DTV\_}$= 1.5V, $V_{DLV\_}$= 0; MAX996_B			±100	mV
DHV_, DLV_, DTV_, Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, $V_{DTV\_}$ at 0 and 4.5V; MAX996_B	0.96		1.001	V/V
DHV_, DLV_, DTV_, Output Voltage Temperature Coefficient		Includes both gain and offset temperature effects		±75		µV/°C
Linearity Error		0V ≤ $V_{DUT\_}$≤ 3V (Note 9)			±5	mV
		Full range (Notes 9, 10)			±15	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_\ \_}$ = 2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 200mV, 6.5V			±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = -1.5V, 4.8V			±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = -1.5V, +6.5V			±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = 0, $V_{DHV\_}$ =1.6V, 3V			±3	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 1.4V			±3	mV
DHV_, DLV_, DTV_ DC Power-Supply Rejection Ratio	PSRR	V_{CC} and V_{EE} independently set to their min/max values	40			dB
Maximum DC Drive Current	$I_{DUT\_}$		±60		±120	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 11)	49	50	51	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1.0mA to ±40mA		1	2.5	Ω
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)						
Drive Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		30		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		40		
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		50		
Term Mode Overshoot		(Note 12)		0		mV
Settling Time to Within 25mV		3V step (Note 13)		10		ns
Settling Time to Within 5mV		3V step (Note 13)		20		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 14)						
Prop Delay, Data to Output	t_{PDD}			2	2.75	ns
Prop Delay Match, T_{LH} vs. T_{HL}		$3V_{P-P}$		±50		ps
Prop Delay Match, Drivers Within Package		(Note 15)		40		ps
Prop Delay Temperature Coefficient				+3		ps/°C
Prop Delay Change vs. Pulse Width		$3V_{P-P}$, 40MHz, 2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width		±60		ps
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		85		ps
Prop Delay, Drive to High-Z	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		2.9		ns
Prop Delay, High-Z to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0		2.9		ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.3		ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V		2.0		ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	0.2 V_{P-P}, 20% to 80%		330		ps
		1 V_{P-P}, 10% to 90%	500	670	800	
		3 V_{P-P}, 10% to 90%	1.1	1.3	1.6	ns
		5 V_{P-P}, 10% to 90%		2.0		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_\_}$ = 2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SC1 = 0, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), 3V_{P-P}, 20% to 80%			75		%
SC1 = 1, SC0 = 0 Slew Rate		Percent of full speed (SC0 = SC1 = 0), 3V_{P-P}, 20% to 80%			50		%
SC1 = 1, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), 3V_{P-P}, 20% to 80%			25		%
Minimum Pulse Width (Note 16)		0.2V_{P-P}, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0			0.65		ns
		1V_{P-P}, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0			1.0		
		3V_{P-P}, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0			2.0		
		5V_{P-P}, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0			2.9		
Data Rate (Note 17)		0.2V_{P-P}, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0			1700		Mbps
		1V_{P-P}, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0			1000		
		3V_{P-P}, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0			500		
		5V_{P-P}, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0			350		
Dynamic Crosstalk		(Note 18)			20		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90% (Note 19)			1.6		ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90% (Note 19)			0.7		ns
COMPARATORS							
DC CHARACTERISTICS							
Input Voltage Range	V_{IN}	(Note 4)		-1.5		+6.5	V
Differential Input Voltage	V_{DIFF}			±8			V
Hysteresis	V_{HYST}				0		mV
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V	MAX996_B			±100	mV
Input Offset Voltage Temperature Coefficient					±50		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = -1.5V, 6.5V (Note 20)		50	55		dB
Linearity Error		$V_{DUT\_}$ = 1.5V (Note 9)			±1	±5	mV
		$V_{DUT\_}$ = -1.5V and 6.5V (Note 9)			±1	±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = -1.5V, 6.5V (Note 21)		50	66		dB
AC CHARACTERISTICS (Note 22)							
Minimum Pulse Width	$t_{PW(MIN)}$	(Note 23)	MAX996_ _GCCQ		0.6		ns
			MAX996_ _HCCQ, MAX996_ _JCCQ		0.9		
Prop Delay	t_{PDL}				1.2	2.0	ns
Prop Delay Temperature Coefficient					2.6		ps/°C

Quad Low-Power, 500Mbps ATE Driver/Comparator

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_\_}$ = 2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prop Delay Match, High/Low vs. Low/High					±40		ps
Prop Delay Match, Comparators Within Package		(Note 15)			40		ps
Prop Delay Dispersion vs. Common-Mode Input		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4, 6.4V (Note 24)			±20		ps
Prop Delay Dispersion vs. Overdrive		50mV to 500mV			60		ps
Prop Delay Dispersion vs. Pulse Width		2.0ns to 23ns pulse width, relative to 12.5ns pulse width	MAX996_ _GCCQ		±25		ps
			MAX996_ _HCCQ, MAX996_ _JCCQ		±45		
Prop Delay Dispersion vs. Slew Rate		0.5V/ns to 6.5V/ns slew rate, peak-to-peak variation			50		ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 1.0ns 10% to 90%, relative to timing at 50% point	Term mode		50		ps
			High-Z mode		250		
OPEN-COLLECTOR LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_: MAX996_ _GCCQ)							
$V_{CCO\_\_}$ Voltage Range	$V_{VCCO\_\_}$			0		3.5	V
Output Low Voltage Compliance		Set by I_{OUT}, R_{TERM}, and $V_{CCO\_\_}$			-0.5		V
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0		$V_{CCO\_\_}$ - 0.1	$V_{CCO\_\_}$ - 0.02		V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0			$V_{CCO\_\_}$ - 0.4		V
Output Voltage Swing				0.350	0.380	0.442	V
Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_\_}$ to CH_, NCH_, CL_, NCL_		48		52	Ω
Differential Rise Time	t_R	20% to 80%			200		ps
Differential Fall Time	t_F	20% to- 80%			200		ps
OPEN-EMITTER LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_: MAX996_ _JCCQ)							
$V_{CCO\_\_}$ Voltage Range	$V_{CCO\_\_}$			-0.1		3.5	V
$V_{CCO\_\_}$ Supply Current	$I_{VCCO\_\_}$	All outputs 50Ω to ($V_{VCCO\_\_}$ - 2V)			330		mA
Output High Voltage	V_{OH}	50Ω to ($V_{VCCO\_\_}$ - 2V)		$V_{CCO\_\_}$ - 1	$V_{CCO\_\_}$ - 0.88		V
Output Low Voltage	V_{OL}	50Ω to ($V_{VCCO\_\_}$ - 2V)			$V_{CCO\_\_}$ - 1.73	$V_{CCO\_\_}$ - 1.6	V
Output Voltage Swing		50Ω to ($V_{VCCO\_\_}$ - 2V)		800	850	900	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, $V_{CCO\_ \_}$ = 2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Rise Time	t_R	20% to 80%		500		ps
Differential Fall Time	t_F	20% to 80%		500		ps
CLAMPS						
High Clamp Input Voltage Range	$V_{CPH\_}$		-0.3		+7.5	V
Low Clamp Input Voltage Range	$V_{CPL\_}$		-2.5		+5.3	V
Clamp Offset Voltage	V_{OS}	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 1.5V			±100	mV
		At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 1.5V			±100	
Offset Voltage Temperature Coefficient				±0.5		mV/°C
Clamp Power-Supply Rejection	PSRR	V_{CC} and V_{EE} independently set to their min and max values, $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0	40			dB
		V_{CC} and V_{EE} independently set to their min and max values, $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0	40			
Voltage Gain	A_V		0.96		1.00	V/V
Voltage Gain Temperature Coefficient				-100		ppm/°C
Clamp Linearity		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = -0.3V to 6.5V		±10		mV
		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to 5.3V		±10		
Short-Circuit Output Current	I_{DUT}	$V_{CPHV\_}$ = 0, $V_{CPLV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V	50		95	mA
		$V_{CPLV\_}$ = 5V, $V_{CPHV\_}$ = 6.5V, $V_{DUT\_}$ = -1.5V	-95		-50	
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, I_{DUT} = -5mA and -15mA	50		55	Ω
		$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, I_{DUT} = 5mA and 15mA	50		55	

Note 1: All min and max limits are 100% tested in production. Tests are performed at worst-case supply voltages where applicable.
Note 2: Total for quad device at worst-case setting. R_L ≥ 10MΩ. The applicable supply currents are measured with typical supply voltages.
Note 3: Does not include internal dissipation of the comparator outputs. With output loads of 50Ω to ($V_{VCCO\_ \_}$ - 2V), this adds 240mW typical to the total chip power (MAX996_ _HCCQ, MAX996_ _JCCQ).
Note 4: Provided that the Absolute Maximum Ratings are not exceeded, externally forced voltages may exceed this range.
Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.
Note 6: Transition time from LLEAK being deasserted to output returning to normal operating mode.
Note 7: Based on simulation results only.
Note 8: With the exception of Offset and Gain/CMRR tests, reference input values are calibrated for offset and gain.
Note 9: Relative to straight line between 0 and 3V.
Note 10: Full ranges are -1.3V ≤ $V_{DHV\_}$ ≤ 6.5V, -1.5V ≤ $V_{DTV\_}$ ≤ 6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ 6.3V.
Note 11: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 40Ω to 50Ω range.
Note 12: $V_{DTV\_}$ = 1.5V, R_S = 50Ω. External signal driven into T-line is a 0 to 3V edge with 1.2ns rise time (10% to 90%). Measurement is made using the comparator.
Note 13: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 14: Prop delays are measured from the crossing point of the differential input signals to the 50% point of expected output swing. Rise time of the differential inputs DATA_ and RCV_ is 250ps (10% to 90%).

Note 15: Rising edge to rising edge or falling edge to falling edge.

Note 16: Specified amplitude is programmed. At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 17: Specified amplitude is programmed. Maximum data rate specified in transitions per second. A square wave that reaches at least 95% of its programmed amplitude may be generated at one-half of this frequency.

Note 18: Crosstalk from any driver to the other three channels. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channels are in term mode with $V_{DTV\_}$ = 1.5V.

Note 19: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_} < V_{DTV\_} < V_{DHV\_}$. If $V_{DTV\_} < V_{DLV\_}$ or $V_{DTV\_} > V_{DHV\_}$, switching speed is degraded by approximately a factor of 3.

Note 20: Change in Offset Voltage over input range.

Note 21: Change in Offset Voltage with power supplies independently set to their minimum and maximum values.

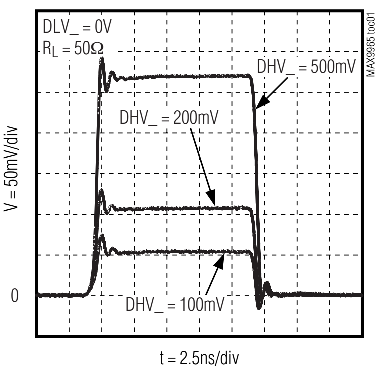
Note 22: Unless otherwise noted, all Prop Delays are measured at 40MHz, $V_{DUT\_}$ = 0 to 2V, $V_{CHV\_} = V_{CLV\_}$ = 1V, slew rate = 2V/ns, Z_S = 50Ω, driver in Term Mode with $V_{DTV\_}$ = 0V. Comparator outputs are terminated with 50Ω to GND at scope input with $V_{CCO\_\_}$ = 2V. Open-collector outputs are also terminated (internally or externally) with R_{TERM} = 50Ω to $V_{CCO\_\_}$. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 23: $V_{DUT\_}$ = 0 to 1V, $V_{CHV\_} = V_{CLV\_}$ = 0.5V. At this pulse width, the output reaches at least 90% of its DC Voltage swing. The pulse width is measured at the crossing points of the differential outputs.

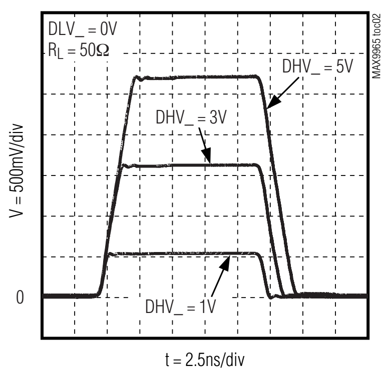
Note 24: Relative to propagation delay at $V_{CHV\_} = V_{CLV\_}$ = 1.5V. $V_{DUT\_}$ = $200mV_{P-P}$. Overdrive = 100mV.

Typical Operating Characteristics

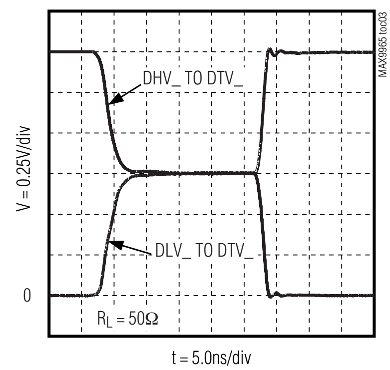
DRIVER SMALL-SIGNAL RESPONSE



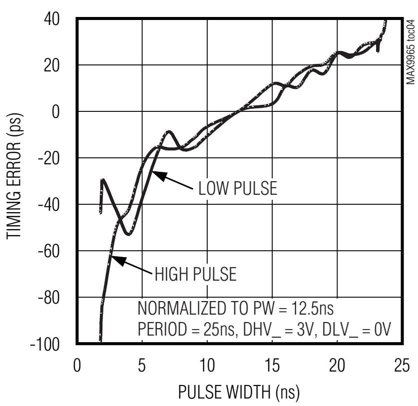
DRIVER LARGE-SIGNAL RESPONSE



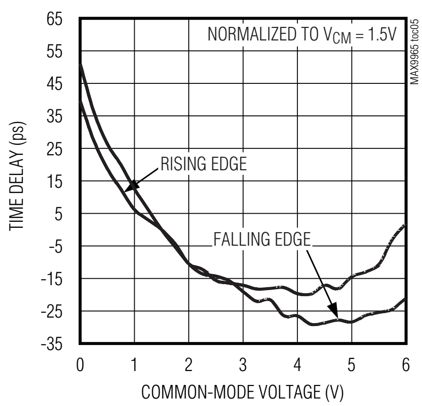
DRIVE TO TERM TRANSITION



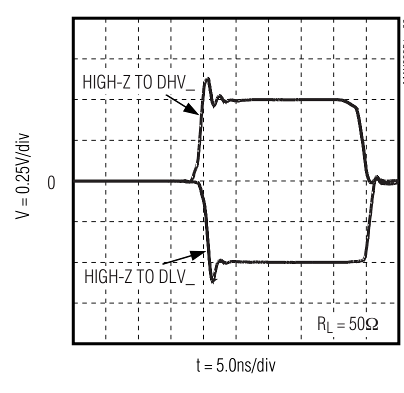
DRIVER TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



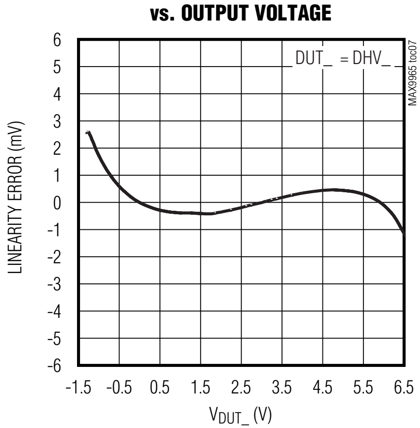
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



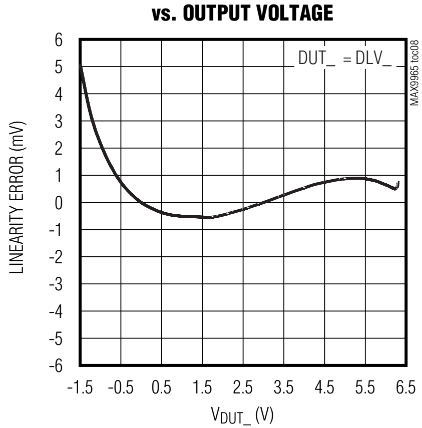
HIGH-Z TO DRIVE TRANSITION



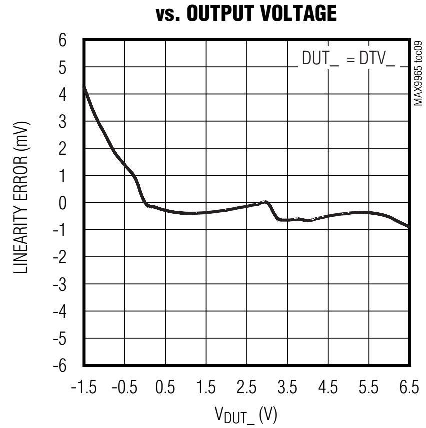
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



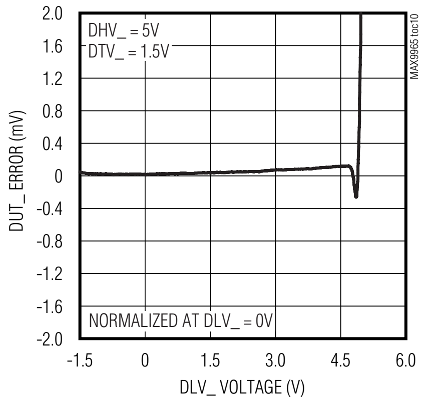
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



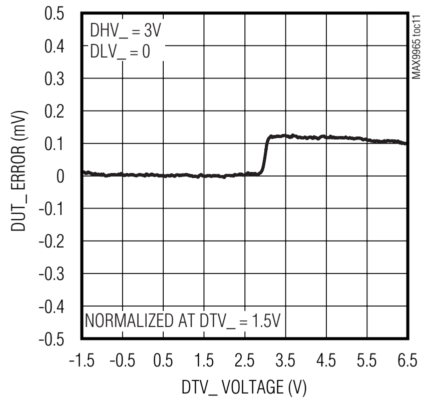
Quad Low-Power, 500Mbps ATE Driver/Comparator

Typical Operating Characteristics (continued)

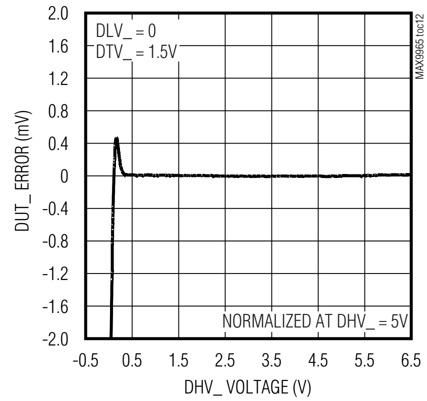
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



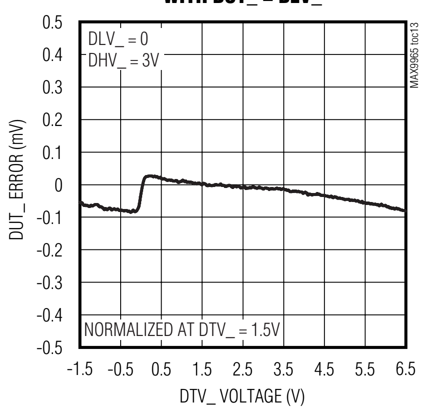
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



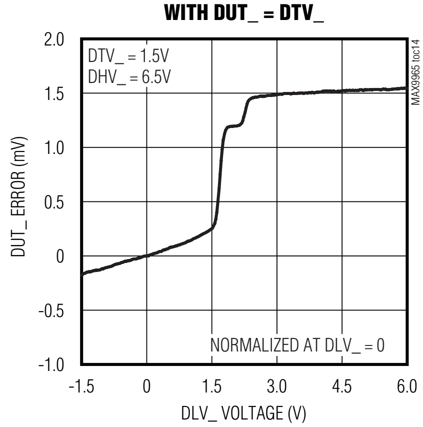
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



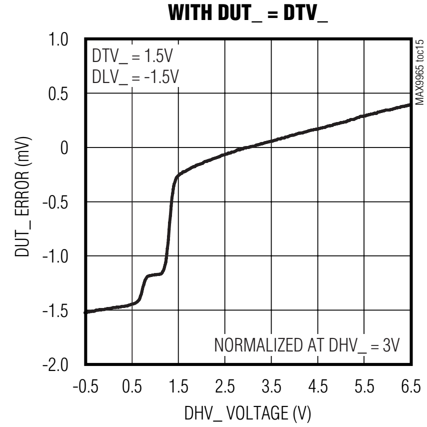
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



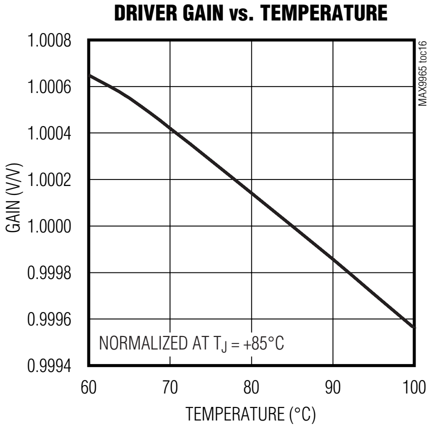
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



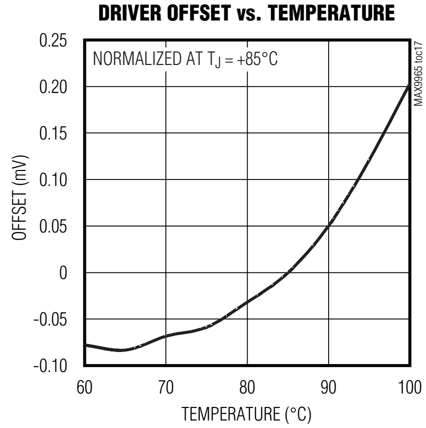
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



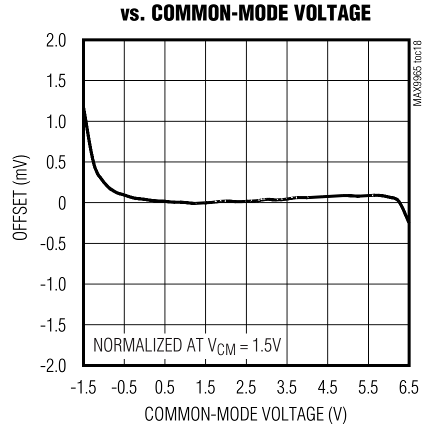
DRIVER GAIN vs. TEMPERATURE



DRIVER OFFSET vs. TEMPERATURE

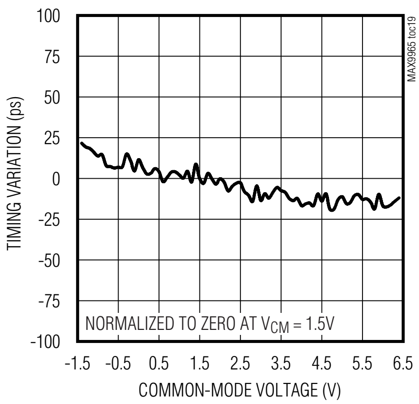


COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE

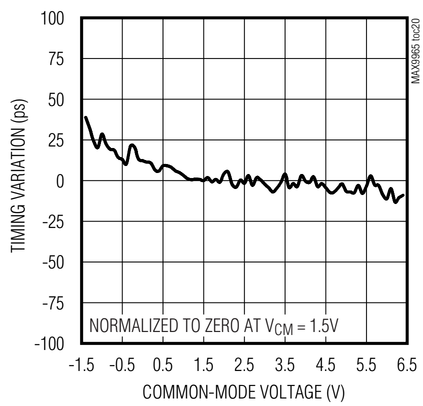


Typical Operating Characteristics (continued)

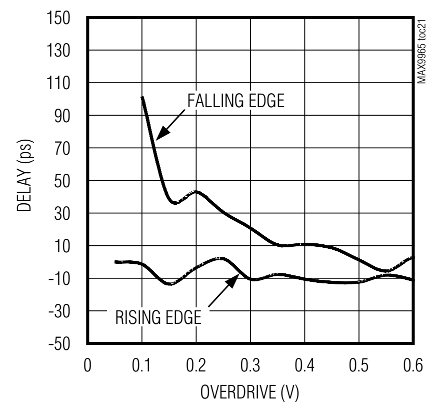
COMPARATOR RISING EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



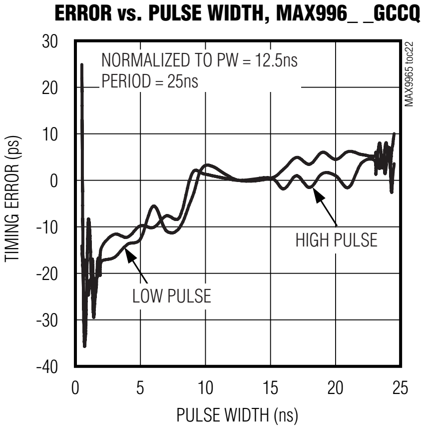
COMPARATOR FALLING EDGE TIMING VARIATION vs. COMMON-MODE VOLTAGE



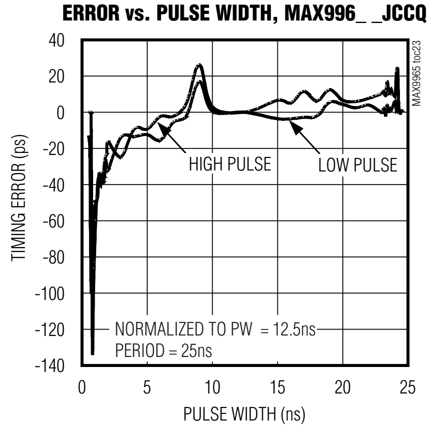
COMPARATOR TIMING VARIATION vs. OVERDRIVE



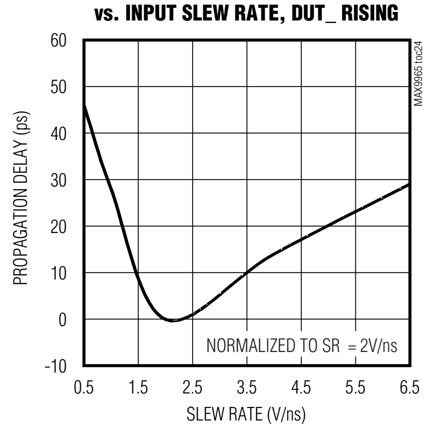
COMPARATOR TRAILING EDGE TIMING ERROR vs. PULSE WIDTH, MAX996_ _GCCQ



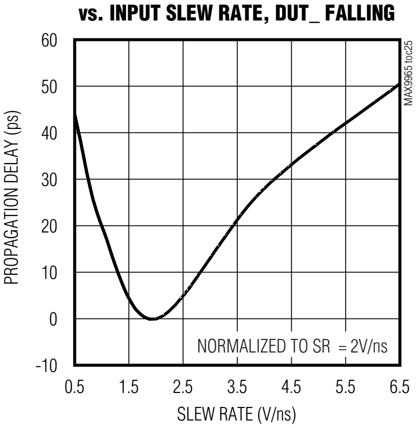
COMPARATOR TRAILING EDGE TIMING ERROR vs. PULSE WIDTH, MAX996_ _JCCQ



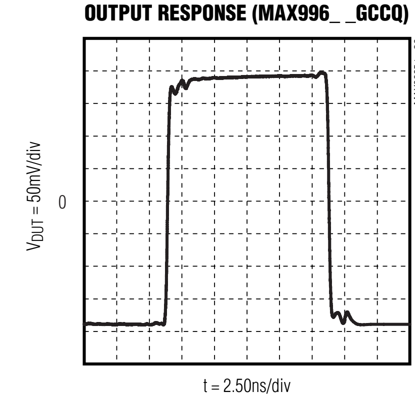
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ RISING



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_ FALLING

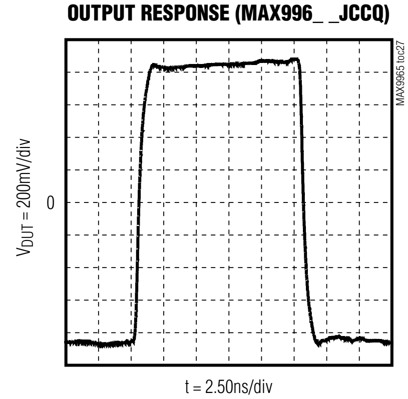


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE (MAX996_ _GCCQ)



V_{DUT} = 0 TO 3V PULSE, CHV_ = CLV_ = 1.5V,
EXTERNAL LOAD = 50Ω

COMPARATOR DIFFERENTIAL OUTPUT RESPONSE (MAX996_ _JCCQ)

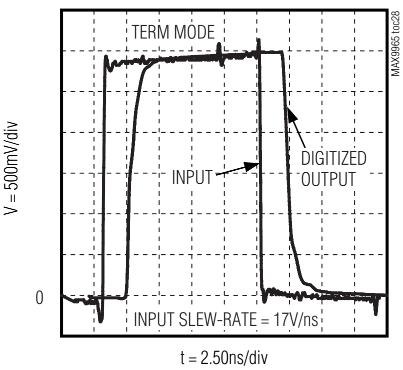


V_{DUT} = 0 TO 3V PULSE, CHV_ = CLV_ = 1.5V,
EXTERNAL LOAD = 50Ω

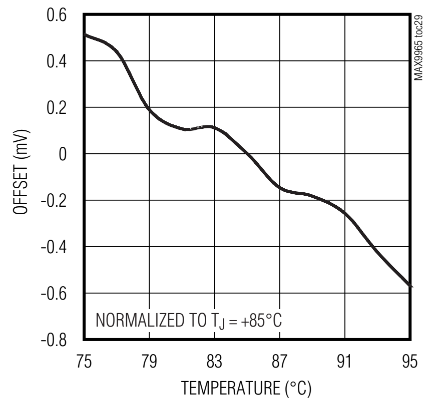
Quad Low-Power, 500Mbps ATE Driver/Comparator

Typical Operating Characteristics (continued)

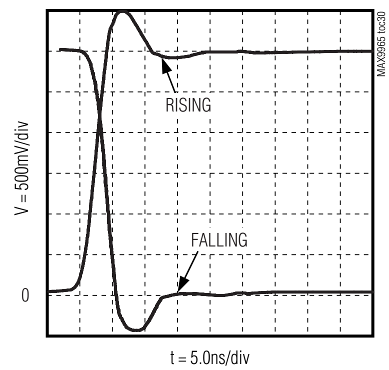
COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE



COMPARATOR OFFSET vs. TEMPERATURE

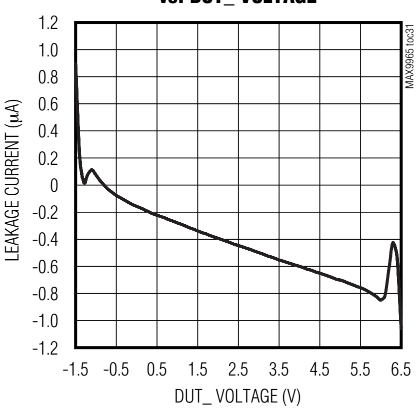


CLAMP RESPONSE

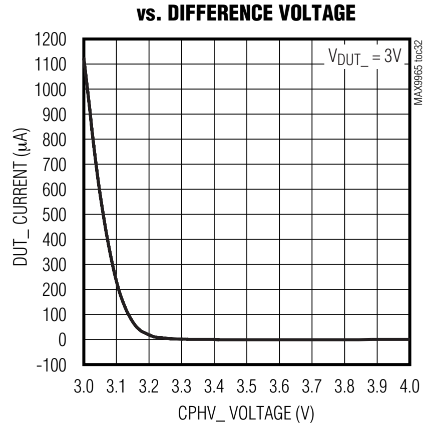


V_{DUT} = 0V TO 3V SQUARE WAVE, R_S = 25Ω
CPLV_ = -0.1V, CPHV_ = +3.1V

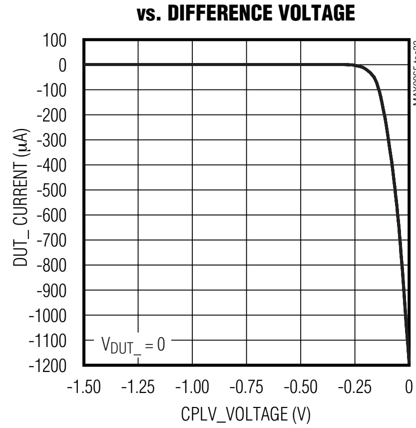
HIGH-Z LEAKAGE CURRENT vs. DUT_ VOLTAGE



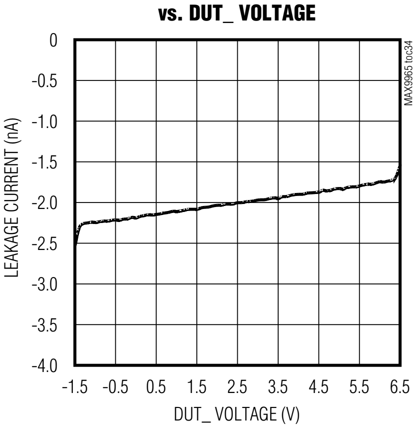
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



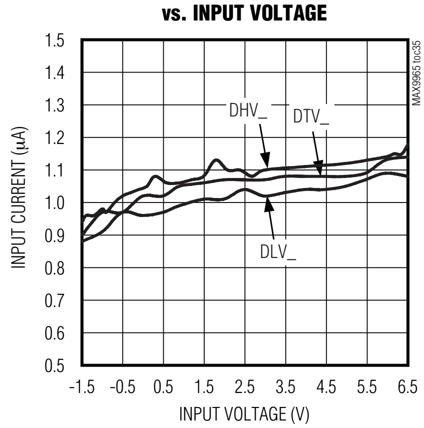
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



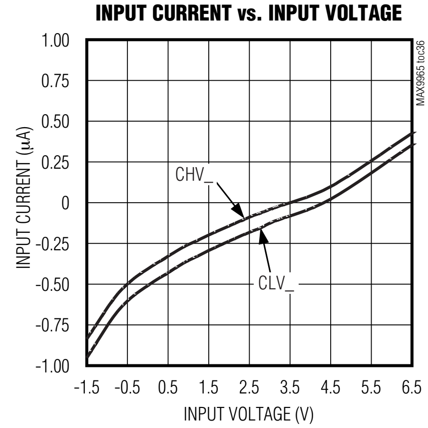
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



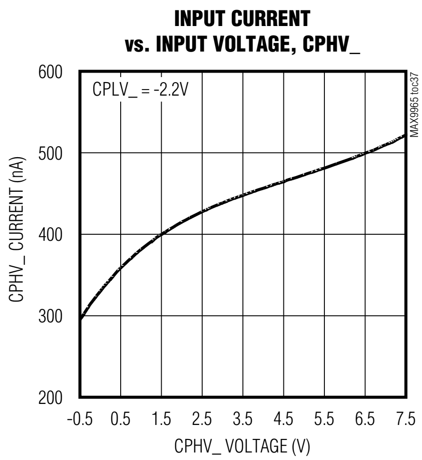
DRIVER REFERENCE CURRENT vs. INPUT VOLTAGE

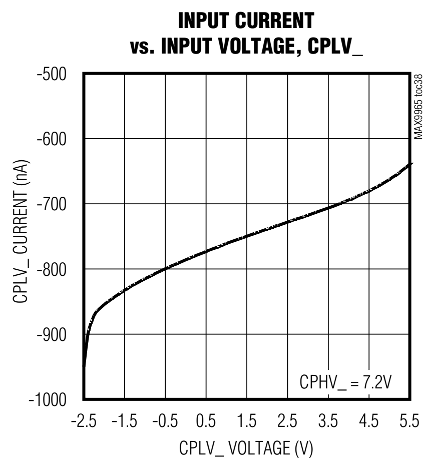


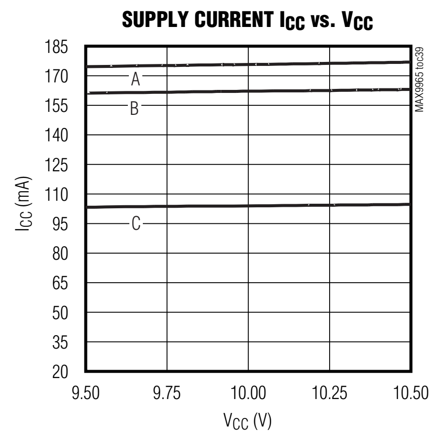
COMPARATOR REFERENCE INPUT CURRENT vs. INPUT VOLTAGE



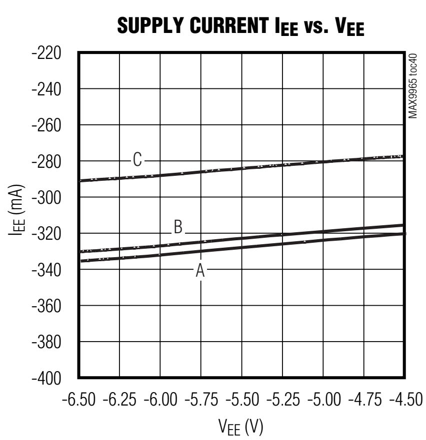
Typical Operating Characteristics (continued)



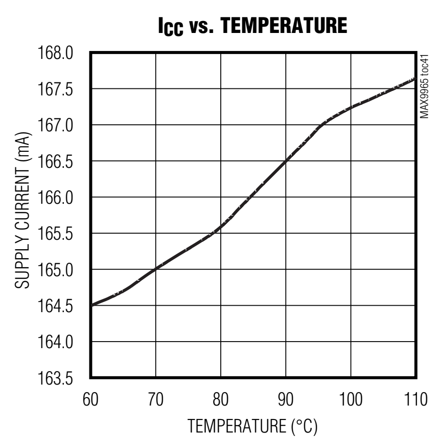




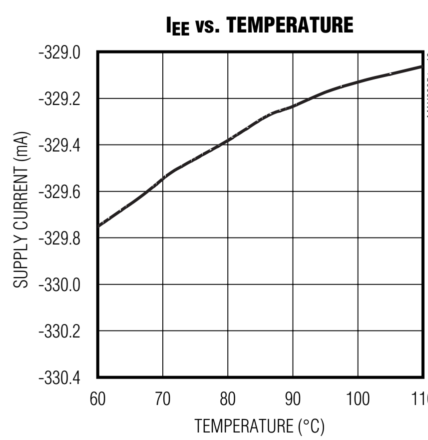
A: DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV_ = -2.2V
B: SAME AS A EXCEPT DUT_ = HIGH-Z
C: SAME AS B EXCEPT DUT_ = LOW LEAK



A: DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV_ = -2.2V
B: SAME AS A EXCEPT DUT_ = HIGH-Z
C: SAME AS B EXCEPT DUT_ = LOW LEAK



DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV = -2.2V, V_{CC} = 9.75V, V_{EE} = -5.25V



DUT_ = DTV_ = 1.5V, DHV_ = 3V, DLV_ = 0, CHV_ = CLV_ = 0, CPHV_ = 7.2V, CPLV = -2.2V, V_{CC} = 9.75V, V_{EE} = -5.25V

Quad Low-Power, 500Mbps ATE Driver/Comparator

Pin Description

PIN		NAME	FUNCTION
MAX9965	MAX9966		
1	25	$V_{CCO}34$	Channel 3/4 Collector Voltage Input. For open-collector outputs, this is the pullup voltage for the internal termination resistors. For open-emitter outputs, this is the collector voltage of the output transistors. Not internally connected on open-collector versions without internal termination resistors. $V_{CCO}34$ services both channel 3 and channel 4.
2	24	DATA4	Channel 4 Multiplexer Control Inputs. Differential controls DATA4 and NDATA4 select driver 4's input from DHV4 or DLV4. Drive DATA4 above NDATA4 to select DHV4. Drive NDATA4 above DATA4 to select DLV4.
3	23	NDATA4	
4	22	RCV4	Channel 4 Multiplexer Control Inputs. Differential controls RCV4 and NRCV4 place channel 4 into receive mode. Drive RCV4 above NRCV4 to place channel 4 into receive mode. Drive NRCV4 above RCV4 to place channel 4 into drive mode.
5	21	NRCV4	
6	20	DATA3	Channel 3 Multiplexer Control Inputs. Differential controls DATA3 and NDATA3 select driver 3's input from DHV3 or DLV3. Drive DATA3 above NDATA3 to select DHV3. Drive NDATA3 above DATA3 to select DLV3.
7	19	NDATA3	
8	18	RCV3	Channel 3 Multiplexer Control Inputs. Differential controls RCV3 and NRCV3 place channel 3 into receive mode. Drive RCV3 above NRCV3 to place channel 3 into receive mode. Drive NRCV3 above RCV3 to place channel 3 into drive mode.
9	17	NRCV3	
10, 27, 54, 55, 60, 61, 65, 66, 71, 72, 99	16, 27, 54, 55, 60, 61, 65, 66, 71, 72, 99	V_{EE}	Negative Power-Supply Input
11, 28, 51, 56, 62, 64, 70, 75, 98	15, 28, 51, 56, 62, 64, 70, 75, 98	GND	Ground Connection
12	14	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low and asserts low-leakage mode. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.
13	13	$\overline{CS}$	Chip Select Input. Serial port activation input. $\overline{CS}$ is active low.
14	12	SCLK	Serial Clock Input. Clock for serial port.
15	11	DIN	Data Input. Serial port data input.
16, 26, 52, 58, 68, 74, 100	10, 26, 52, 58, 68, 74, 100	V_{CC}	Positive Power-Supply Input
17	9	NRCV2	Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 into receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode.
18	8	RCV2	
19	7	NDATA2	Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2.
20	6	DATA2	
21	5	NRCV1	Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 into receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.
22	4	RCV1	
23	3	NDATA1	Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.
24	2	DATA1	

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9965	MAX9966		
25	1	$V_{CCO}12$	Channel 1/2 Collector Voltage Input. For open-collector outputs, this is the pullup voltage for the internal termination resistors. For open-emitter outputs, this is the collector voltage of the output transistors. Not internally connected on open-collector versions without internal termination resistors. $V_{CCO}12$ services both channel 1 and channel 2.
29	97	NCL2	Channel 2 Low Comparator Output. Differential output of channel 2 low comparator.
30	96	CL2	
31	95	NCH2	Channel 2 High Comparator Output. Differential output of channel 2 high comparator.
32	94	CH2	
33	93	NCL1	Channel 1 Low Comparator Output. Differential output of channel 1 low comparator.
34	92	CL1	
35	91	NCH1	Channel 1 High Comparator Output. Differential output of channel 1 high comparator.
36	90	CH1	
37	89	CPHV2	Channel 2 High Clamp Reference Input
38	88	CPLV2	Channel 2 Low Clamp Reference Input
39	87	DHV2	Channel 2 Driver High Reference Input
40	86	DLV2	Channel 2 Driver Low Reference Input
41	85	DTV2	Channel 2 Driver Termination Reference Input
42	84	CHV2	Channel 2 High Comparator Reference Input
43	83	CLV2	Channel 2 Low Comparator Reference Input
44	82	CPHV1	Channel 1 High Clamp Reference Input
45	81	CPLV1	Channel 1 Low Clamp Reference Input
46	80	DHV1	Channel 1 Driver High Reference Input
47	79	DLV1	Channel 1 Driver Low Reference Input
48	78	DTV1	Channel 1 Driver Termination Reference Input
49	77	CHV1	Channel 1 High Comparator Reference Input
50	76	CLV1	Channel 1 Low Comparator Reference Input
53	73	DUT1	Channel 1 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp.
57, 69	57, 69	N.C.	No Connect. Leave open.
59	67	DUT2	Channel 2 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp.
63	63	TEMP	Temperature Monitor Output

Quad Low-Power, 500Mbps ATE Driver/Comparator

Pin Description (continued)

PIN		NAME	FUNCTION
MAX9965	MAX9966		
67	59	DUT3	Channel 3 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp.
73	53	DUT4	Channel 4 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp.
76	50	CLV4	Channel 4 Low Comparator Reference Input
77	49	CHV4	Channel 4 High Comparator Reference Input
78	48	DTV4	Channel 4 Driver Termination Reference Input
79	47	DLV4	Channel 4 Driver Low Reference Input
80	46	DHV4	Channel 4 Driver High Reference Input
81	45	CPLV4	Channel 4 Low Clamp Reference Input
82	44	CPHV4	Channel 4 High Clamp Reference Input
83	43	CLV3	Channel 3 Low Comparator Reference Input
84	42	CHV3	Channel 3 High Comparator Reference Input
85	41	DTV3	Channel 3 Driver Termination Reference Input
86	40	DLV3	Channel 3 Driver Low Reference Input
87	39	DHV3	Channel 3 Driver High Reference Input
88	38	CPLV3	Channel 3 Low Clamp Reference Input
89	37	CPHV3	Channel 3 High Clamp Reference Input
90	36	CH4	Channel 4 High Comparator Output. Differential outputs of channel 4 high comparator.
91	35	NCH4	
92	34	CL4	Channel 4 Low Comparator Output. Differential outputs of channel 4 low comparator.
93	33	NCL4	
94	32	CH3	Channel 3 High Comparator Output. Differential outputs of channel 3 high comparator.
95	31	NCH3	
96	30	CL3	Channel 3 Low Comparator Output. Differential outputs of channel 3 low comparator.
97	29	NCL3	

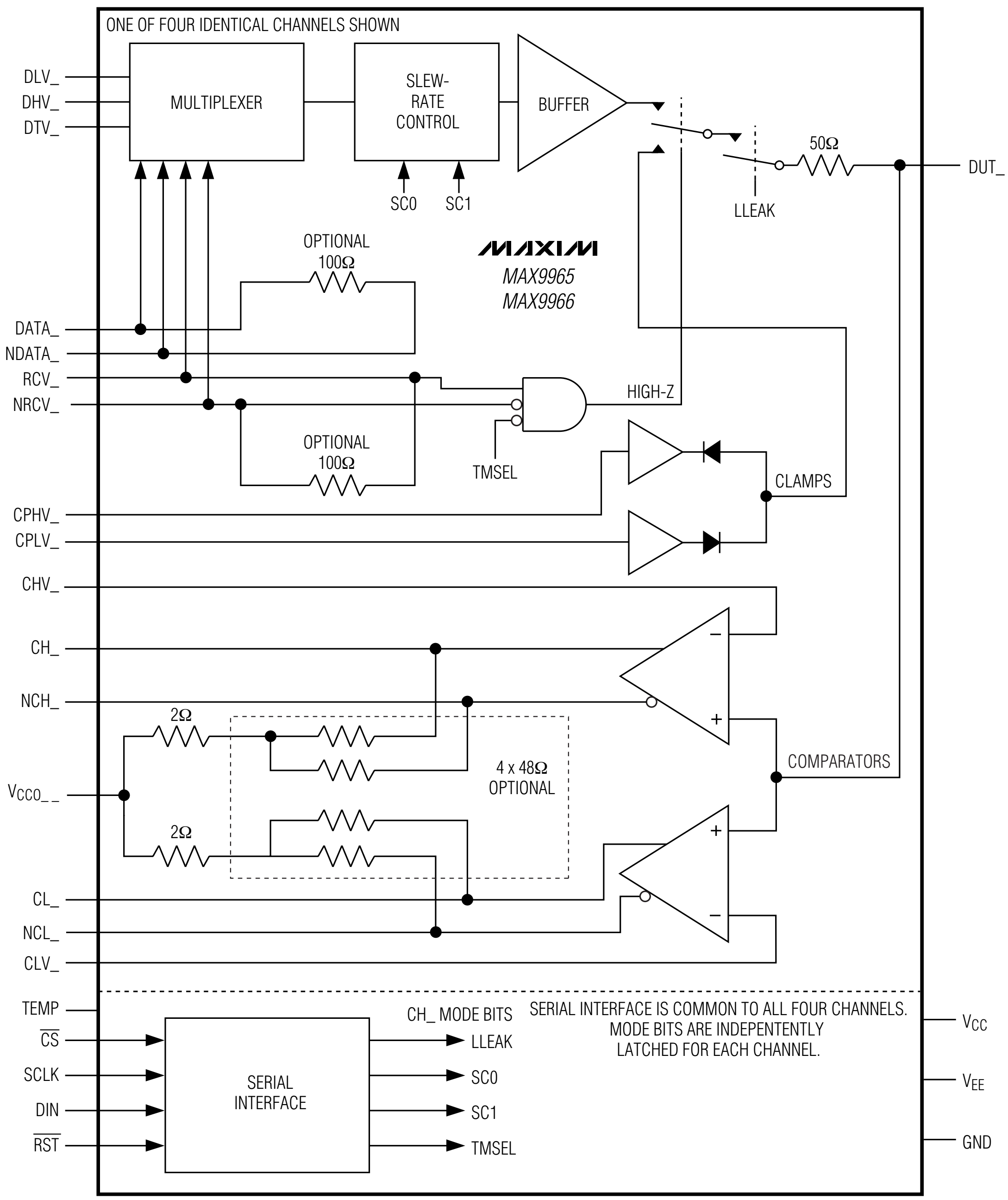


Figure 1. MAX9965/MAX9966 Block Diagram

Detailed Description

The MAX9965/MAX9966 four-channel, high-speed pin electronics driver and comparator ICs for automatic test equipment include, for each channel, a three-level pin driver, a dual comparator, and variable clamps (Figure 1). The driver features a -1.5V to +6.5V operating range and high-speed operation, including high-Z and active termination (3rd-level drive) modes, which is highly linear even at low-voltage swings. The devices are similar to the MAX9963/MAX9964 but with a comparator that provides even lower timing dispersion, due to changes in input slew rate and pulse width. The clamps provide damping of high-speed DUT_ waveforms when the device is configured as a high-impedance receiver.

Each of the four channels has high-speed, differential inputs compatible with ECL, LVPECL, LVDS, and GTL signal levels, with optional 100Ω differential input terminations. Optional internal resistors at DATA_ and RCV_ provide differential termination of LVDS inputs. Optional internal resistors at CH_ and CL_ provide the pullup voltage and source termination for open-collector comparator outputs. These options significantly reduce the discrete component count on the circuit board.

The MAX9965/MAX9966 are available in two grade options. An A-grade version provides tighter matching of gain and offset of the drivers, and tighter offset matching of the comparators. This allows reference levels to be shared across multiple channels in cost-sensitive systems. A B-grade version provides lower cost for system designs that incorporate independent reference levels for each channel.

The MAX9965/MAX9966 modal operation is programmed through a 3-wire, low-voltage, CMOS-compatible serial interface.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode control bit TMSEL. A slew-rate circuit controls the slew rate of the buffer input. One of four possible slew rates can be selected (Table 1); the speed of the internal multiplexer sets the 100% driver slew rate (see the Driver Large-Signal Response in the *Typical Operating Characteristics*).

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed in low-leakage mode (Figure 2, Table 2). In high-impedance mode, the clamps are connected. This switching is controlled by the high-speed input RCV_ and the mode control bits TMSEL and LLEAK. In high-impedance mode, the bias current at DUT_ is less than 2µA over the 0 to 3V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 15nA. See the *Low-Leakage Mode* section for more detailed information.

The nominal driver output resistance is 50Ω. Contact the factory for different values within the 40Ω to 50Ω range.

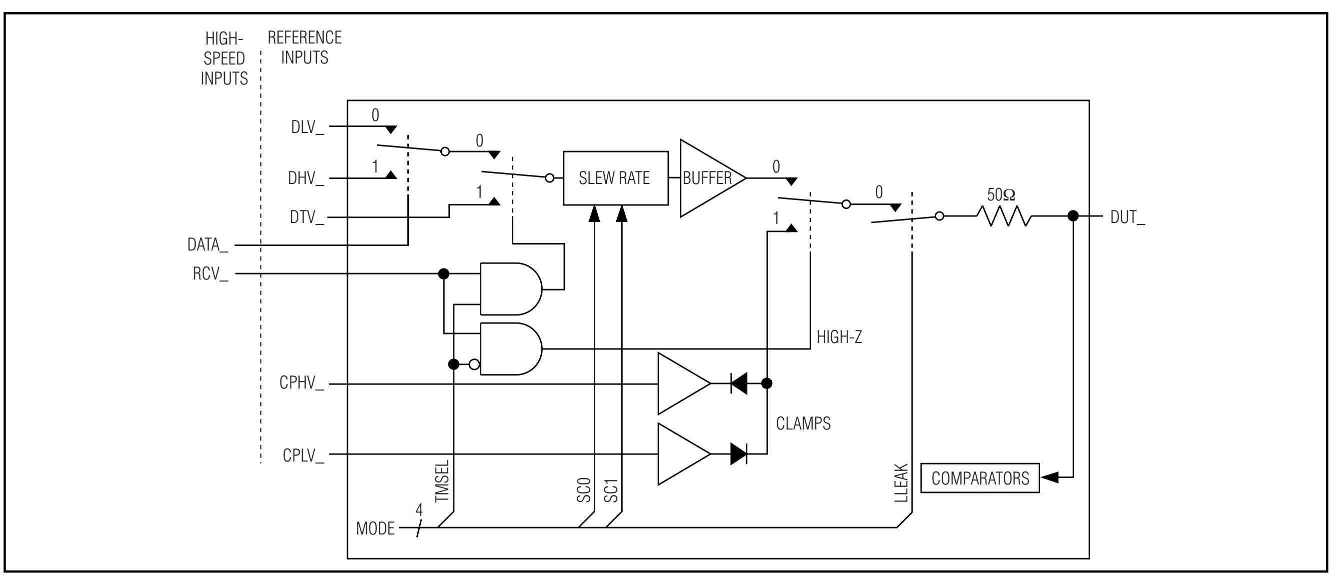


Figure 2. Simplified Driver Channel

Table 1. Slew Rate Logic

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

Table 2. Driver Logic

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA_	RCV_	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-z)
X	X	X	1	Low-leakage mode

Clamps

A pair of voltage clamps (high and low) can be configured to limit the voltage at DUT_, and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using external connections CPHV_ and CPLV_. The clamps are enabled only when the driver is in the high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range and must be empirically determined. The optimal clamp voltages are application specific. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected DUT_ voltage range; overvoltage protection remains active without loading DUT_.

Comparators

The MAX9965/MAX9966 have two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 3.

The MAX9965/MAX9966s' comparators feature BJT inputs for improved comparator dispersion in contrast to the MAX9963/MAX9964s' JFET comparators.

Table 3. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CH_	CL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

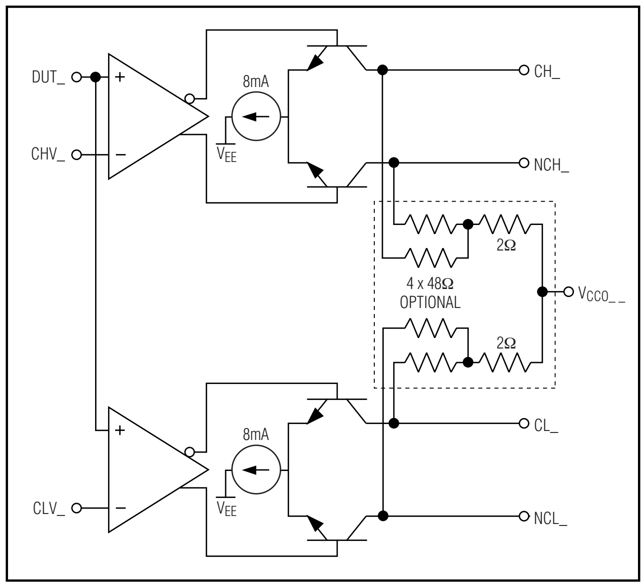


Figure 3. Open-Collector Comparator Outputs

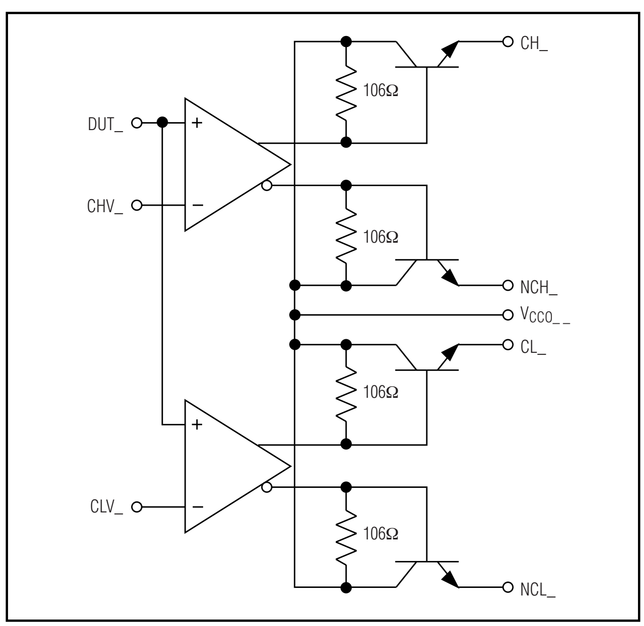


Figure 4. Open-Emitter Comparator Outputs

Quad Low-Power, 500Mbps ATE Driver/Comparator

Three configurations are available for the comparator differential outputs to ease interfacing with a wide variety of logic families. An open-collector configuration switches an 8mA current source between two outputs. This configuration is available with and without internal termination resistors connected to $V_{CCO\_}$ (Figure 3). For external termination, leave $V_{CCO\_}$ unconnected and add the required external resistors. These resistors are typically 50Ω to the pullup voltage at the receiving end of the output trace. Alternate configurations may be used, provided that the Absolute Maximum Ratings are not exceeded. For internal termination, connect $V_{CCO\_}$ to the desired VOH voltage. Each output provides a nominal 400mV_{P-P} swing and 50Ω source termination.

An open-emitter configuration is also available (Figure 4). Connect an external collector voltage to $V_{CCO\_}$ and add external pulldown resistors. These are typically 50Ω to $V_{CCO\_}$ -2V at the receiving end of the output trace. Alternate configurations may be used, provided that the Absolute Maximum Ratings are not exceeded.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with $\overline{RST}$ places the MAX9965/MAX9966 into a very-low-leakage state in which the DUT_ input current is less than 15nA over the 0 to 3V range. In this mode, the driver, comparators, and clamps are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel. If DUT_ is driven with a high-speed signal while LLEAK is asserted, leakage current momentarily increases beyond the limits specified for normal operation. The Low-Leakage Recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 4. Shift Register Functions

BIT	NAME	FUNCTION
D7	1E	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to zero to make no change to channel 1.
D6	2E	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to zero to make no change to channel 2.
D5	3E	Channel 3 Write Enable. Set to 1 to update the control byte for channel 3. Set to zero to make no change to channel 3.
D4	4E	Channel 4 Write Enable. Set to 1 to update the control byte for channel 4. Set to zero to make no change to channel 4.
D3	LLEAK	Low-Leakage Select. Set to 1 to put driver and clamps into low-leakage mode. Set to zero for normal operation.
D2	SC1	Driver Slew Rate Select. SC1 and SC0 set the driver slew rate. See Table 1.
D1	SC0	
D0	TMSEL	Driver Termination Select. Set to 1 to force the driver output to the DTV_ voltage (term mode) when RCV_ = 1. Set to zero to place the driver into a high impedance state (high-z mode) when RCV_ = 1. See Table 2.

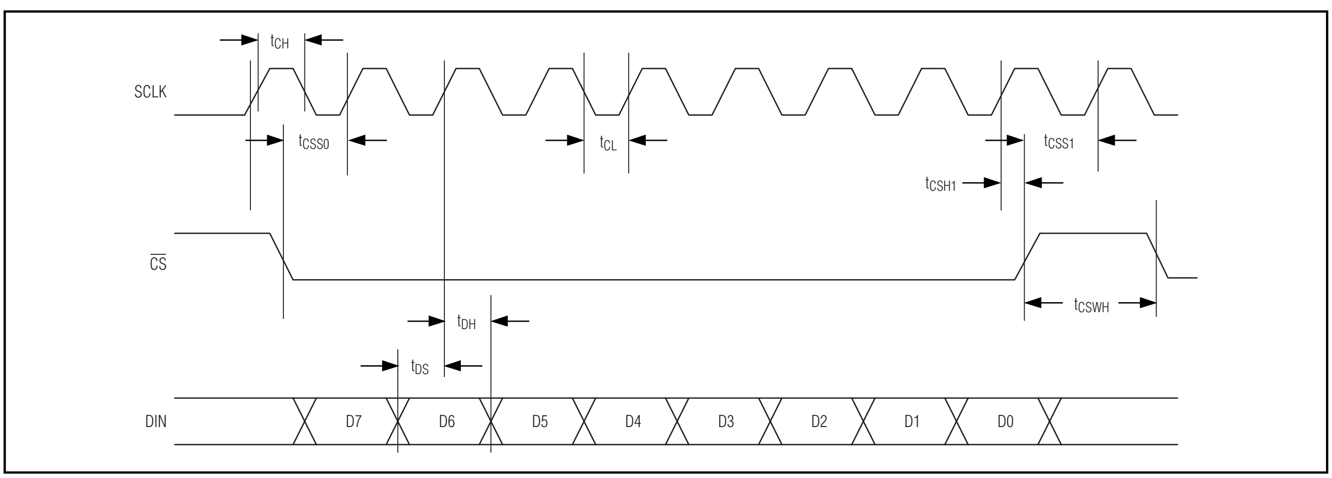


Figure 5. Serial Interface Timing

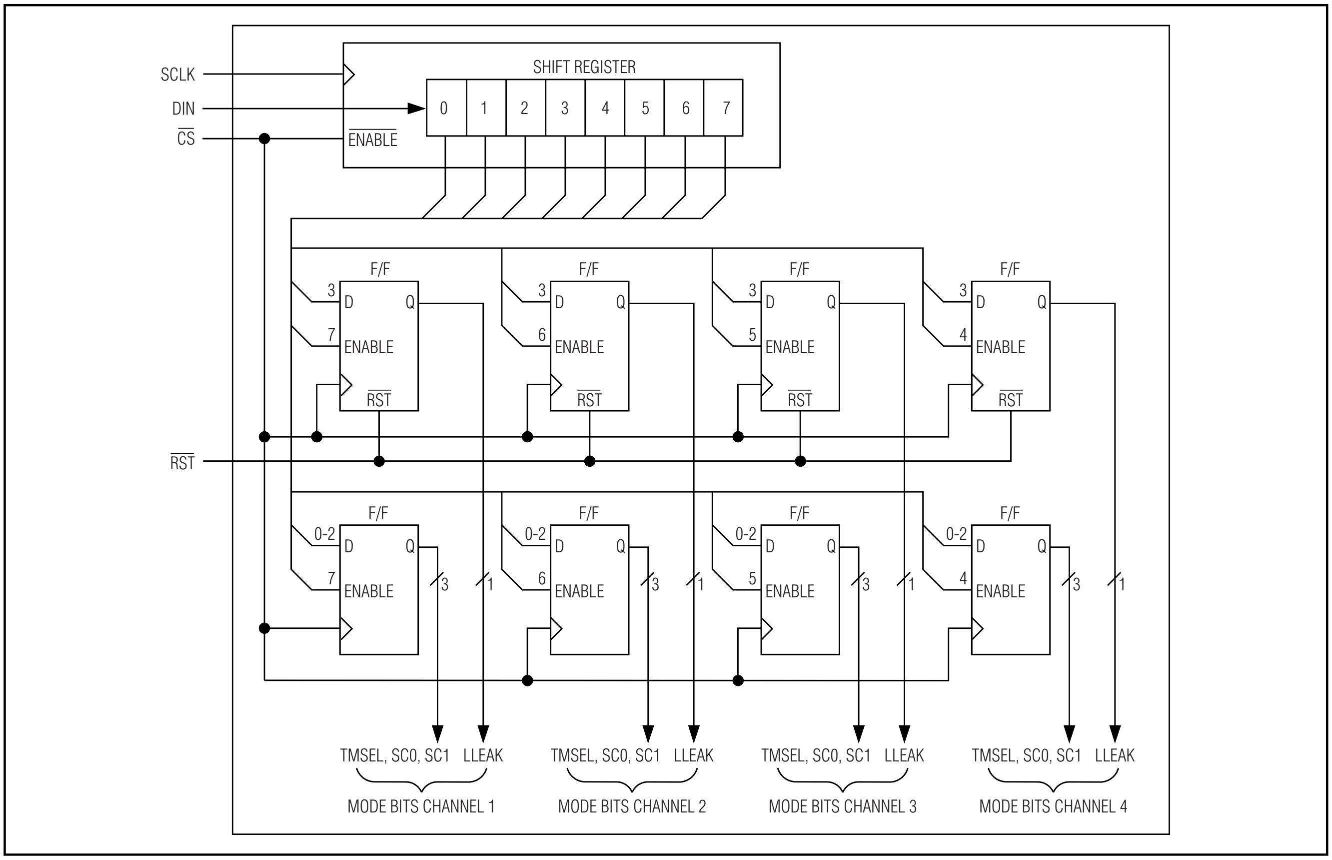


Figure 6. Serial Interface

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal output voltage of 3.43V at a die temperature of +70°C (343K). The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 15kΩ (typ).

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9965/MAX9966 modes (Figure 6). Control data flow into a bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high, as shown in the serial timing diagram, Figure 5. Data from the shift register are then loaded into any or all of a group of four quad latches, determined by bits D4 through D7, as indicated in Figure 6 and Table 4. The quad latches contain the four mode bits for each channel of the quad pin driver. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel, as shown in Tables 1 and 2. $\overline{RST}$ sets LLEAK = 1 for all channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

Heat Removal

These devices require heat removal under normal circumstances through the exposed pad, either by soldering to circuit board copper (MAX9966) or by use of an external heat sink (MAX9965). The exposed pad is electrically at V_{EE} potential for both package types, and must be either connected to V_{EE} or isolated.

Chip Information

TRANSISTOR COUNT: 7293

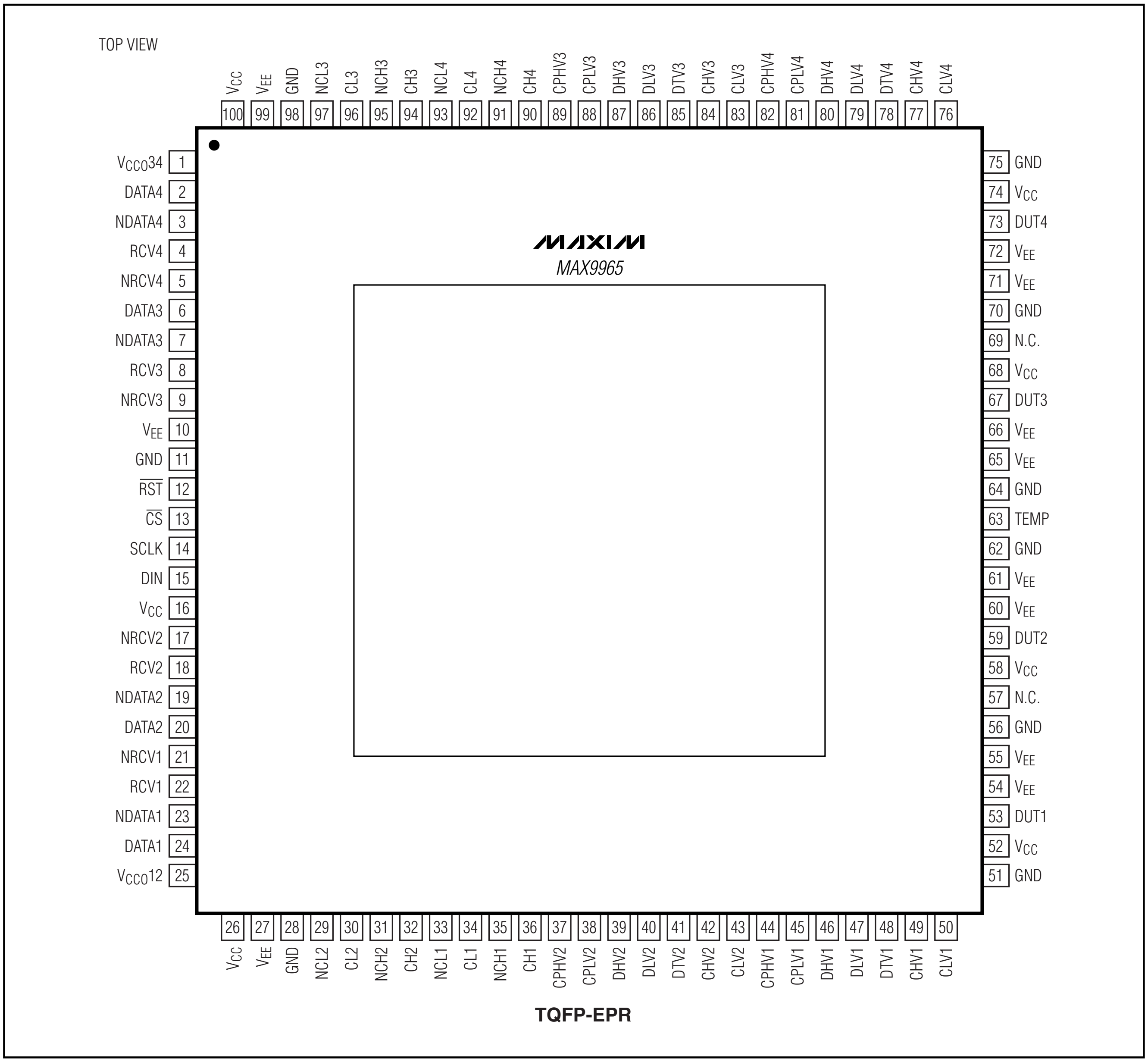
PROCESS: Bipolar

Selector Guide

PART	ACCURACY GRADE	COMPARATOR OUTPUT TYPE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION	HEAT EXTRACTION	PIN-PACKAGE
MAX9965ADCCQ*	A	Open collector	None	None	Top	100 TQFP-EPR
MAX9965AKCCQ*	A	Open collector	None	100Ω LVDS	Top	100 TQFP-EPR
MAX9965AGCCQ*	A	Open collector	50Ω to $V_{CCO\_}$	100Ω LVDS	Top	100 TQFP-EPR
MAX9965AHCCQ*	A	Open emitter	None	None	Top	100 TQFP-EPR
MAX9965AJCCQ*	A	Open emitter	None	100Ω LVDS	Top	100 TQFP-EPR
MAX9965BDCCQ*	B	Open collector	None	None	Top	100 TQFP-EPR
MAX9965BKCCQ*	B	Open collector	None	100Ω LVDS	Top	100 TQFP-EPR
MAX9965BGCCQ	B	Open collector	50Ω to $V_{CCO\_}$	100Ω LVDS	Top	100 TQFP-EPR
MAX9965BHCCQ*	B	Open emitter	None	None	Top	100 TQFP-EPR
MAX9965BJCCQ	B	Open emitter	None	100Ω LVDS	Top	100 TQFP-EPR
MAX9966ADCCQ*	A	Open collector	None	None	Bottom	100 TQFP-EP
MAX9966AKCCQ*	A	Open collector	None	100Ω LVDS	Bottom	100 TQFP-EP
MAX9966AGCCQ*	A	Open collector	50Ω to $V_{CCO\_}$	100Ω LVDS	Bottom	100 TQFP-EP
MAX9966AHCCQ*	A	Open emitter	None	None	Bottom	100 TQFP-EP
MAX9966AJCCQ*	A	Open emitter	None	100Ω LVDS	Bottom	100 TQFP-EP
MAX9966BDCCQ*	B	Open collector	None	None	Bottom	100 TQFP-EP
MAX9966BKCCQ*	B	Open collector	None	100Ω LVDS	Bottom	100 TQFP-EP
MAX9966BGCCQ	B	Open collector	50Ω to $V_{CCO\_}$	100Ω LVDS	Bottom	100 TQFP-EP
MAX9966BHCCQ*	B	Open emitter	None	None	Bottom	100 TQFP-EP
MAX9966BJCCQ*	B	Open emitter	None	100Ω LVDS	Bottom	100 TQFP-EP

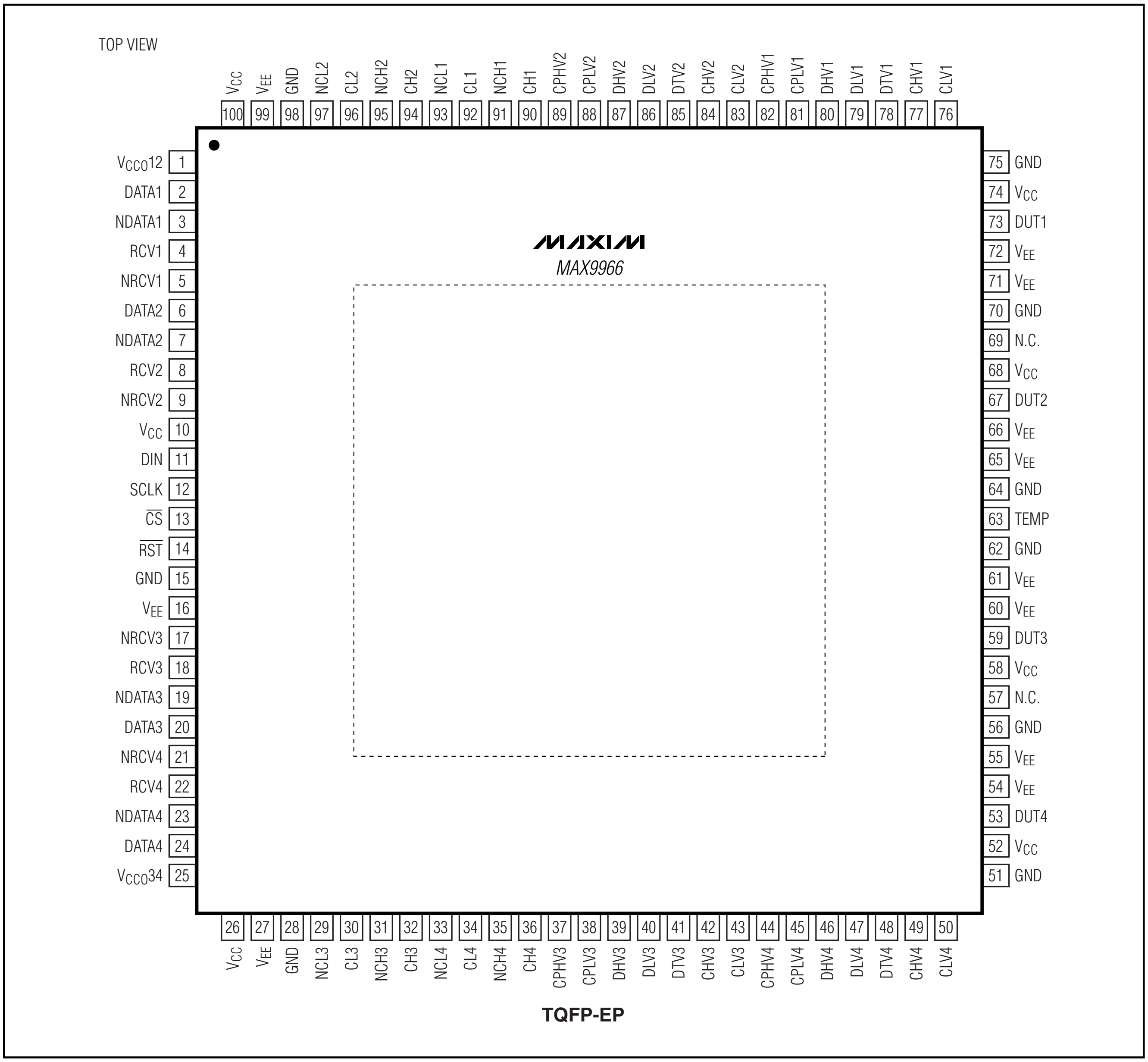
**Future product—contact factory for availability.*

MAX9965 Pin Configuration



Quad Low-Power, 500Mbps ATE Driver/Comparator

MAX9966 Pin Configuration



Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

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