19-3557; Rev 2; 10/05

MAXIM

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

General Description

The MAX9218 digital video serial-to-parallel converter deserializes a total of 27 bits during data and control phases. In the data phase, the LVDS serial input is converted to 18 bits of parallel video data and in the control phase, the input is converted to 9 bits of parallel control data. The separate video and control phases take advantage of video timing to reduce the serial data rate. The MAX9218 pairs with the MAX9217 serializer to form a complete digital video transmission system.

Proprietary data decoding reduces EMI and provides DC balance. The DC balance allows AC-coupling, providing isolation between the transmitting and receiving ends of the interface. The MAX9218 features a selectable rising or falling output latch edge.

ESD tolerance is specified for ISO 10605 with ±10kV contact discharge and ±30kV air discharge.

The MAX9218 operates from a +3.3V core supply and features a separate output supply for interfacing to 1.8V to 3.3V logic-level inputs. This device is available in 48-lead Thin QFN and TQFP packages and is specified from -40°C to +85°C.

Applications

Navigation System Display

In-Vehicle Entertainment System

Video Camera

LCD Displays

Features

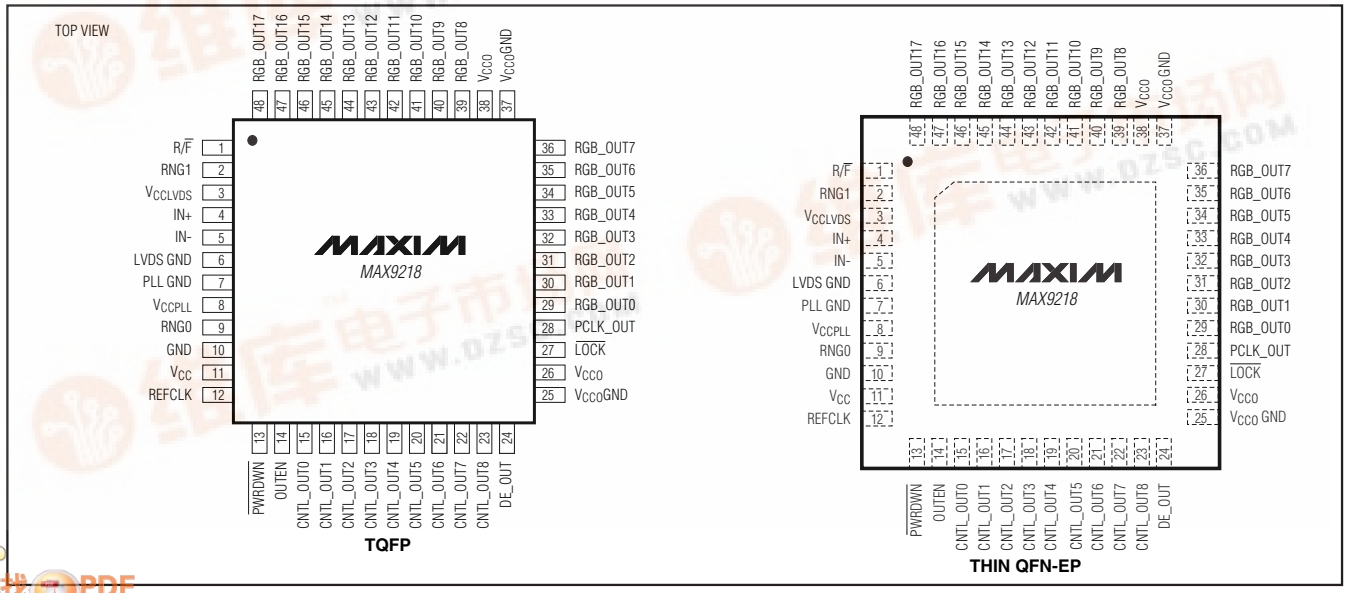
- ♦ Proprietary Data Decoding for DC Balance and Reduced EMI
- ♦ Control Data Deserialized During Video Blanking
- ♦ Five Control Data Inputs Are Single Bit-Error Tolerant
- ♦ Output Transition Time Is Scaled to Operating Frequency for Reduced EMI
- ♦ Staggered Output Switching Reduces EMI
- ♦ Output Enable Allows Busing of Outputs
- ♦ Clock Pulse Stretch on Lock
- ♦ Wide ±2% Reference Clock Tolerance
- ♦ Synchronizes to MAX9217 Serializer Without External Control
- ♦ ISO 10605 ESD Protection
- ♦ Separate Output Supply Allows Interface to 1.8V to 3.3V Logic
- ♦ +3.3V Core Power Supply
- ♦ Space-Saving Thin QFN and TQFP Packages
- ♦ -40°C to +85°C Operating Temperature

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9218ECM	-40°C to +85°C	48 TQFP	C48-5
MAX9218ETM	-40°C to +85°C	48 Thin QFN-EP*	T4866-1

*EP = Exposed pad.

Pin Configurations



27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to _GND.....-0.5V to +4.0V
Any Ground to Any Ground.....-0.5V to +0.5V
IN+, IN- to LVDS GND.....-0.5V to +4.0V
IN+, IN- Short Circuit to LVDS GND or V_{CCLVDS} .....Continuous
IN+, IN- Short Through 0.125µF (or smaller), 25V Series Capacitor.....-0.5V to +16V
(R/$\overline{F}$, OUTEN, RNG_, REFCLK, $\overline{PWRDWN}$) to GND.....-0.5V to (V_{CC} + 0.5V)
(RGB_OUT[17:0], CNTL_OUT[8:0], DE_OUT, PCLK_OUT, $\overline{LOCK}$) to V_{CCO} GND.....-0.5V to (V_{CCO} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
48-Lead TQFP (derate 20.8mW/°C above +70°C) 1667mW
48-Lead Thin QFN (derate 37mW/°C above +70°C) .2963mW
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND.....±3.0kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge (IN+, IN-) to GND.....±10kV
Air Discharge (IN+, IN-) to GND.....±30kV
Storage Temperature Range.....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (R/$\overline{F}$, OUTEN, RNG0, RNG1, REFCLK, $\overline{PWRDWN}$)						
High-Level Input Voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low-Level Input Voltage	V_{IL}		-0.3		+0.8	V
Input Current	I_{IN}	V_{IN} = -0.3V to (V_{CC} + 0.3V), $\overline{PWRDWN}$ = high or low	-70		+70	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-1.5	V
SINGLE-ENDED OUTPUTS (RGB_OUT[17:0], CNTL_OUT[8:0], DE_OUT, PCLK_OUT, $\overline{LOCK}$)						
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA	V_{CCO} - 0.1			V
		I_{OH} = -2mA, RNG1, RNG0 = high	V_{CCO} - 0.35			
		I_{OH} = -2mA, RNG1, RNG0 both not high simultaneously	V_{CCO} - 0.4			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA			0.1	V
		I_{OL} = 2mA, RNG1, RNG0 = high			0.3	
		I_{OL} = 2mA, RNG1, RNG0 both not high simultaneously			0.35	
High-Impedance Output Current	I_{OZ}	$\overline{PWRDWN}$ = low or OUTEN = low, V_O = -0.3V to V_{CCO} + 0.3V	-10		+10	µA

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	RNG1, RNG0 = high, V_O = 0			-10		-50	mA
		RNG1, RNG0 both not high simultaneously, V_O = 0			-7		-40	
LVDS INPUT (IN+, IN-)								
Differential Input High Threshold	V_{TH}						50	mV
Differential Input Low Threshold	V_{TL}				-50			mV
Input Current	I_{IN+}, I_{IN-}	$\overline{PWRDWN}$ = high or low			-20		+20	µA
Input Bias Resistor	R_{IB}	$\overline{PWRDWN}$ = high or low			35	50	65	kΩ
		$V_{CC\_}$ = 0 or open, $\overline{PWRDWN}$ = 0 or open, Figure 1			35	50	65	kΩ
Power-Off Input Current	I_{INO+}, I_{INO-}	$V_{CC\_}$ = 0 or open, $\overline{PWRDWN}$ = 0 or open			-40		+40	µA
POWER SUPPLY								
Worst-Case Supply Current	I_{CCW}	C_L = 8pF, worst-case pattern, Figure 2	RNG1 = low, RNG0 = low	3MHz			20	mA
				7MHz			35	
			RNG1 = high, RNG0 = low	7MHz			25	
				15MHz			47	
			RNG1 = high, RNG0 = high	15MHz			37	
				35MHz			70	
Power-Down Supply Current	I_{CCZ}	(Note 3)					50	µA

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AC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to 3.6V, C_L = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFCLK TIMING REQUIREMENTS							
Period	t_T			28.57		333.00	ns
Frequency	f_{CLK}			3		35	MHz
Frequency Variation	Δf_{CLK}	REFCLK to serializer PCLK_IN		-2.0		+2.0	%
Duty Cycle	DC			40	50	60	%
Transition Time	t_{TRAN}	20% to 80%				6	ns
SWITCHING CHARACTERISTICS							
Output Rise Time	t_R	Figure 3	RNG1, RNG0 = high	3.2		4.4	ns
			RNG1, RNG0 both not high simultaneously	3.8		5.5	
Output Fall Time	t_F	Figure 3	RNG1, RNG0 = high	2.7		4.5	ns
			RNG1, RNG0 both not high simultaneously	3.6		5.3	
PCLK_OUT High Time	t_{HIGH}	Figure 4		0.4 x t_T	0.45 x t_T	0.6 x t_T	ns
PCLK_OUT Low Time	t_{LOW}	Figure 4		0.4 x t_T	0.45 x t_T	0.6 x t_T	ns
Data Valid Before PCLK_OUT	t_{DVB}	Figure 5		0.35 x t_T	0.4 x t_T		ns
Data Valid After PCLK_OUT	t_{DVA}	Figure 5		0.35 x t_T	0.4 x t_T		ns
Input-to-Output Delay	t_{DELAY}	Figure 6		2.575 x t_T + 8.5		2.725 x t_T + 12.8	ns
PLL Lock to REFCLK	t_{PLLREF}	Figure 7				16385 x t_T	ns
Power-Down Delay	t_{PDD}	Figure 7				100	ns
Output Enable Time	t_{OE}	Figure 8				30	ns
Output Disable Time	t_{OZ}	Figure 9				30	ns

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} and V_{TL}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +25°C.

Note 3: All LVTTL/LVCMOS inputs, except $\overline{PWRDWN}$ at ≤ 0.3V or ≥ V_{CC} - 0.3V. $\overline{PWRDWN}$ is ≤ 0.3V.

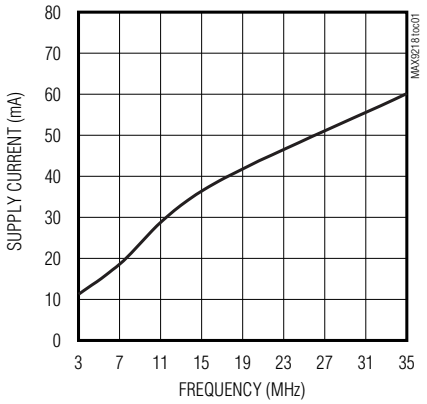
Note 4: AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

Note 5: C_L includes probe and test jig capacitance.

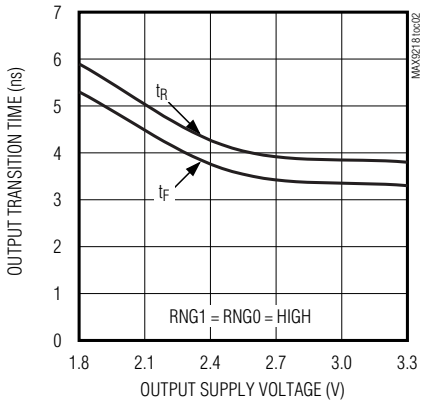
Typical Operating Characteristics

($V_{CC\_}$ = +3.3V, C_L = 8pF, T_A = +25°C, unless otherwise noted.)

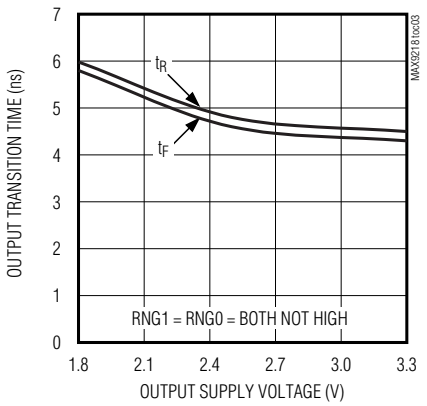
WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY



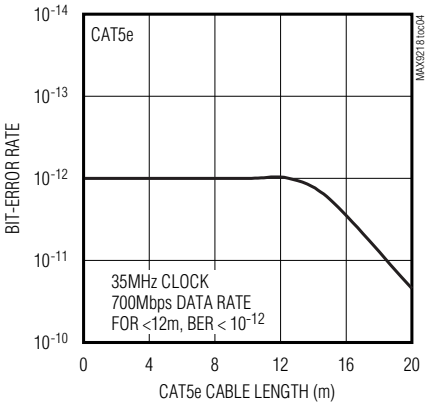
OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE (V_{CCO})



OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE (V_{CCO})



BIT-ERROR RATE vs. CABLE LENGTH



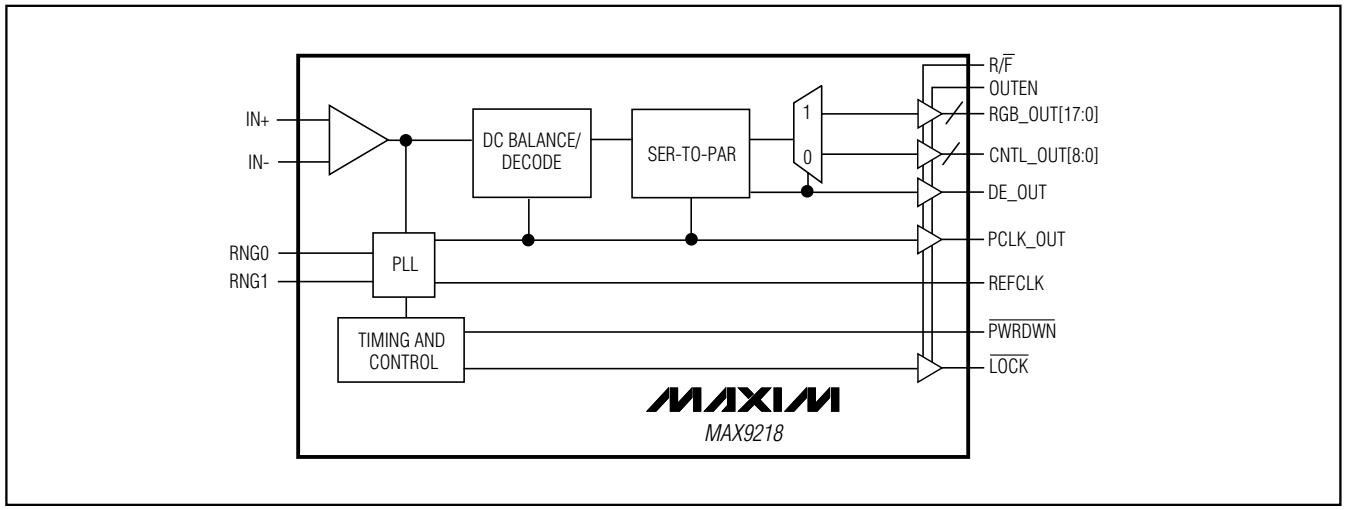
27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

Pin Description

PIN	NAME	FUNCTION
1	R/$\overline{F}$	Rising or Falling Latch Edge Select. LVTTL/LVCMOS input. Selects the edge of PCLK_OUT for latching data into the next chip. Set R/$\overline{F}$ = high for a rising latch edge. Set R/$\overline{F}$ = low for a falling latch edge. Internally pulled down to GND.
2	RNG1	LVTTL/LVCMOS Range Select Input. Set to the range that includes the serializer parallel clock input frequency. Internally pulled down to GND.
3	V_{CCLVDS}	LVDS Supply Voltage. Bypass to LVDS GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
4	IN+	Noninverting LVDS Serial Data Input
5	IN-	Inverting LVDS Serial Data Input
6	LVDS GND	LVDS Supply Ground
7	PLL GND	PLL Supply Ground
8	V_{CCPLL}	PLL Supply Voltage. Bypass to PLL GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
9	RNG0	LVTTL/LVCMOS Range Select Input. Set to the range that includes the serializer parallel clock input frequency. Internal pulldown to GND.
10	GND	Digital Supply Ground
11	V_{CC}	Digital Supply Voltage. Supply for LVTTL/LVCMOS inputs and digital circuits. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
12	REFCLK	LVTTL/LVCMOS Reference Clock Input. Apply a reference clock that is within ±2% of the serializer PCLK_IN frequency. Internally pulled down to GND.
13	$\overline{PWRDWN}$	LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND.
14	OUTEN	LVTTL/LVCMOS Output Enable Input. High activates the single-ended outputs. Driving low places the single-ended outputs in high impedance. Internally pulled down to GND.
15–23	CNTL_OUT [8:0]	LVTTL/LVCMOS Control Data Outputs. CNTL_OUT[8:0] are latched into the next chip on the rising or falling edge of PCLK_OUT as selected by R/$\overline{F}$ when DE_OUT is low, and are held at the last state when DE_OUT is high.
24	DE_OUT	LVTTL/LVCMOS Data Enable Output. High indicates RGB_OUT[17:0] are active. Low indicates CNTL_OUT[8:0] are active.
25, 37	V_{CCO} GND	Output Supply Ground
26, 38	V_{CCO}	Output Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
27	$\overline{LOCK}$	LVTTL/LVCMOS Lock Indicator Output. Outputs are valid when $\overline{LOCK}$ is low.
28	PCLK_OUT	LVTTL/LVCMOS Parallel Clock Output. Latches data into the next chip on the edge selected by R/$\overline{F}$.
29–36, 39–48	RGB_OUT [17:0]	LVTTL/LVCMOS Red, Green, and Blue Digital Video Data Outputs. RGB_OUT[17:0] are latched into the next chip on the edge of PCLK_OUT selected by R/$\overline{F}$ when DE_OUT is high, and are held at the last state when DE_OUT is low.
EP	GND	Exposed Pad for Thin QFN Package Only. Connect to GND.

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

Functional Diagram



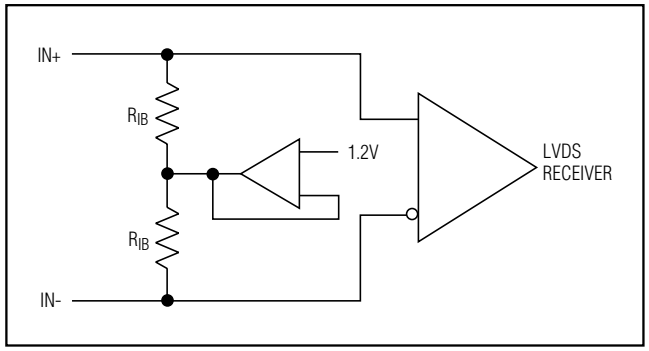


Figure 1. LVDS Input Bias

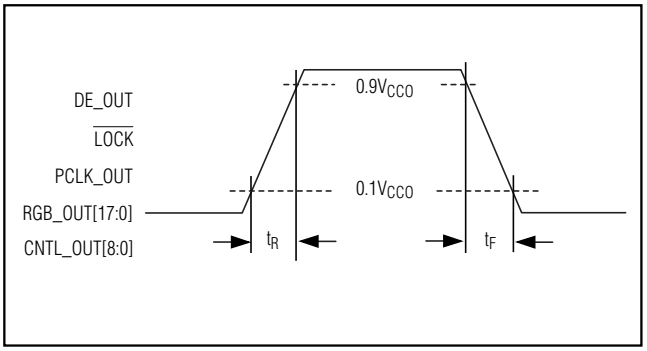


Figure 3. Output Rise and Fall Times

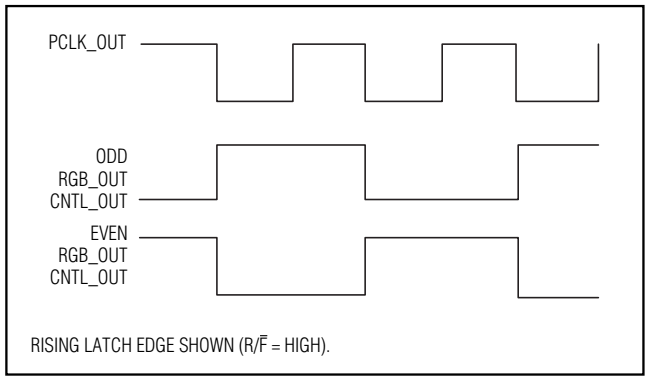


Figure 2. Worst-Case Output Pattern

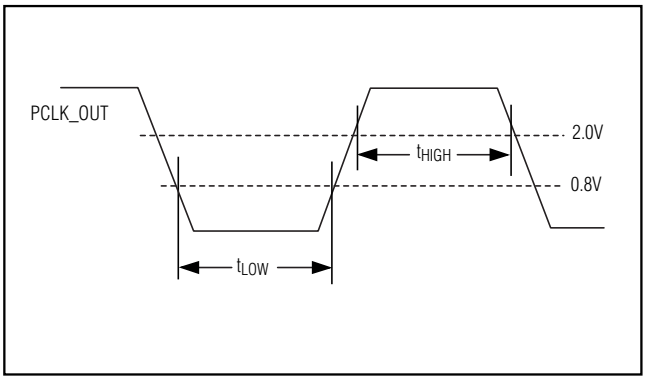


Figure 4. High and Low Times

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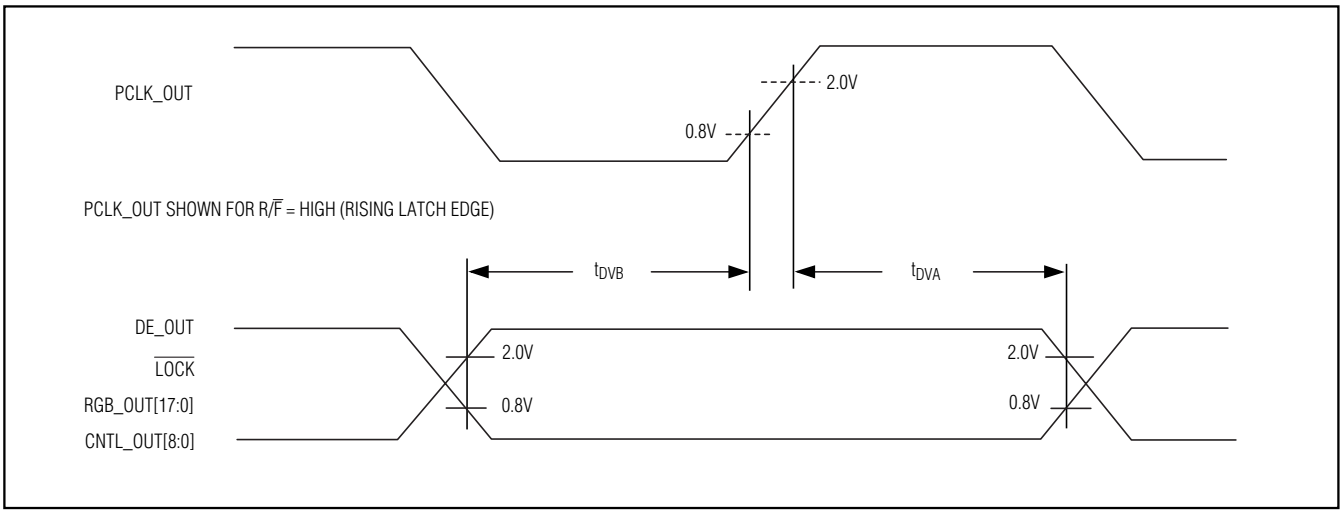

Figure 5. Synchronous Output Timing

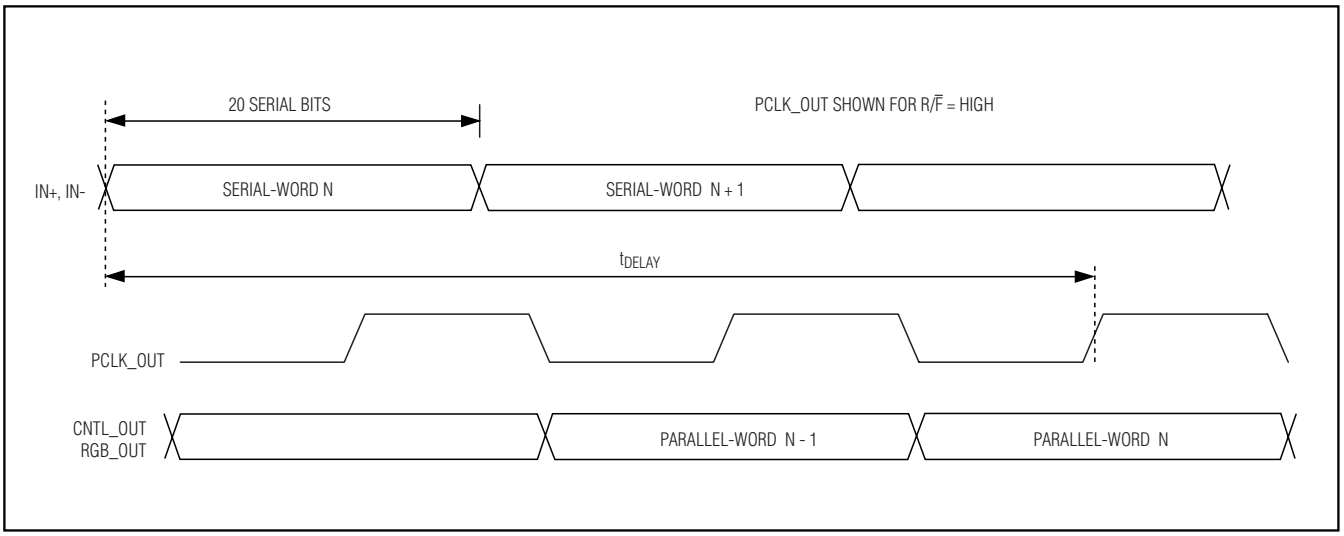

Figure 6. Deserializer Delay

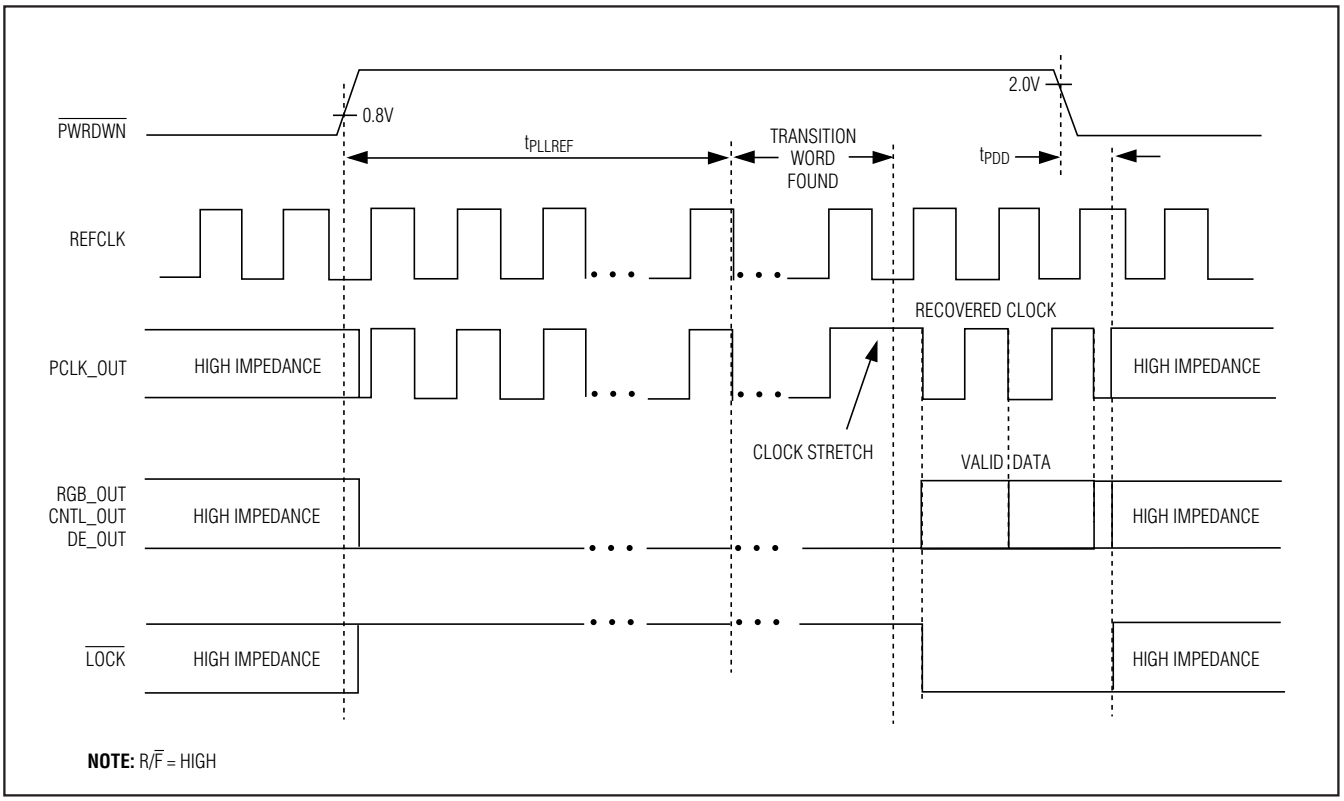

Figure 7. PLL Lock to REFCLK and Power-Down Delay

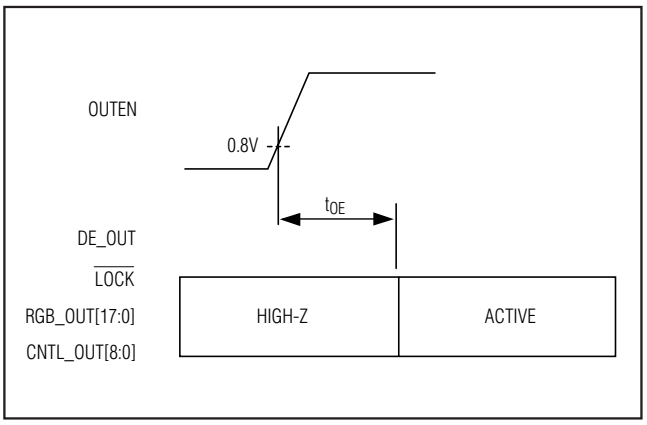

Figure 8. Output Enable Time

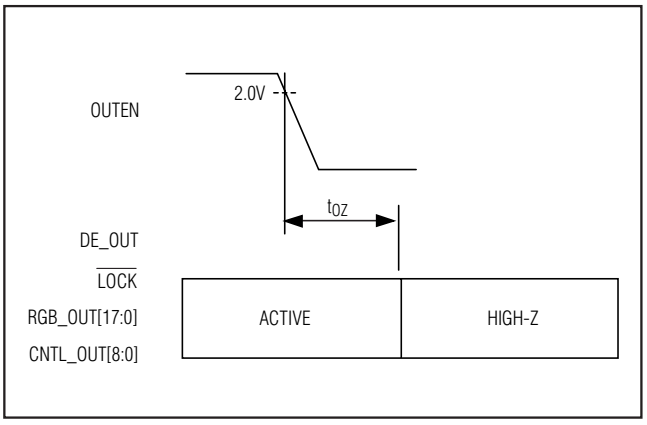

Figure 9. Output Disable Time

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Detailed Description

The MAX9218 DC-balanced deserializer operates at a parallel clock frequency of 3MHz to 35MHz, deserializing video data to the RGB_OUT[17:0] outputs when the data enable output DE_OUT is high, or control data to the CNTL_OUT[8:0] outputs when DE_OUT is low. The video phase words are decoded using 2 overhead bits, EN0 and EN1. Control phase words are decoded with 1 overhead bit, EN0. Encoding, performed by the MAX9217 serializer, reduces EMI and maintains DC balance across the serial cable. The serial input word formats are shown in Table 1 and Table 2.

Control data inputs C0 to C4, each repeated over 3 serial bit times by the serializer, are decoded using majority voting. Two or three bits at the same state determine the state of the recovered bit, providing single bit-error tolerance for C0 to C4. The state of C5 to C8 is determined by the level of the bit itself (no voting is used).

AC-Coupling Benefits

AC-coupling increases the input voltage of the LVDS receiver to the voltage rating of the capacitor. Two capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise. The MAX9217 serializer can also be DC-coupled to the MAX9218 deserializer. Figure 10 is the AC-coupled serializer and deserializer with two capacitors per link, and Figure 11 is the AC-coupled serializer and deserializer with four capacitors per link.

Applications Information

Selection of AC-Coupling Capacitors

See Figure 12 for calculating the capacitor values for AC-coupling, depending on the parallel clock frequency. The plot shows capacitor values for two- and four-capacitor-per-link systems. For applications using less than 18MHz clock frequency, use 0.125µF capacitors.

Termination and Input Bias

The IN+ and IN- LVDS inputs are internally connected to +1.2V through 35kΩ (min) to provide biasing for AC-coupling (Figure 1). Assuming 100Ω interconnect, the LVDS input can be terminated with a 100Ω resistor. Match the termination to the differential impedance of the interconnect.

Use a Thevenin termination, providing 1.2V bias, on an AC-coupled link in noisy environments. For interconnect with 100Ω differential impedance, pull each LVDS line up to V_{CC} with 130Ω and down to ground with 82Ω at the deserializer input (Figure 10 and Figure 11). This termination provides both differential and common-mode termination. The impedance of the Thevenin termination should be half the differential impedance of the interconnect and provide a bias voltage of 1.2V.

Table 1. Serial Video Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	EN1	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17

Bit 0 is the LSB and is deserialized first. EN[1:0] are encoding bits. S[17:0] are encoded symbols.

Table 2. Serial Control Phase Word Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	C0	C0	C0	C1	C1	C1	C2	C2	C2	C3	C3	C3	C4	C4	C4	C5	C6	C7	C8

Bit 0 is the LSB and is deserialized first. C[8:0] are the mapped control inputs.

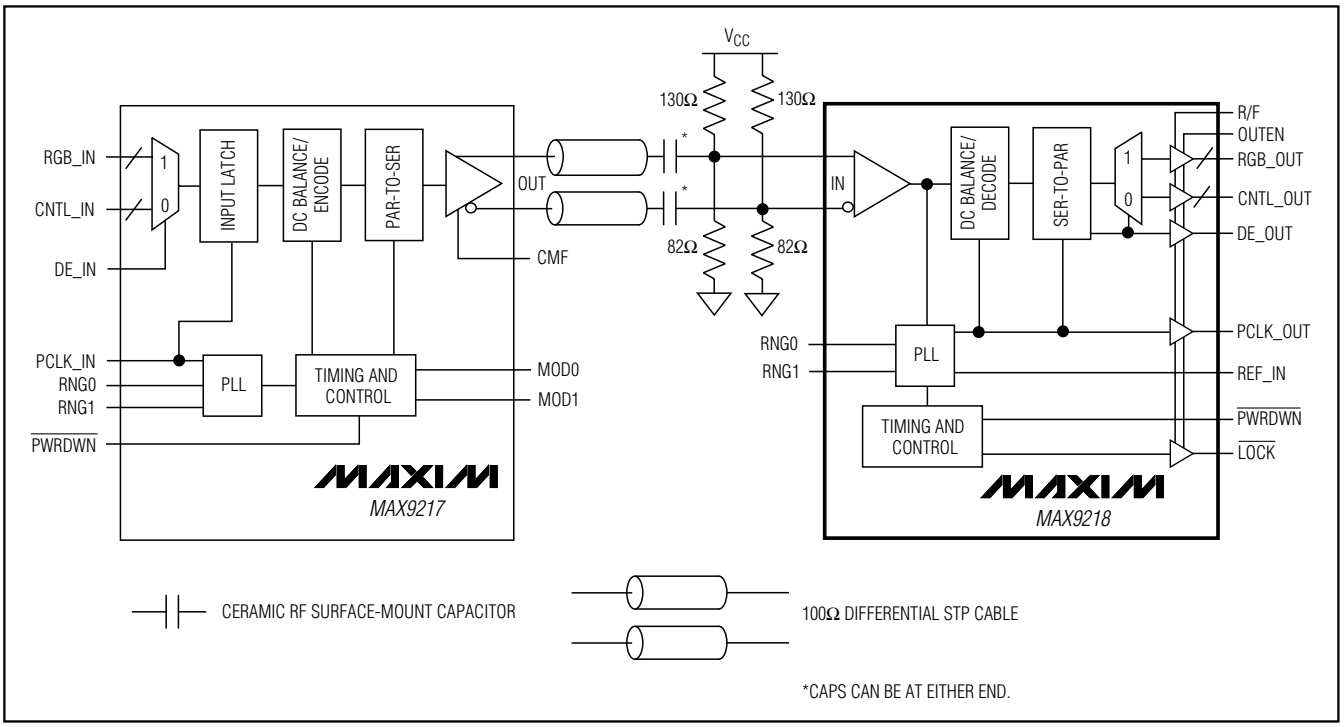


Figure 10. AC-Coupled Serializer and Deserializer with Two Capacitors per Link

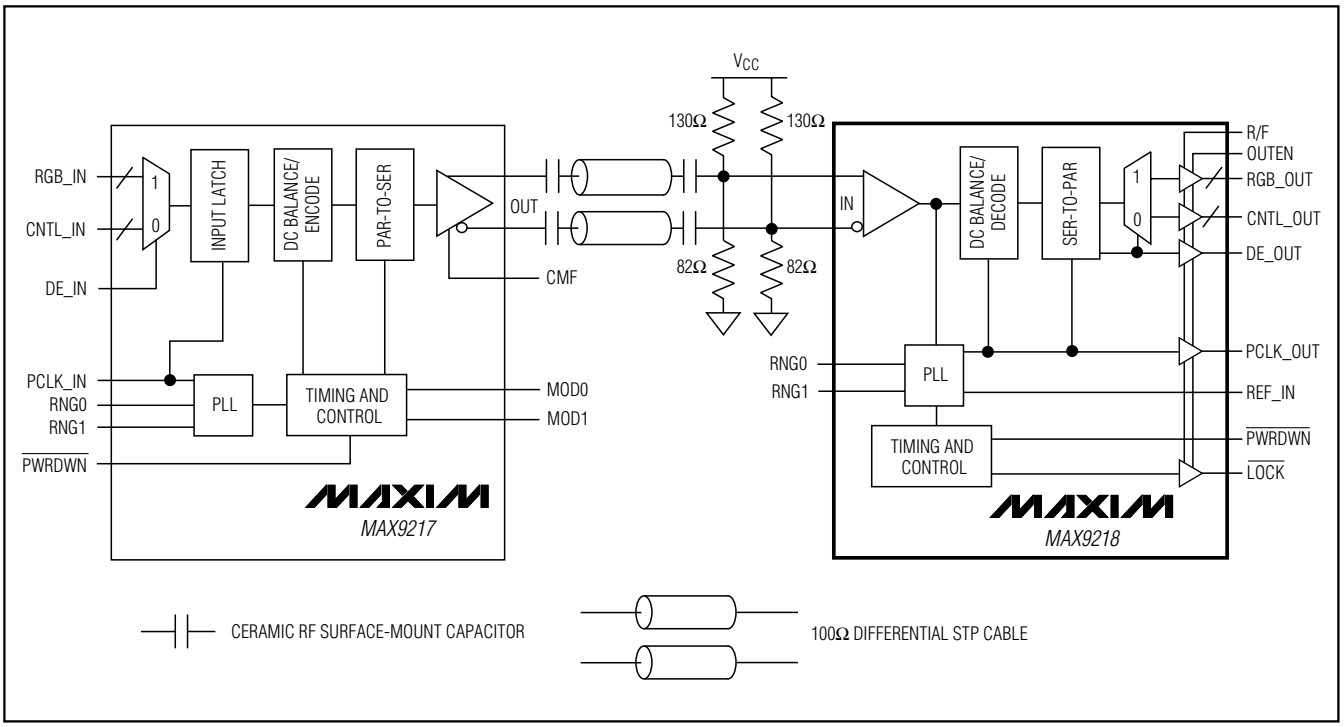


Figure 11. AC-Coupled Serializer and Deserializer with Four Capacitors per Link

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

Input Frequency Detection

A frequency-detection circuit detects when the LVDS input is not switching. When not switching, all outputs except $\overline{LOCK}$ are low, $\overline{LOCK}$ is high, and PCLK_OUT follows REFCLK. This condition occurs, for example, if the serializer is not driving the interconnect or if the interconnect is open.

Frequency Range Setting (RNG[1:0])

The RNG[1:0] inputs select the operating frequency range of the MAX9218 and the transition time of the outputs. Select the frequency range that includes the MAX9217 serializer PCLK_IN frequency. Table 3 shows the selectable frequency ranges and the corresponding data rates and output transition times.

Power Down

Driving $\overline{PWRDWN}$ low puts the outputs in high impedance and stops the PLL. With $\overline{PWRDWN} \le 0.3V$ and all LVTTL/LVCMOS inputs ≤ 0.3V or ≥ V_{CC} - 0.3V, the supply current is reduced to less than 50µA. Driving $\overline{PWRDWN}$ high initiates lock to the local reference clock (REFCLK) and afterwards to the serial input.

Lock and Loss of Lock ($\overline{LOCK}$)

When $\overline{PWRDWN}$ is driven high, the PLL begins locking to REFCLK, drives $\overline{LOCK}$ from high impedance to high and the other outputs from high impedance to low except PCLK_OUT. PCLK_OUT outputs REFCLK while the PLL is locking to REFCLK. Locking to REFCLK takes a maximum of 16,385 REFCLK cycles. When locking to REFCLK is complete, the serial input is monitored for a transition word. When a transition word is found, $\overline{LOCK}$ is driven low indicating valid output data, and the parallel rate clock recovered from the serial input is output on PCLK_OUT. PCLK_OUT is stretched on the change from REFCLK to recovered clock (or vice versa).

Table 3. Frequency Range Programming

RNG1	RNG0	PARALLEL CLOCK (MHz)	SERIAL DATA RATE (Mbps)	OUTPUT TRANSITION TIME
0	0	3 to 7	60 to 140	Slow
0	1			
1	0	7 to 15	140 to 300	
1	1	15 to 35	300 to 700	Fast

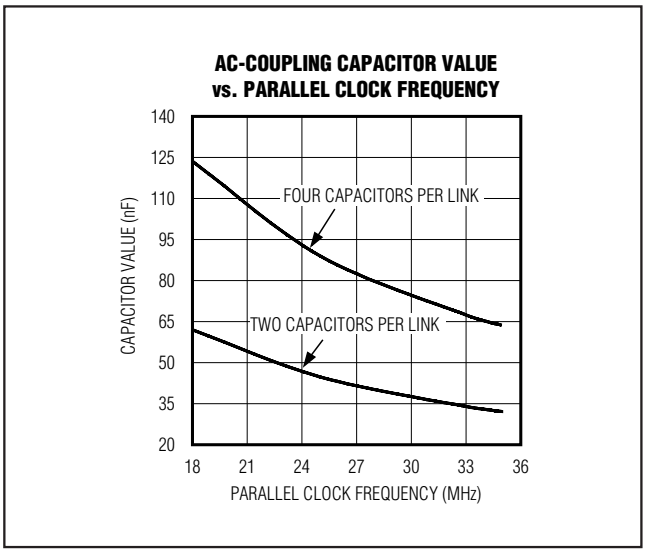


Figure 12. AC-Coupling Capacitor Values vs. Clock Frequency of 18MHz to 35MHz

If a transition word is not detected within 2^{20} cycles of PCLK_OUT, $\overline{LOCK}$ is driven high and the other outputs except PCLK_OUT are driven low. REFCLK is output on PCLK_OUT and the deserializer continues monitoring the serial input for a transition word. See Figure 7 for the synchronization timing diagram.

Output Enable (OUTEN) and Busing Outputs

The outputs of two MAX9218s can be bused to form a 2:1 mux with the outputs controlled by the output enable. Wait 30ns between disabling one deserializer (driving OUTEN low) and enabling the second one (driving OUTEN high) to avoid contention of the bused outputs. OUTEN controls all outputs.

Rising or Falling Output Latch Edge (R/$\overline{F}$)

The MAX9218 has a selectable rising or falling output latch edge through a logic setting on R/$\overline{F}$. Driving R/$\overline{F}$ high selects the rising output latch edge, which latches the parallel output data into the next chip on the rising edge of PCLK_OUT. Driving R/$\overline{F}$ low selects the falling output latch edge, which latches the parallel output data into the next chip on the falling edge of PCLK_OUT. The MAX9218 output-latch-edge polarity does not need to match the MAX9217 serializer input-latch-edge polarity. Select the latch-edge polarity required by the chip being driven by the MAX9218.

Staggered and Transition Time Adjusted Outputs

RGB_OUT[17:0] are grouped into three groups of six, with each group switching about 1ns apart in the video phase to reduce EMI and ground bounce. CNTL_OUT[8:0] switch during the control phase. Output transition times are slower in the 3MHz-to-7MHz and 7MHz-to-15MHz ranges and faster in the 15MHz-to-35MHz range.

Data Enable Output (DE_OUT)

The MAX9218 deserializes video and control data at different times. Control data is deserialized during the video blanking time. DE_OUT high indicates that video data is being deserialized and output on RGB_OUT[17:0]. DE_OUT low indicates that control data is being deserialized and output on CNTL_OUT[8:0]. When outputs are not being updated, the last data received is latched on the outputs. Figure 13 shows the DE_OUT timing.

Power-Supply Circuits and Bypassing

There are separate on-chip power domains for digital circuits and LVTTL/LVCMOS inputs (V_{CC} supply and GND), outputs (V_{CCO} supply and V_{CCO} GND), PLL (V_{CCPLL} supply and V_{CCPLL} GND), and the LVDS input (V_{CCLVDS} supply and V_{CCLVDS} GND). The grounds are isolated by diode connections. Bypass each V_{CC}, V_{CCO}, V_{CCPLL}, and V_{CCLVDS} pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin. The outputs are powered from V_{CCO}, which accepts a 1.71V to 3.6V supply, allowing direct interface to inputs with 1.8V to 3.3V logic levels.

Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Board Layout

Separate the LVTTL/LVCMOS outputs and LVDS inputs to prevent crosstalk. A four-layer PC board with separate layers for power, ground, and signals is recommended.

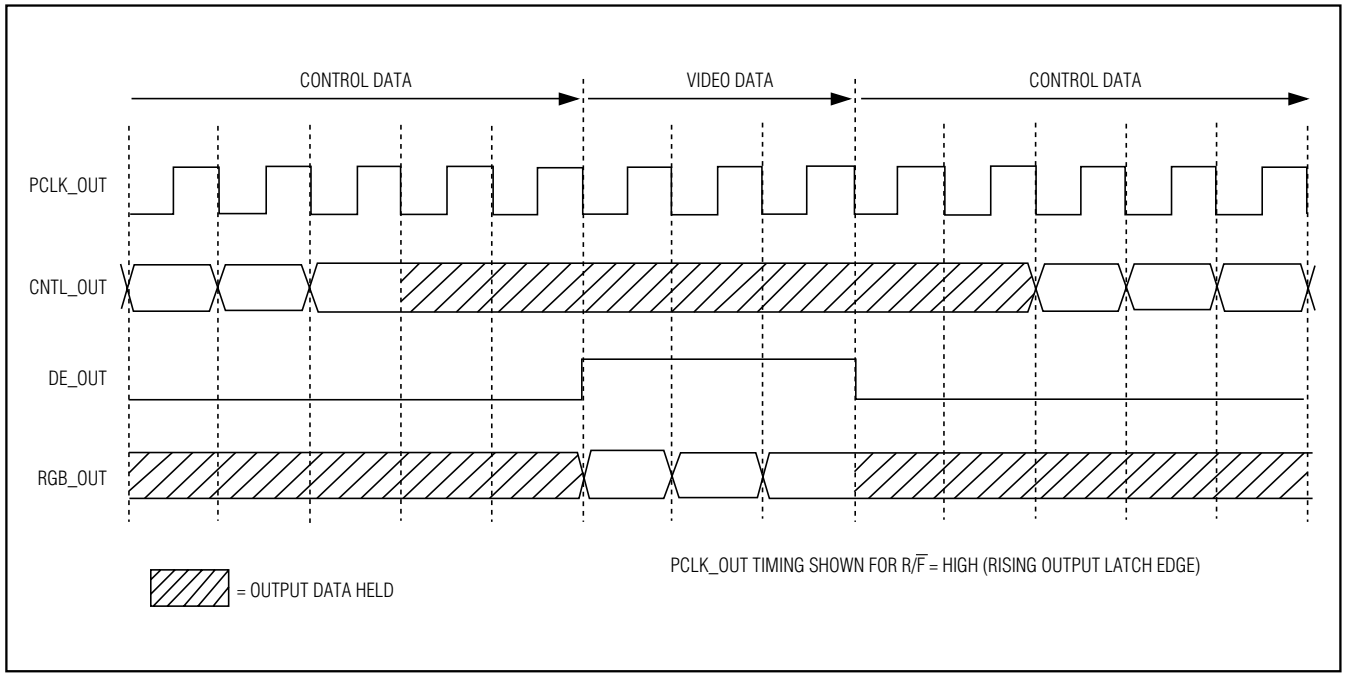


Figure 13. Output Timing

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

ESD Protection

The MAX9218 ESD tolerance is rated for the Human Body Model and ISO 10605. ISO 10605 specifies ESD tolerance for electronic systems. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 14). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 15).

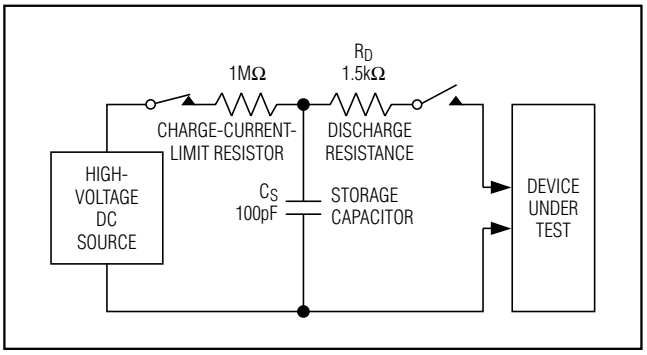


Figure 14. Human Body ESD Test Circuit

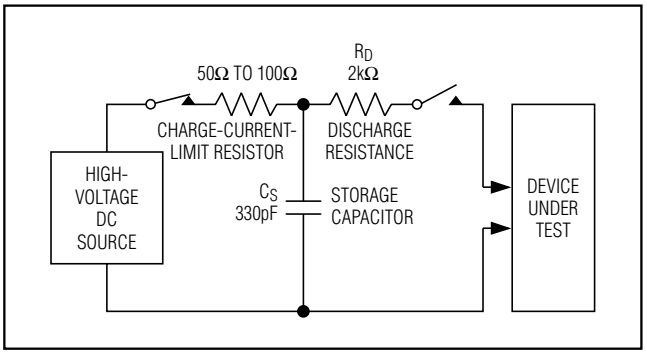


Figure 15. ISO 10605 Contact Discharge ESD Test Circuit

Chip Information

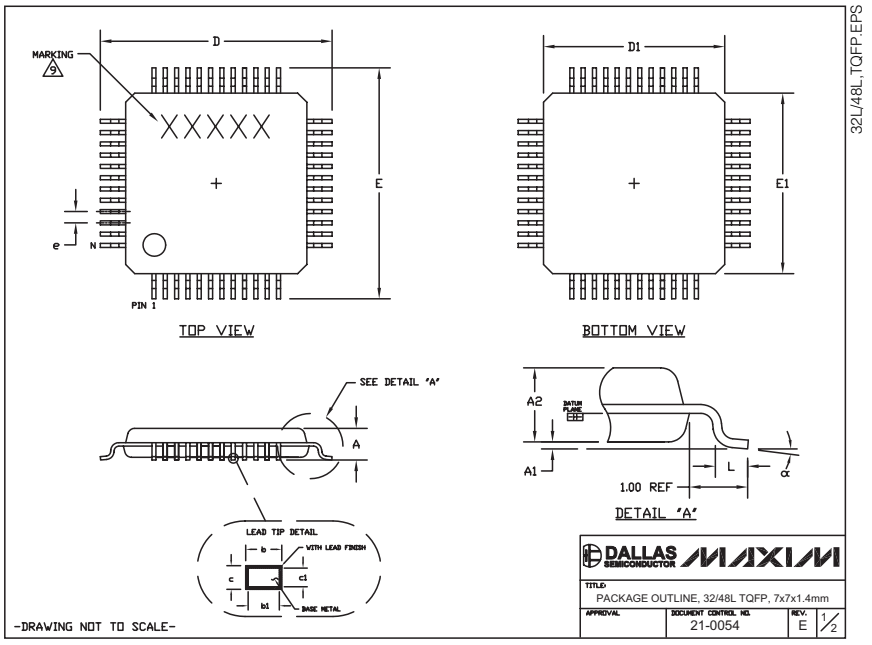
TRANSISTOR COUNT: 17,782

PROCESS: CMOS

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

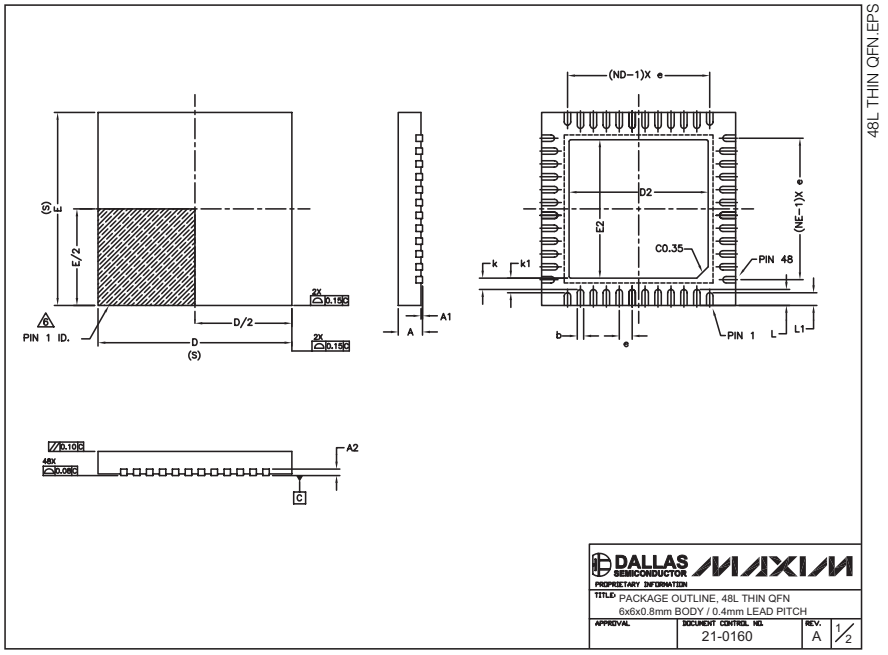
JEDEC VARIATION				
	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E_1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°

-DRAWING NOT TO SCALE-
DALLAS SEMICONDUCTOR MAXIM
TITLE
PACKAGE OUTLINE, 32/48L TQFP, 7x7x1.4mm
APPROVAL
DOCUMENT CONTROL NO.
21-0054
REV.
E
2/2

27-Bit, 3MHz-to-35MHz DC-Balanced LVDS Deserializer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER TO JEDEC MO-220.
6. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
7. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

	COMMON DIMENSIONS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.700	0.750	0.800
A1	0.000	-- --	0.050
A2		0.200 REF.	
b	0.150	0.200	0.250
D	5.900	6.000	6.100
e		0.400 TYP.	
E	5.900	6.000	6.050
k	0.250	0.350	0.450
k1	0.350	0.450	0.550
L	0.400	0.500	0.600
L1	0.300	0.400	0.500
N		48	
ND		12	
NE		12	

	EXPOSED PAD VARIATONS					
PKG. CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40