

Interleaved High-Efficiency, Dual Power-Supply Controllers for Notebook Computers

General Description

The MAX8716/MAX8717/MAX8757 are dual, step-down, interleaved, fixed-frequency, switch-mode power-supply (SMPS) controllers with synchronous rectification. They are intended for main (5V/3.3V) and I/O power generation in battery-powered systems.

Fixed-frequency operation with optimal interleaving minimizes input ripple current from the lowest input voltages up to the 26V maximum input. Optimal 40/60 interleaving allows the input voltage to go down to 8.3V before duty-cycle overlap occurs, compared to 180° out-of-phase regulators where the duty-cycle overlap occurs when the input drops below 10V.

Accurate output current limit is achieved using a sense resistor. Alternatively, power dissipation can be reduced using lossless inductor current sensing. Independent ON/OFF controls and power-good signals allow flexible power sequencing. Soft-start reduces inrush current, while soft-stop gradually ramps the output voltage down preventing negative voltage dips.

A low-noise mode maintains high light-load efficiency while keeping the switching frequency out of the audible range.

The MAX8716 is available in a 24-pin thin QFN package, and the MAX8717/MAX8757 are available in a 28-pin thin QFN package.

Applications

2 to 4 Li+ Cell Battery-Powered Devices

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Main or I/O Power Supplies

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

- ◆ Fixed 200kHz, 300kHz, or 500kHz Switching Frequency
- ◆ No Current-Sense Resistor Required
- ◆ 40/60 Optimal Interleaving
- ◆ Reduced Input-Capacitor Requirement
- ◆ 3.3V and 5V fixed or 1.0V to 5.5V Adjustable Outputs (Dual Mode™)
- ◆ 4V to 26V Input Range
- ◆ Independently Selectable PWM, Skip, and Low-Noise Mode Operation
- ◆ Soft-Start and Soft-Stop
- ◆ 2V Precision Reference with 0.75% Accuracy
- ◆ Independent Power-Good Outputs

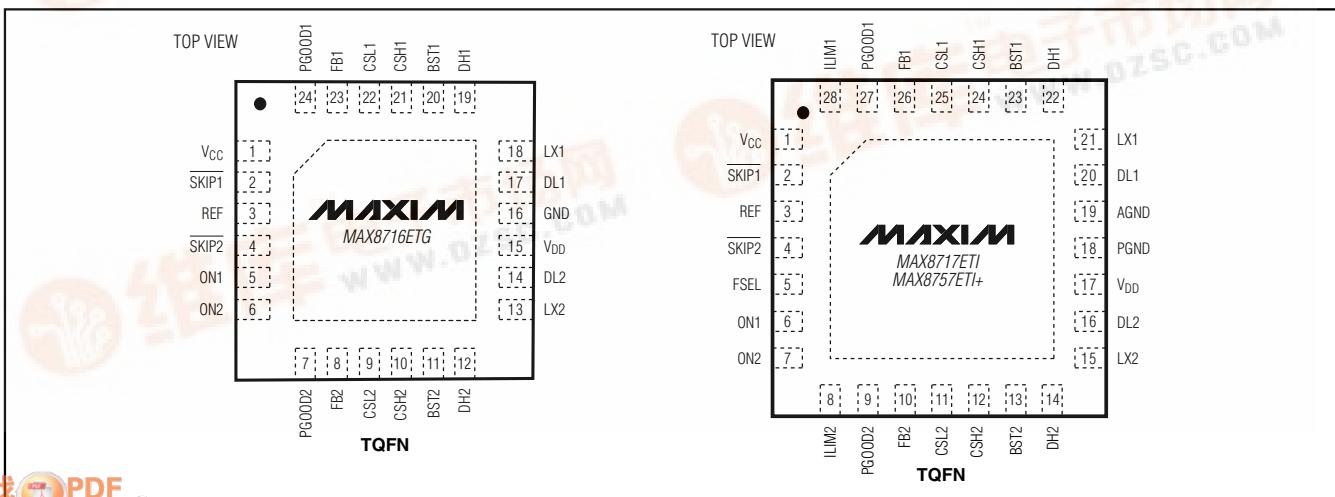
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8716ETG*	-40°C to +85°C	24 Thin QFN 4mm x 4mm
MAX8716ETG+	-40°C to +85°C	24 Thin QFN 4mm x 4mm
MAX8717ETI	-40°C to +85°C	28 Thin QFN 5mm x 5mm
MAX8717ETI+	-40°C to +85°C	28 Thin QFN 5mm x 5mm
MAX8757ETI+	-40°C to +85°C	28 Thin QFN 5mm x 5mm

+Denotes lead-free package.

*Future product—contact factory for availability.

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} , V_{CC} , $CSL1$, $CSH1$, $CSL2$, $CSH2$ to AGND	-0.3V to +6V
$ON1$, $ON2$, $\overline{SKIP1}$, $\overline{SKIP2}$, $PGOOD1$, $PGOOD2$ to AGND	-0.3V to +6V
$FB1$, $FB2$, $ILIM1$, $ILIM2$, $FSEL$ to AGND	-0.3V to +6V
REF to AGND	-0.3V to (V_{CC} + 0.3V)
$BST1$, $BST2$ to AGND	-0.3V to +36V
$LX1$ to $BST1$	-6V to +0.3V
$LX2$ to $BST2$	-6V to +0.3V
$DH1$ to $LX1$	-0.3V to (V_{B1} + 0.3V)
$DH2$ to $LX2$	-0.3V to (V_{B2} + 0.3V)
$DL1$, $DL2$ to PGND	-0.3V to (V_{DD} + 0.3V)
AGND to PGND	-0.3V to +0.3V

REF Short Circuit to AGND	Continuous
REF Current	+10mA
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
24-Pin Thin QFN 4mm x 4mm (derate 20.8mW/ $^\circ\text{C}$)	
above +70 $^\circ\text{C}$)	1666.7mW
28-Pin Thin QFN 5mm x 5mm (derate 21.3mW/ $^\circ\text{C}$)	
above +70 $^\circ\text{C}$)	1702.1mW
Operating Temperature Range	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Junction Temperature	+150 $^\circ\text{C}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$

Note 1: For the 24-pin TQFN version, AGND and PGND refer to a single pin designated GND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN} = 12\text{V}$, $FSEL = \text{REF}$, $\overline{SKIP} = 0$, $V_{ON_} = V_{ILIM_} = V_{CC} = V_{DD} = 5\text{V}$, $T_A = 0^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}			26		V
	V_{BIAS}	V_{CC} , V_{DD}	4.5		5.5	
V _{CC} Undervoltage-Lockout Threshold	V_{UVLO}	200mV typical hysteresis	V_{CC} rising	3.9	4.15	4.4
			V_{CC} falling	3.7	3.95	4.2
Quiescent Supply Current (V_{CC})	I_{CC}	CSL _— and FB _— forced above their regulation points		0.8	1.3	mA
Quiescent Supply Current (V_{DD})	I_{DD}	CSL _— and FB _— forced above their regulation points		<1	5	μA
Shutdown Supply Current (V_{CC})		ON1 = ON2 = GND		<1	5	μA
Shutdown Supply Current (V_{DD})		ON1 = ON2 = GND		<1	5	μA
MAIN SMPS CONTROLLERS						
PWM1 Output Voltage in Fixed Mode	V_{OUT1}	$V_{IN} = 6\text{V}$ to 26V, $\overline{SKIP1} = V_{CC}$, zero to full load (Note 2)	3.265	3.30	3.365	V
PWM2 Output Voltage in Fixed Mode	V_{OUT2}	$V_{IN} = 6\text{V}$ to 26V, $\overline{SKIP2} = V_{CC}$, zero to full load (Note 2)	4.94	5.00	5.09	V
Feedback Voltage in Adjustable Mode (Note 2)	$V_{FB_}$	$V_{IN} = 6\text{V}$ to 26V, FB1 or FB2, duty factor = 20% to 80%	0.990	1.005	1.020	V
		$V_{IN} = 6\text{V}$ to 26V, FB1 or FB2, duty factor = 50%	0.995	1.005	1.015	
Output-Voltage Adjust Range		Either SMPS	1.0		5.5	V
FB1, FB2 Fixed-Mode Threshold Voltage		Dual-mode comparator	1.9		2.1	V
Feedback Input Leakage Current		FB1 = 1.1V, FB2 = 1.1V	-0.1		+0.1	μA
DC Load Regulation		Either SMPS, $\overline{SKIP} = V_{CC}$, zero to full load		-0.1		%

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $FSEL = REF$, $SKIP_ = 0$, $V_{ON_} = V_{ILIM_} = V_{CC} = V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Line-Regulation Error		Either SMPS, $4V < V_{IN} < 26V$		0.03		%/V
FB_ Input Bias Current	$I_{FB_}$	$V_{FB_} = 0$ to $5.5V$	-0.1		+0.1	μA
Operating Frequency	f_{OSC}	$FSEL = GND$	170	200	230	kHz
		$FSEL = REF$ (Note 3)	270	300	330	
		$FSEL = V_{CC}$	425	500	575	
Maximum Duty Factor	D_{MAX}	$FSEL = GND$	97.5	99		%
		$FSEL = REF$ (Note 3)	97.5	99		
		$FSEL = V_{CC}$	97.5	99		
Minimum On-Time	$t_{ON(MIN)}$	(Note 4)			200	ns
SMPS1 to SMPS2 Phase Shift		SMPS2 starts after SMPS1		40		%
				144		Degrees
Soft-Start Ramp Time	t_{SSTART}	Measured from the rising edge of $ON_$ to full scale, $REF = 2V$		2		ms
Soft-Stop Ramp Time	t_{STOP}	Measured from the falling edge of $ON_$ to full scale		4		ms
CURRENT LIMIT						
ILIM_ Adjustment Range			0.5		V_{REF}	V
Current-Limit Threshold (Fixed)	$V_{LIMIT_}$	$V_{CSH_} - V_{CSL_}$, $ILIM_ = V_{CC}$ (Note 3)	45	50	55	mV
Current-Limit Threshold (Adjustable)	$V_{LIMIT_}$	$V_{CSH_} - V_{CSL_}$	$V_{ILIM_} = 2.00V$	190	200	210
			$V_{ILIM_} = 1.00V$	94	100	106
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH_} - V_{CSL_}$, $SKIP_ = ILIM_ = V_{CC}$ (Note 3)		-67	-60	-53
					-120	%
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{CSH_} - V_{CSL_}$, $SKIP_ = GND$ or REF		3		mV
Idle Mode™ Threshold	V_{IDLE}	$V_{CSH_} - V_{CSL_}$, $SKIP_ = GND$	$ILIM_ = V_{CC}$ (Note 3)	6	10	14
			With respect to current-limit threshold		20	%
Low-Noise Mode Threshold	V_{LN}	$V_{CSH_} - V_{CSL_}$, $SKIP_ = REF$	$ILIM_ = V_{CC}$ (Note 3)	2.5	5	7.5
			With respect to current-limit threshold		10	%
ILIM_ Leakage Current				0.1		μA
REFERENCE (REF)						
Reference Voltage	V_{REF}	$V_{CC} = 4.5V$ to $5.5V$, $I_{REF} = 0$	$T_A = +25^\circ C$ to $+85^\circ C$	1.985	2.00	2.015
			$T_A = 0^\circ C$ to $+85^\circ C$	1.98	2.00	2.02

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $FSEL = \text{REF}$, $\overline{\text{SKIP}}_1 = 0$, $V_{ON_} = V_{ILIM_} = V_{CC} = V_{DD} = 5V$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Load Regulation	ΔV_{REF}	$I_{REF} = 0\mu\text{A}$ to $50\mu\text{A}$			10	mV
Reference Sink Current				10		μA
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 50mV		1.8		V
FAULT DETECTION						
Output Overvoltage Trip Threshold		MAX8716/MAX8717 only	11	15	19	%
Output Overvoltage Fault-Propagation Delay	$t_{OV\text{P}}$	50mV overdrive, MAX8716/MAX8717 only		10		μs
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold	65	70	75	%
Output Undervoltage Fault-Propagation Delay	$t_{UV\text{P}}$	50mV overdrive		10		μs
Output Undervoltage-Protection Blanking Time	t_{BLANK}	From rising edge of $ON_$		6144		$1/\text{fosc}$
PGOOD_ Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%	-12.5	-10	-8.0	%
PGOOD_ Propagation Delay	$t_{PGOOD_}$	Falling edge, 50mV overdrive		10		μs
PGOOD_ Output Low Voltage		$I_{SINK} = 4\text{mA}$			0.4	V
PGOOD_ Leakage Current	$I_{PGOOD_}$	High state, PGOOD_ forced to 5.5V			1	μA
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			+160	$^\circ\text{C}$
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ - LX_ forced to 5V (Note 5)	1.5	5		Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state (Note 5)	1.7	5		Ω
		DL_, low state (Note 5)	0.6	3		
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V		2		A
DL_ Gate-Driver Source Current	I_{DL} (SOURCE)	DL_ forced to 2.5V		1.7		A
DL_ Gate-Driver Sink Current	I_{DL} (SINK)	DL_ forced to 2.5V		3.3		A
Dead Time	t_{DEAD}	DL_ rising	35			ns
		DH_ rising	26			
LX_, BST_ Leakage Current		$V_{BST_} = V_{LX_} = 26\text{V}$	<2	20		μA
INPUTS AND OUTPUTS						
Logic Input Current		ON1, ON2	-1		+1	μA
ON_ Input Voltage		Rising edge, hysteresis = 225mV	1.2	1.7	2.2	V
Tri-Level Input Logic		$\overline{\text{SKIP}}_1, \overline{\text{SKIP}}_2, \text{FSEL}$	High	$V_{CC} - 0.2$		V
			REF	1.7	2.3	
			GND		0.5	

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $FSEL = REF$, $\overline{SKIP}_1 = 0$, $V_{ON_} = V_{ILIM_} = V_{CC} = V_{DD} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		\overline{SKIP}_1 , \overline{SKIP}_2 , $FSEL$, 0V, or V_{CC}	-3		+3	μA
Input Leakage Current		I_{LIM1} , I_{LIM2} , 0V, or V_{CC}	-0.1		+0.1	μA
Input Leakage Current		$CSH_$, 0V, or V_{DD}	-0.1		+0.1	μA
Input Bias Current		$CSL_$, 0V, or V_{DD}	25	50		μA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN} = 12V$, $FSEL = REF$, $\overline{SKIP}_1 = 0$, $V_{ON_} = V_{ILIM_} = V_{CC} = V_{DD} = 5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}			26		V
	V_{BIAS}	V_{CC} , V_{DD}	4.5	5.5		
Quiescent Supply Current (V_{CC})	I_{CC}	$CSL_$ and $FB_$ forced above their regulation points		1.3		mA
Quiescent Supply Current (V_{DD})	I_{DD}	$CSL_$ and $FB_$ forced above their regulation points		5		μA
Shutdown Supply Current (V_{CC})		$ON1 = ON2 = GND$		5		μA
Shutdown Supply Current (V_{DD})		$ON1 = ON2 = GND$		5		μA
MAIN SMPS CONTROLLERS						
PWM1 Output Voltage in Fixed Mode	V_{OUT1}	$V_{IN} = 6V$ to $26V$, $\overline{SKIP}_1 = V_{CC}$, zero to full load (Note 1)	3.255	3.375		V
PWM2 Output Voltage in Fixed Mode	V_{OUT2}	$V_{IN} = 6V$ to $26V$, $\overline{SKIP}_2 = V_{CC}$, zero to full load (Note 1)	4.925	5.105		V
Feedback Voltage in Adjustable Mode	$V_{FB_}$	$V_{IN} = 6V$ to $26V$, $FB1$ or $FB2$, duty factor = 20% to 80% (Note 1)	0.987	1.023		V
Output Voltage Adjust Range		Either SMPS	1.0	5.5		V
FB1, FB2 Fixed-Mode Threshold Voltage		Dual-mode comparator	1.9	2.1		V
Operating Frequency	f_{OSC}	$FSEL = GND$	170	230		kHz
		$FSEL = REF$ (Note 3)	270	330		
		$FSEL = V_{CC}$	425	575		
Maximum Duty Factor	D_{MAX}	$FSEL = GND$	97.5			%
		$FSEL = REF$ (Note 3)	97.5			
		$FSEL = V_{CC}$	97.5			
Minimum On-Time	$t_{ON(MIN)}$	(Note 4)		200		ns
CURRENT LIMIT						
ILIM_ Adjustment Range			0.5	V_{REF}		V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $FSEL = REF$, $\overline{SKIP}_- = 0$, $V_{ON_} = V_{ILIM_} = V_{CC} = V_{DD} = 5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Limit Threshold (Fixed)	$V_{LIMIT_}$	$V_{CSH_} - V_{CSL_}$, $ILIM_ = V_{CC}$ (Note 3)		44	56	56	mV
Current-Limit Threshold (Adjustable)	$V_{LIMIT_}$	$V_{CSH_} - V_{CSL_}$	$V_{ILIM_} = 2.00V$	188	212	212	mV
			$V_{ILIM_} = 1.00V$	93	107	107	
REFERENCE (REF)							
Reference Voltage	V_{REF}	$V_{CC} = 4.5V$ to $5.5V$, $I_{REF} = 0$		1.98	2.02	2.02	V
FAULT DETECTION							
Output Overvoltage Trip Threshold		MAX8716/MAX8717 only		11	19	19	%
Output Undervoltage-Protection Trip Threshold		With respect to error-comparator threshold		65	75	75	%
PGOOD_Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1%		-12.5	-8.0	-8.0	%
PGOOD_Output Low Voltage		$I_{SINK} = 4mA$			0.4	0.4	V
GATE DRIVERS							
DH_Gate-Driver On-Resistance	R_{DH}	$BST_ - LX_$ forced to $5V$ (Note 5)			5	5	Ω
DL_Gate Driver On-Resistance	R_{DL}	$DL_$, high state (Note 5)			5	5	Ω
		$DL_$, low state (Note 5)			3	3	
INPUTS AND OUTPUTS							
ON_Input Voltage		Rising edge, hysteresis = 225mV		1.2	2.2	2.2	V
Three-Level Input Logic		$\overline{SKIP1}$, $\overline{SKIP2}$, $FSEL$	High	$V_{CC} - 0.2$			V
			REF	1.7	2.3	2.3	
			GND		0.5	0.5	

Note 2: When the inductor is in continuous conduction, the output voltage will have a DC regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple.

Note 3: Default setting for the MAX8716.

Note 4: Specifications are guaranteed by design, not production tested.

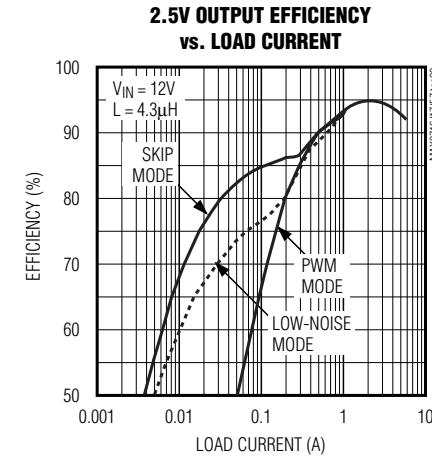
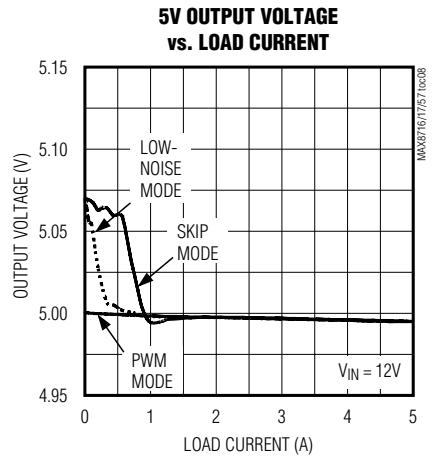
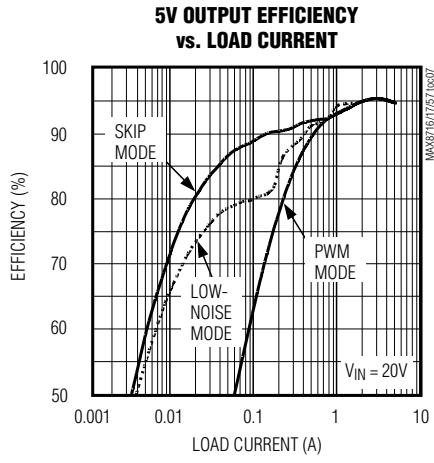
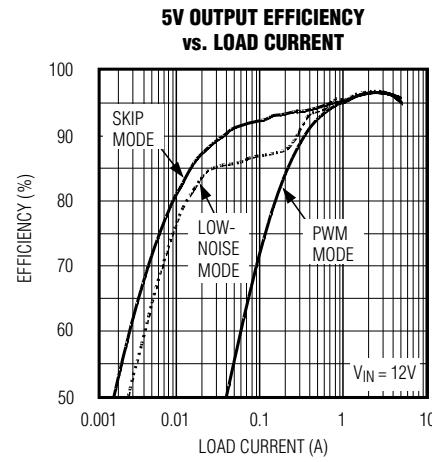
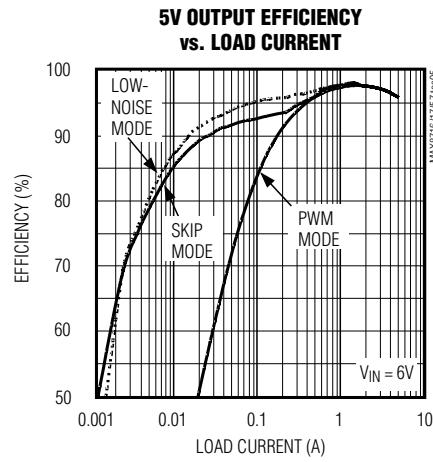
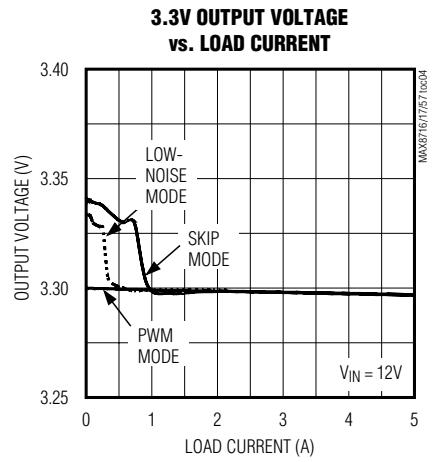
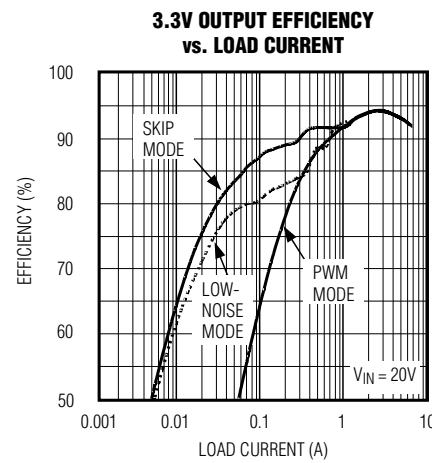
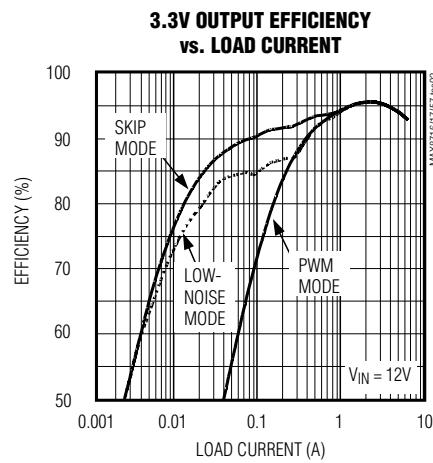
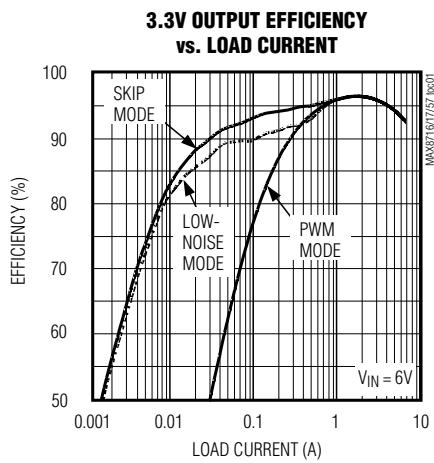
Note 5: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the thin QFN package.

Note 6: Specifications from $0^\circ C$ to $-40^\circ C$ are guaranteed by design, not production tested.

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Typical Operating Characteristics

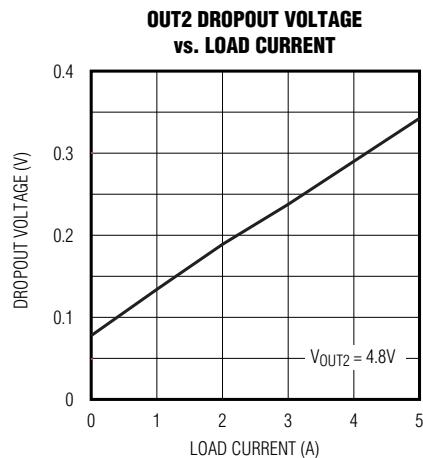
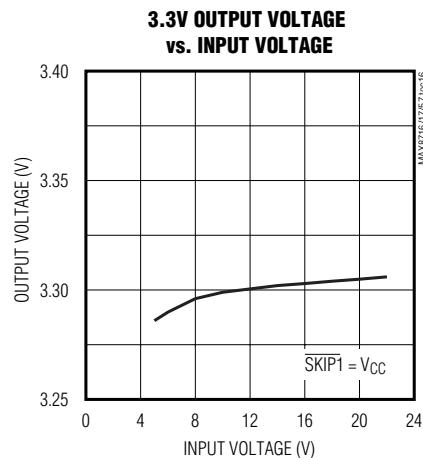
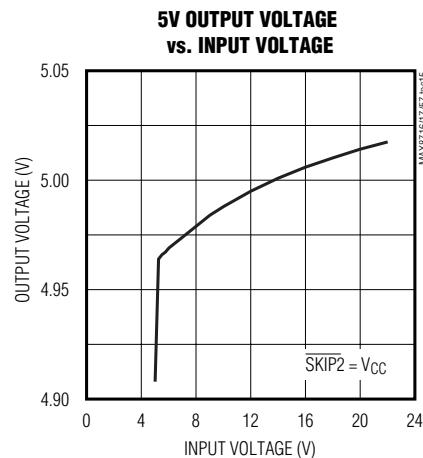
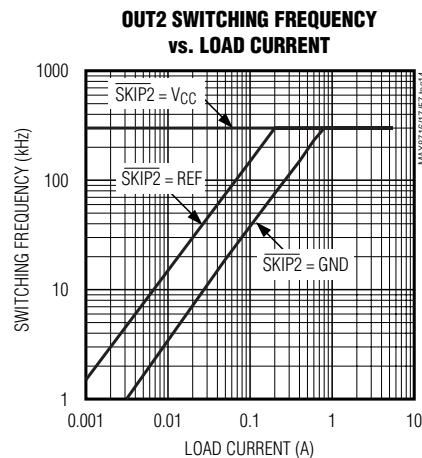
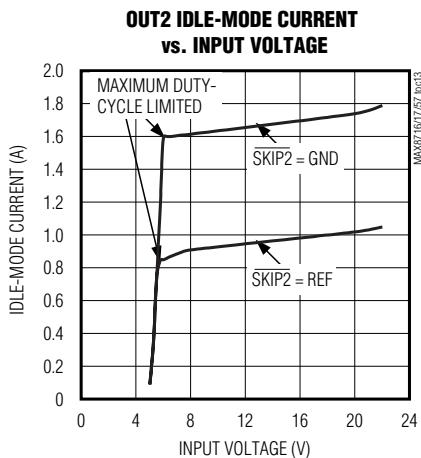
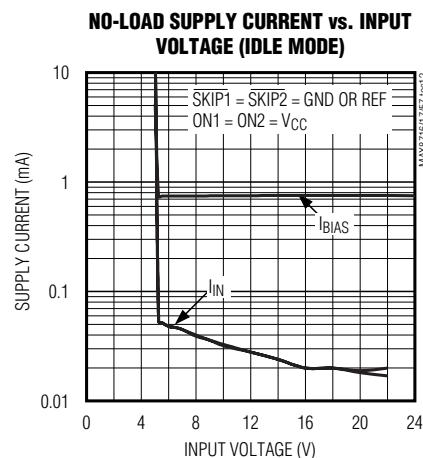
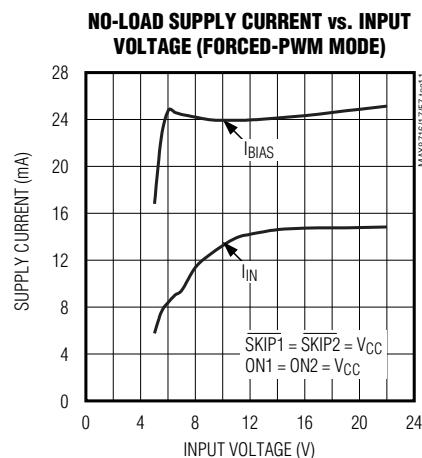
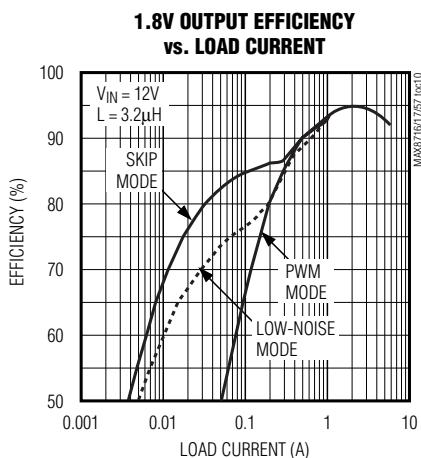
(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $\overline{SKIP}_- = GND$, $FSEL = REF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

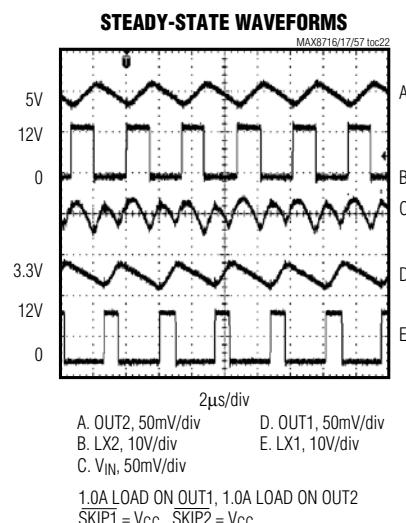
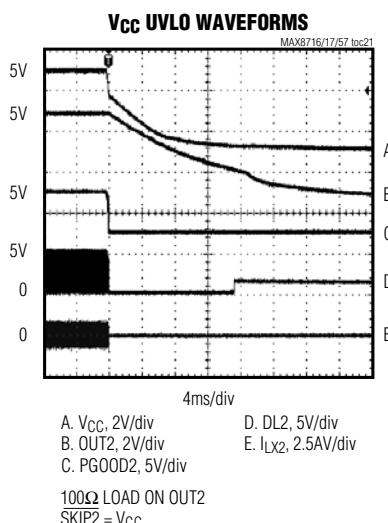
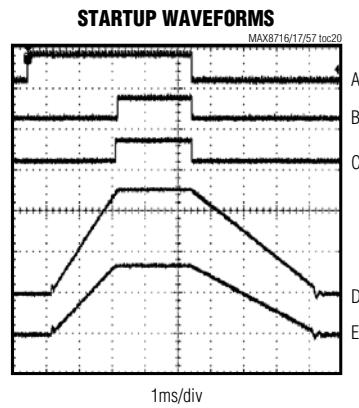
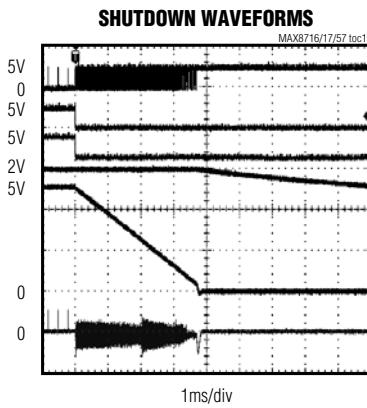
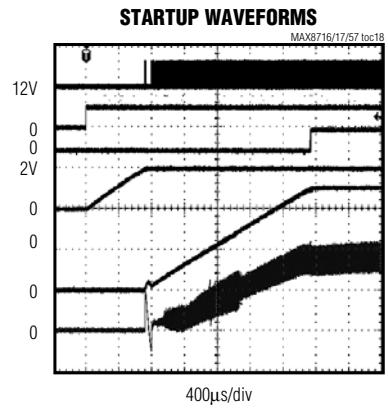
(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $\overline{SKIP}_- = GND$, $FSEL = REF$, $T_A = +25^\circ C$, unless otherwise noted.)



Interleaved High-Efficiency, Dual Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics (continued)

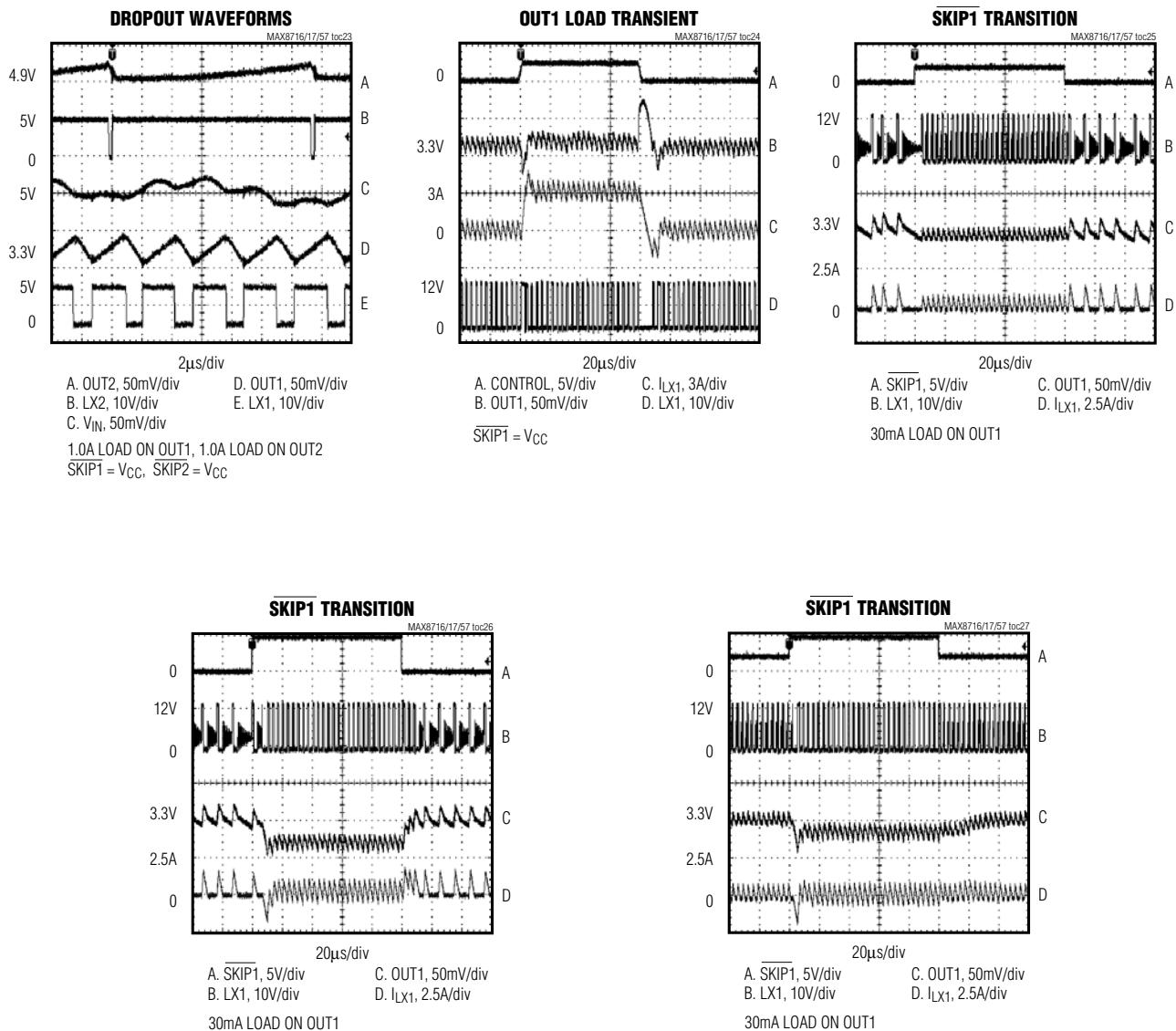
(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $\overline{SKIP}_- = GND$, $FSEL = REF$, $T_A = +25^\circ C$, unless otherwise noted.)



Interleaved High-Efficiency, Dual Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $\overline{SKIP}_- = GND$, $FSEL = REF$, $T_A = +25^\circ C$, unless otherwise noted.)



Interleaved High-Efficiency, Dual Power-Supply Controllers for Notebook Computers

Pin Description

PIN		NAME	FUNCTION
MAX8716	MAX8717/ MAX8757		
1	1	V _{CC}	Analog Supply Input. Connect to the system supply voltage (+4.5V to +5.5V) through a series 20Ω resistor. Bypass V _{CC} to AGND with a 1μF or greater ceramic capacitor.
2	2	SKIP1	Low-Noise Mode Control for SMPS1. Connect SKIP1 to GND for normal idle-mode (pulse-skipping) operation or to V _{CC} for PWM mode (fixed frequency). Connect to REF for low-noise mode.
3	3	REF	2.0V Reference Voltage Output. Bypass REF to AGND with a 0.1μF or greater ceramic capacitor. The reference can source up to 50μA. Loading REF degrades output voltage accuracy according to the REF load-regulation error (see the <i>Typical Operating Characteristics</i>). The reference shuts down when both ON1 and ON2 are low.
4	4	SKIP2	Low-Noise Mode Control for SMPS2. Connect SKIP2 to GND for normal idle-mode (pulse-skipping) operation or to V _{CC} for PWM mode (fixed frequency). Connect to REF for low-noise mode.
—	5	FSEL	Frequency Select Input. This four-level logic input sets the controller's switching frequency. Connect FSEL to V _{CC} for 500kHz, to REF for 300kHz, and to GND for 200kHz operation.
5	6	ON1	SMPS1 Enable Input. Drive ON1 high to enable SMPS1. Drive ON1 low to shut down SMPS1.
6	7	ON2	SMPS2 Enable Input. Drive ON2 high to enable SMPS2. Drive ON2 low to shut down SMPS2.
—	8	ILIM2	SMPS2 Peak Current-Limit Threshold Adjustment. Connect ILIM2 to V _{CC} to enable the default 50mV current-limit threshold. In adjustable mode, the current-limit threshold across CSH2 and CSL2 is precisely 1/10th the voltage seen at ILIM2 over a 500mV to 2.0V range. The logic threshold for switchover to the 50mV default value is approximately V _{CC} - 1V.
7	9	PGOOD2	SMPS2 Open-Drain Power-Good Output. PGOOD2 is low when SMPS2 is more than 10% below its regulation threshold, during soft-start, and in shutdown.
8	10	FB2	Feedback Input for SMPS2. Connect FB2 to V _{CC} for fixed 5V output. In adjustable mode, FB2 regulates to 1V.
9	11	CSL2	Negative Current-Sense Input for SMPS2. Connect to the negative terminal of the current-sense element. Figure 8 describes two different current-sensing options.
10	12	CSH2	Positive Current-Sense Input for SMPS2. Connect to the positive terminal of the current-sense element. Figure 8 describes two different current-sensing options.
11	13	BST2	Boost Flying Capacitor Connection for SMPS2. Connect to an external capacitor and diode as shown in Figure 1. An optional resistor in series with BST2 allows the DH2 turn-on current to be adjusted.
12	14	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2.
13	15	LX2	Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 is the lower supply rail for the DH2 high-side gate driver.

Interleaved High-Efficiency, Dual Power-Supply Controllers for Notebook Computers

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8716	MAX8717/ MAX8757		
14	16	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from PGND to V _{DD} .
15	17	V _{DD}	Supply Voltage Input for the DL_ Gate Drivers. Connect to a 5V supply.
16	—	GND	Power and Analog Ground. Connect backside pad to GND.
—	18	PGND	Power Ground
—	19	AGND	Analog Ground. Connect backside pad to AGND.
17	20	DL1	Low-Side Gate-Driver Output for SMPS1. DL1 swings from PGND to V _{DD} .
18	21	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 is the lower supply rail for the DH1 high-side gate driver.
19	22	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1.
20	23	BST1	Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor and diode as shown in Figure 1. An optional resistor in series with BST1 allows the DH1 turn-on current to be adjusted.
21	24	CSH1	Positive Current-Sense Input for SMPS1. Connect to the positive terminal of the current-sense element. Figure 8 describes two different current-sensing options.
22	25	CSL1	Negative Current-Sense Input for SMPS1. Connect to the negative terminal of the current-sense element. Figure 8 describes two different current-sensing options.
23	26	FB1	Feedback Input for SMPS1. Connect FB1 to V _{CC} for fixed 3.3V output. In adjustable mode, FB1 regulates to 1V.
24	27	PGOOD1	SMPS1 Open-Drain Power-Good Output. PGOOD1 is low when SMPS1 is more than 10% below its regulation threshold, during soft-start, and in shutdown.
—	28	ILIM1	SMPS1 Peak Current-Limit Threshold Adjustment. Connect ILIM1 to V _{CC} to enable the default 50mV current-limit threshold. In adjustable mode, the current-limit threshold across CSH1 and CSL1 is precisely 1/10th the voltage seen at ILIM1 over a 500mV to 2.0V range. The logic threshold for switchover to the 50mV default value is approximately V _{CC} - 1V.
EP	EP	EP	Exposed Pad. Connect exposed backside pad to analog ground.

Detailed Description

The MAX8716/MAX8717/MAX8757 Standard Application Circuit (Figure 1) generates the 5V/5A and 3.3V/5A typical of the main supplies in notebook computers. The input supply range is 6V to 24V. See Table 1 for component selections, while Table 2 lists the component manufacturers.

The MAX8716/MAX8717/MAX8757 contain two interleaved fixed-frequency, step-down controllers designed for low-voltage power supplies. The optimal interleaved architecture guarantees out-of-phase operation, which reduces the input capacitor ripple.

SMPS 5V Bias Supply (V_{CC} and V_{DD})

The MAX8716/MAX8717/MAX8757 switch-mode power supplies (SMPS) require a 5V bias supply in addition to the high-power input supply (battery or AC adapter). V_{DD} is the power rail for the MOSFET gate drive, and V_{CC} is the power rail for the IC. Connect the external 4.5V to 5.5V supply directly to V_{DD} and connect V_{DD} to V_{CC} through an RC filter, as shown in Figure 1. The maximum supply current required is:

$$I_{BIAS} = I_{CC} + f_{sw} (Q_{G(NL1)} + Q_{G1(NH1)} + Q_{G2(NL2)} + Q_{G2(NH2)}) = 1.3\text{mA to } 40\text{mA}$$

where I_{CC} is 1.3mA, f_{sw} is the switching frequency, and Q_G are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

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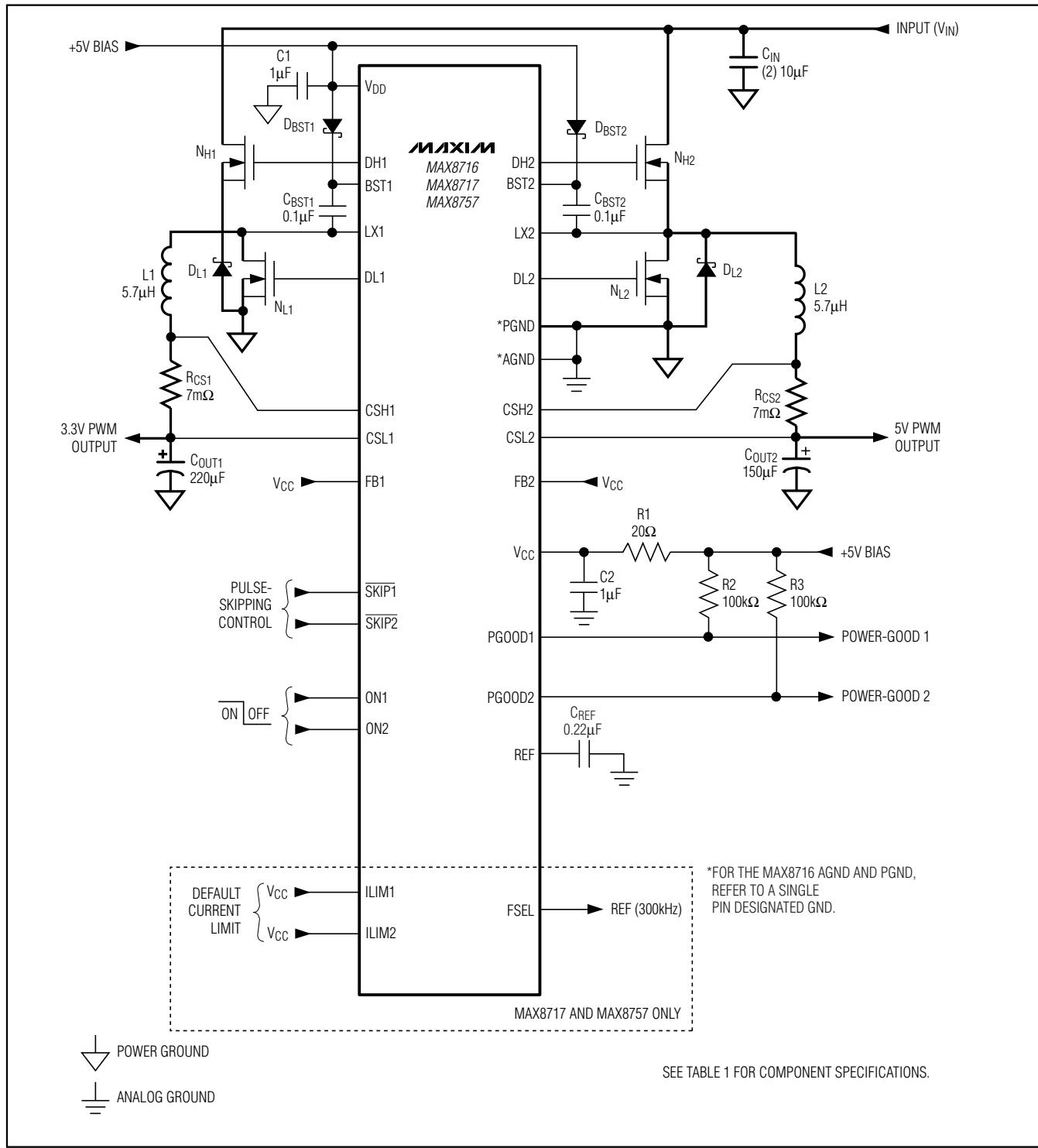


Figure 1. Standard Application Circuit

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Table 1. Component Selection for Standard Applications

COMPONENT	5A/300kHz	5A/500kHz
Input Voltage	V_{IN} = 7V to 24V	V_{IN} = 7V to 24V
C _{IN} Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM
C _{OUT1} , Output Capacitor for 3.3V Output	220µF, 4V, 25mΩ low-ESR capacitor Sanyo 4TPE220M	150µF, 4V, 25mΩ low-ESR capacitor Sanyo 4TPE150M
C _{OUT2} , Output Capacitor for 5V Output	150µF, 6.3V, 25mΩ low-ESR capacitor Sanyo 6TPE150M	100µF, 6.3V, 25mΩ low-ESR capacitor Sanyo 6TPE100M
N _H _ High-Side MOSFET	Fairchild Semiconductor FDS6612A, International Rectifier IRF7807V	Fairchild Semiconductor FDS6612A, International Rectifier IRF7807V
N _L _ Low-Side MOSFET	Fairchild Semiconductor FDS6670S, International Rectifier IRF7807VD1	Fairchild Semiconductor FDS6670S, International Rectifier IRF7807VD1
D _L _ Schottky Rectifier (If Needed)	Nihon EC21QS03L 2A, 30V, 0.45V _f	Nihon EC21QS03L 2A, 30V, 0.45V _f
L __ Inductor	5.7µH Sumida CDEP105-5R7NC	3.9µH Sumida CDRH124-3R9NC
R _{SENSE} __	7mΩ ±1%, 0.5W resistor IRC LR2010-01-R007F or Dale WSL-2010-R007F	7mΩ ±1%, 0.5W resistor IRC LR2010-01-R007F or Dale WSL-2010-R007F

Reference (REF)

The 2V reference is accurate to ±1.5% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.1µF or greater ceramic capacitor. The reference sources up to 50µA and sinks 10µA to support external loads.

SMPS Detailed Description

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. The POR circuit also ensures that the low-side drivers are driven high until the SMPS controllers are activated. The V_{CC} input undervoltage-lockout (UVLO) circuitry inhibits switching if V_{CC} is below the V_{CC} UVLO threshold.

An internal soft-start gradually increases the regulation voltage during startup to reduce the input surge currents (see the startup waveforms in the *Typical Operating Characteristics*).

SMPS Enable Controls (ON1, ON2)

ON1 and ON2 provide independent control of output soft-start and soft-shutdown. This allows flexible control of startup and shutdown sequencing. The outputs can be started simultaneously, sequentially, or independently. To provide sequential startup, connect

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX	www.avx.com
Central Semiconductor	www.centralsemi.com
Coilcraft	www.coilcraft.com
Coiltronics	www.coiltronics.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
Kemet	www.kemet.com
Panasonic	www.panasonic.com/industrial
Sanyo	www.secc.co.jp
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com

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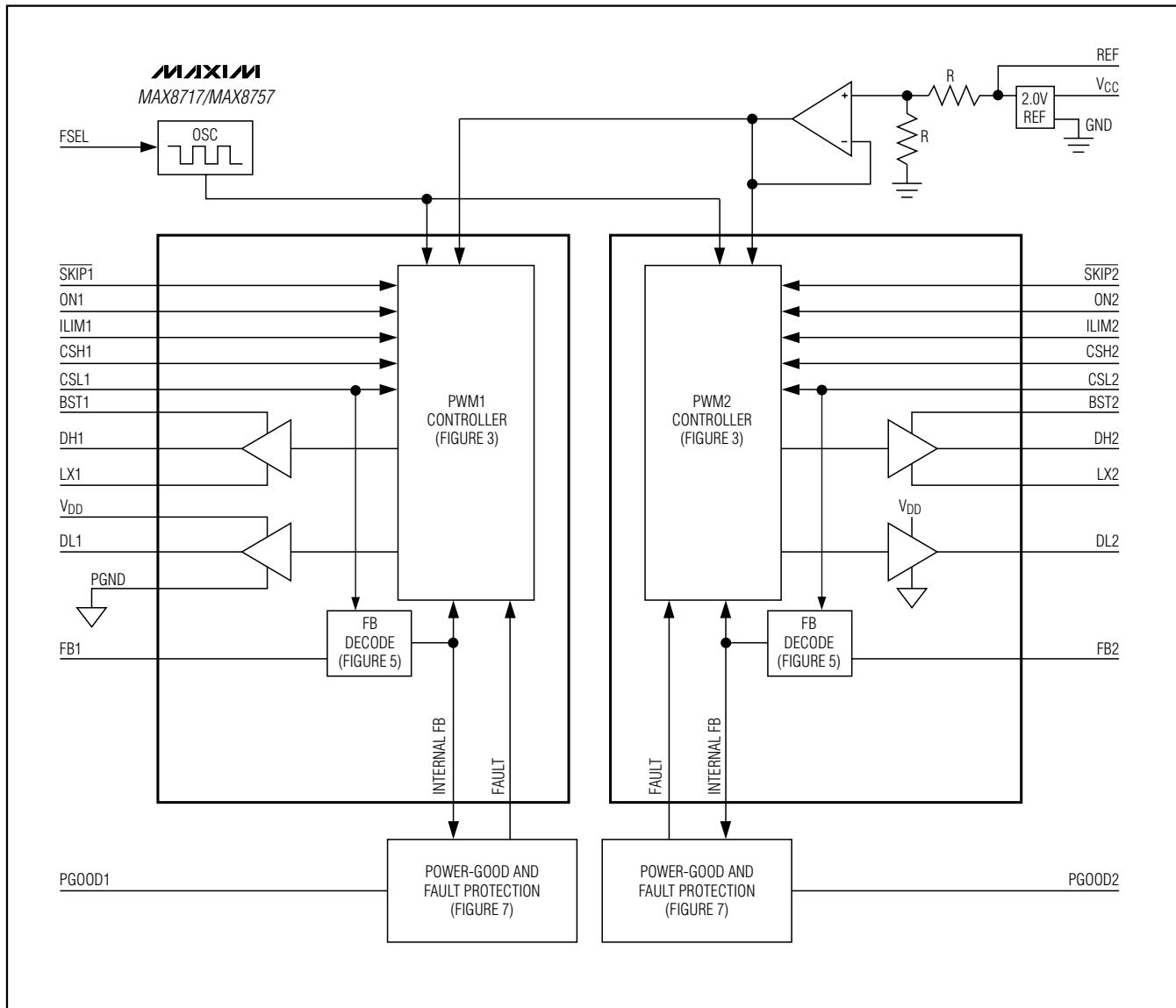


Figure 2. Functional Diagram

ON_ of one regulator to PGOOD_ of the other. For example, with ON1 connected to PGOOD2, OUT1 soft-starts after OUT2 is in regulation. Drive ON_ low to clear the overvoltage, undervoltage, and thermal fault latches.

Soft-Start and Soft-Shutdown

Soft-start begins when ON_ is driven high and REF is in regulation. During soft-start, the output is ramped up from 0V to the final set voltage in 2ms. This reduces inrush current and provides a predictable ramp-up time for power sequencing.

Soft-shutdown begins after ON_ goes low, an output undervoltage fault occurs, or a thermal fault occurs.

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The two outputs are independent. A fault at one output does not trigger shutdown of the other. During soft-shutdown the output is ramped down to 0V in 4ms, reducing negative inductor currents that can cause negative voltages on the output. At the end of soft-shutdown, DL_{_} is driven high until startup is again triggered by a rising edge of ON_{_}. The reference is turned off when both outputs have been shut down.

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums two signals: the output-voltage error signal with respect to the reference voltage and the slope-compensation ramp (Figure 3). The MAX8716/MAX8717/MAX8757 use a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it. The MAX8716/MAX8717/MAX8757 use a relatively low loop gain, allowing the use of low-cost output capacitors. The low loop gain results in the 0.1% typical load-regulation error and helps reduce the output capacitor size and cost by shifting the unity-gain crossover frequency to a lower level.

Frequency Selection (FSEL)

The FSEL input selects the PWM mode switching frequency. Table 3 shows the switching frequency based on the FSEL connection. High-frequency (500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

Forced-PWM Mode

To maintain low-noise fixed-frequency operation, drive SKIP_{_} high to put the output into forced-PWM mode. This disables the zero-crossing comparator and allows negative inductor current. During forced-PWM mode, the switching frequency remains constant and the no-load supply current is typically between 8mA and 20mA per phase, depending on external MOSFETs and switching frequency.

Light-Load Operation Control (SKIP_{_})

The MAX8716/MAX8717/MAX8757 include SKIP_{_} inputs that enable the corresponding outputs to operate in discontinuous mode. Connect SKIP_{_} to GND or REF as shown in Table 4 to enable or disable the zero-crossing comparators of either controller. When the

zero-crossing comparator is enabled, the controller forces DL_{_} low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the controller to skip pulses under light-load conditions to avoid overcharging the output. During skip mode, the VDD current consumption is reduced and efficiency is improved. During low-noise skip mode, the no-load ripple amplitude is two times smaller and the no-load switching frequency is four times higher, although the light-load efficiency is somewhat lower.

Table 3. FSEL Configuration Table

FSEL	SWITCHING FREQUENCY (kHz)
V _{CC}	500
REF	300
GND	200

Idle-Mode Current-Sense Threshold

When pulse-skipping mode is enabled, the on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle-mode current-sense threshold. Under light-load conditions, the on-time duration depends solely on the idle-mode current-sense threshold, which is 20% (SKIP_{_} = GND) of the full-load current-limit threshold set by ILIM_{_}, or the low-noise current-sense threshold, which is 10% (SKIP_{_} = REF) of the full-load current-limit threshold set by ILIM_{_}. This forces the controller to source a minimum amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until output voltage drops below the feedback threshold. Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses. Therefore, the controller regulates the valley of the output ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 4). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across CSH_{_} and CSL_{_}. Once V_{CSH} - V_{CSL} drops below the 3mV zero-crossing current-sense threshold, the comparator forces DL_{_} low (Figure 3). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical

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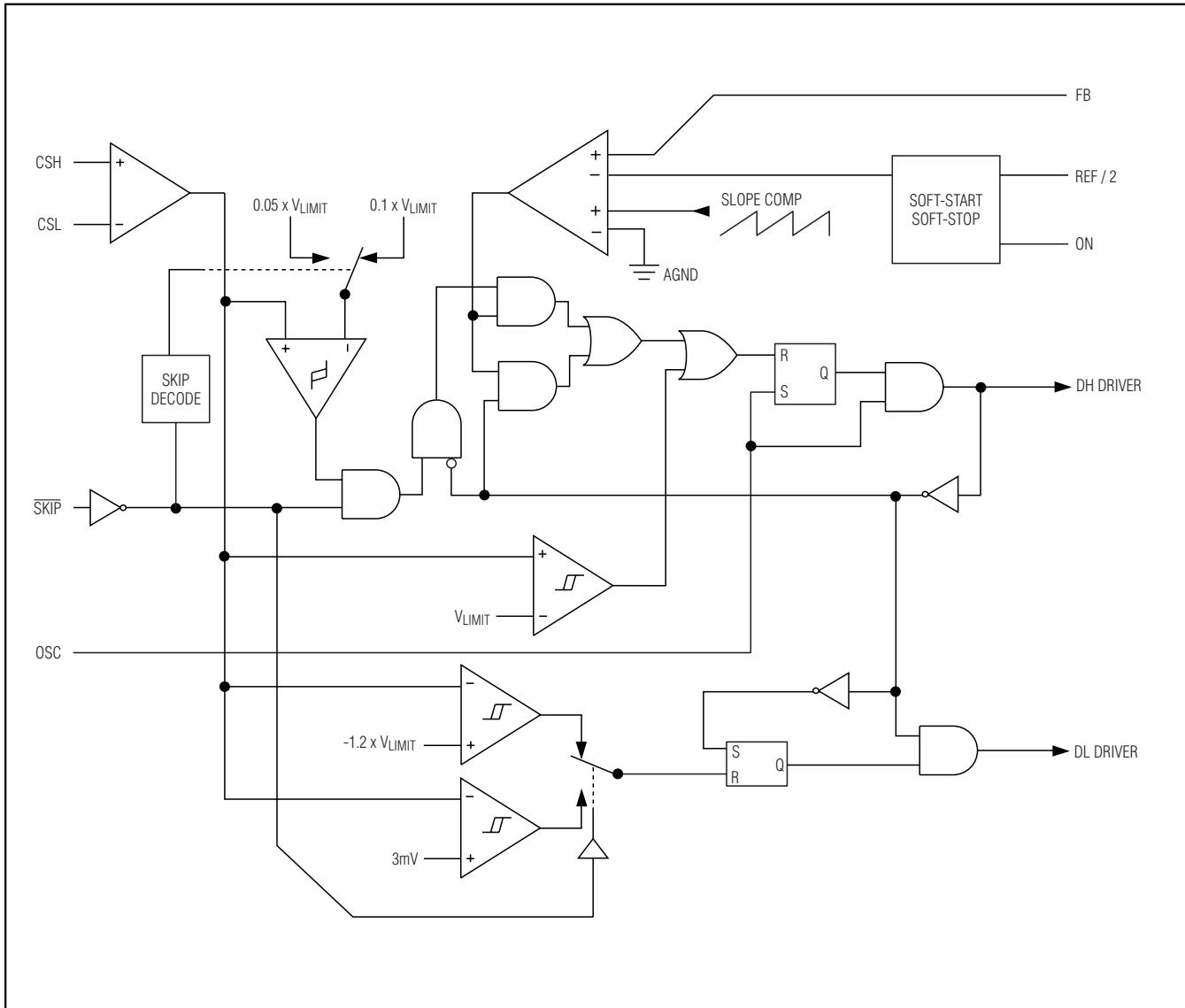


Figure 3. PWM-Controller Functional Diagram

conduction" point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is determined by:

$$I_{LOAD(SKIP)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2LV_{IN}f_{OSC}}$$

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductance. Generally, low inductance produces a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the

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Table 4. SKIP_ Configuration Table

SKIP_	MODE	COMMENTS
Vcc	Forced-PWM mode	Fixed-frequency operation. Constant output ripple voltage. Able to source and sink current.
GND	Skip mode	High efficiency at light loads. Source-only applications.
REF	Low-noise skip mode	Good efficiency at light loads. Two times smaller no-load ripple and 4 times higher frequency compared with skip mode. Source-only applications.

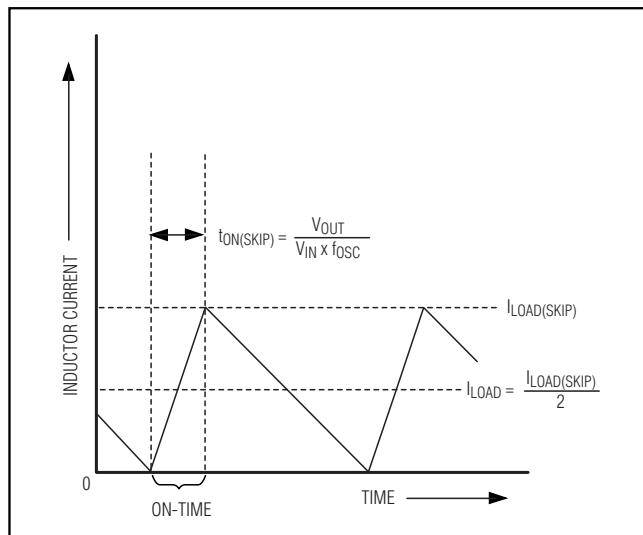


Figure 4. Pulse-Skipping/Discontinuous Crossover Point

Table 5. Operating Modes Truth Table

MODE	CONDITION	COMMENT
Power-Up	VCC UVLO	DL_ tracks VCC as VCC rises from 0V to +5V. When ON_ is low, DL_ tracks VCC as VCC falls. When ON_ is high, DL_ is forced low as VCC falls below the 3.95V (typ) falling UVLO threshold. DL_ is forced high when VCC falls below 1V (typ).
Run	ON1 or ON2 enabled	Normal operation.
Output Overvoltage (OVP) Protection	Either output > 115% of nominal level	When the overvoltage (OV) comparator trips, the faulted side sets the OV latch, forcing PGOOD_ low and DL_ high. The other controller is not affected. The OV latch is cleared by cycling Vcc below 1V or cycling the respective ON_ pin.
Output Undervoltage Protection (UVP)	Either output < 70% of nominal level, UVP is enabled 6144 clock cycles (1/fosc) after the output is enabled (ON_ going high)	When the undervoltage (UV) comparator trips, the faulted side sets the UV latch, forcing PGOOD_ low and initiating the soft-shutdown sequence by pulsing only DL_. DL_ goes high after soft-shutdown. The other controller is not affected. The UV latch is cleared by cycling Vcc below 1V or cycling the respective ON_ pin.
Shutdown	ON1 and ON2 are driven low	DL_ stays high after soft-shutdown is completed. All circuitry is shut down.
Thermal Shutdown	T _J > +160°C	Exited by POR or cycling ON1 and ON2. DL1 and DL2 remain high.

coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Output Voltage
DC output accuracy specifications in the *Electrical Characteristics* refer to the error comparator's threshold. When the inductor continuously conducts, the

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MAX8716/MAX8717/MAX8757 regulate the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM} \left(1 - \frac{ASLOPE(V_{IN} - V_{NOM})}{V_{IN}} \right) - \left(\frac{V_{RIPPLE}}{2} \right)$$

where V_{NOM} is the nominal output voltage, $ASLOPE$ equals 1%, and V_{RIPPLE} is the output ripple voltage ($V_{RIPPLE} = R_{ESR} \times \Delta I_{INDUCTOR}$ as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the MAX8716/MAX8717/MAX8757 regulate the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold. For PFM operation (discontinuous conduction), the output voltage is approximately defined by the following equation:

$$V_{OUT(PFM)} = V_{NOM} + \frac{1}{2} \left(\frac{f_{SW}}{f_{OSC}} \right) I_{IDLE} R_{ESR}$$

where V_{NOM} is the nominal output voltage, f_{OSC} is the maximum switching frequency set by the internal oscillator, f_{SW} is the actual switching frequency, and I_{IDLE} is the idle-mode inductor current when pulse skipping.

Adjustable/Fixed Output Voltages (Dual-Mode Feedback)

Connect FB1 and FB2 to V_{CC} to enable the fixed SMPS output voltages (3.3V and 5V, respectively), set by a preset, internal resistive voltage-divider connected between CSL₋ and analog ground. See Figure 5. Connect a resistive voltage-divider at FB₋ between CSL₋ and GND to adjust the respective output voltage between 1V and 5.5V. Choose R₂ (resistance from FB to AGND) to be approximately 10k Ω and solve for R₁ (resistance from OUT to FB) using the equation:

$$R_1 = R_2 \left(\frac{V_{OUT} - 1}{V_{FB} - 1} \right)$$

where $V_{FB} = 1V$ nominal.

Current-Limit Protection (ILIM₋)

The current-limit circuit uses differential current-sense inputs (CSH₋ and CSL₋) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller turns off the high-side MOSFET (Figure 3). At the next

rising edge of the internal oscillator, the PWM controller does not initiate a new cycle unless the current-sense signal drops below the current-limit threshold. The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT} / V_{IN}).

In forced-PWM mode, the MAX8716/MAX8717/MAX8757 also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately -120% of the positive current limit and tracks the positive current limit when ILIM is adjusted.

Connect ILIM₋ to V_{CC} for the 50mV default threshold, or adjust the current-limit threshold with an external resistor-divider at ILIM₋. Use a 2 μ A to 20 μ A divider current for accuracy and noise immunity. The current-limit threshold adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage equals precisely 1/10 the voltage seen at ILIM₋. The logic threshold for switchover to the 50mV default value is approximately V_{CC} - 1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CSH₋ and CSL₋. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

MOSFET Gate Drivers (DH₋, DL₋)

The DH₋ and DL₋ drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large $V_{IN} - V_{OUT}$ differential exists. The high-side gate drivers (DH₋) source and sink 2A, and the low-side gate drivers (DL₋) source 1.7A and sink 3.3A. This ensures robust gate drive for high-current applications. The DH₋ floating high-side MOSFET drivers are powered by diode-capacitor charge pumps at BST₋ (Figure 6) while the DL₋ synchronous-rectifier drivers are powered directly by the external 5V supply (V_{DD}).

Adaptive dead-time circuits monitor the DL₋ and DH₋ drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL₋ and DH₋ drivers to the MOSFET

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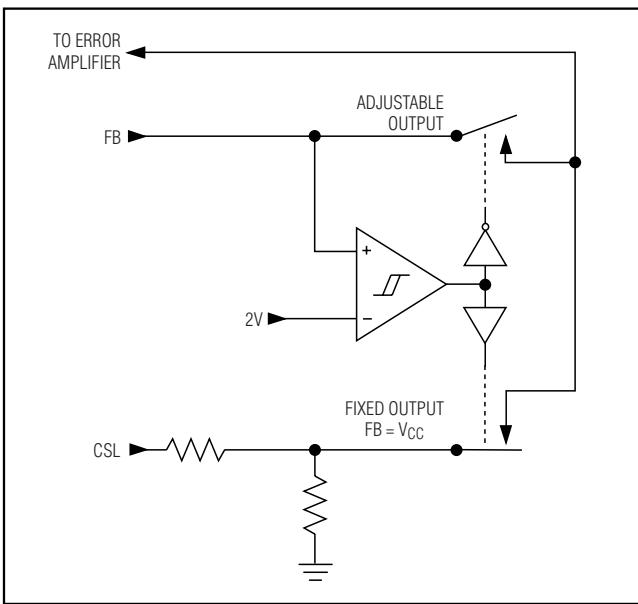


Figure 5. Dual-Mode Feedback Decoder

gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX8716/MAX8717/MAX8757 interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL_– is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL_– from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_–) quickly switches from ground to V_{IN}. Applications with high input voltages and long inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_– edges do not pull up the low-side MOSFETs gate, causing shoot-through currents. The capacitive coupling between LX_– and DL_– created by the MOSFET’s gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN} \left(\frac{C_{RSS}}{C_{ISS}} \right)$$

Variation of the threshold voltage may cause problems in marginal designs. Alternatively, adding a resistor less than 10Ω in series with BST_– may remedy the problem by increasing the turn-on time of the high-side MOSFET without degrading the turn-off time (Figure 6).

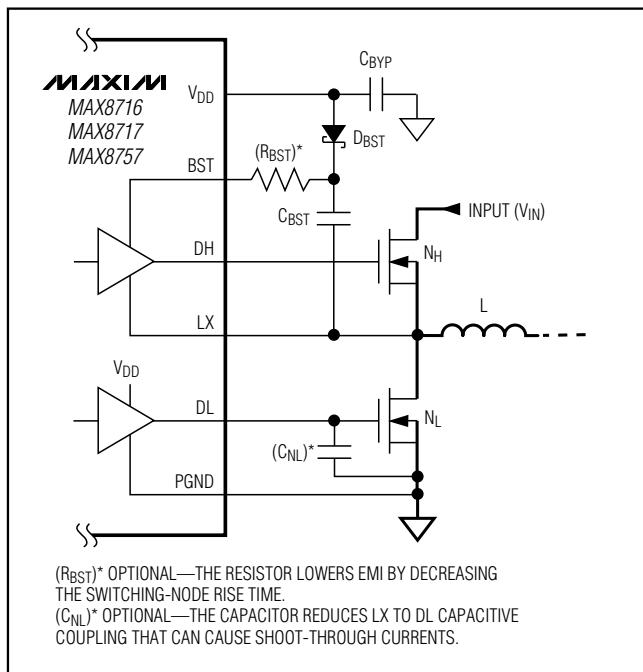


Figure 6. Optional Gate-Driver Circuitry

Power-Good Output (PGOOD_–)

PGOOD_– is the open-drain output of a comparator that continuously monitors each SMPS output voltage for overvoltage and undervoltage conditions. PGOOD_– is actively held low in shutdown (ON_– = GND), soft-start, and soft-shutdown. Once the analog soft-start terminates, PGOOD_– becomes high impedance as long as the output is above 90% of the nominal regulation voltage set by FB_–. PGOOD_– goes low once the output drops 10% below its nominal regulation point, an output overvoltage fault occurs, or ON_– is pulled low. For a logic-level PGOOD_– output voltage, connect an external pullup resistor between PGOOD_– and +5V or +3.3V. A 100kΩ pullup resistor works well in most applications.

Fault Protection

Output Overvoltage Protection (MAX8716/MAX8717 Only)

If the output voltage of either SMPS rises above 115% of its nominal regulation voltage, the corresponding controller sets its overvoltage fault latch, pulls PGOOD_– low, and forces DL_– high for the corresponding SMPS controller. The other controller is not affected. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse will blow. Cycle V_{CC} below 1V or toggle ON_– to clear the overvoltage fault latch and restart the SMPS controller.

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Output Undervoltage Protection

If the output voltage of either SMPS falls below 70% of its regulation voltage, the corresponding controller sets its undervoltage fault latch, pulls PGOOD_{_} low, and begins soft-shutdown for the corresponding SMPS controller by pulsing DL_{_}. DH_{_} remains off during the soft-shutdown sequence initiated by an undervoltage fault. The other controller is not affected. After soft-shutdown has completed, the MAX8716/MAX8717/MAX8757 force DL_{_} high and DH_{_} low. Cycle VCC below 1V or toggle ON₁ to clear the undervoltage fault latch and restart the SMPS controller.

VCC POR and UVLO

Power-on reset (POR) occurs when VCC rises above approximately 2V, resetting the fault latch and preparing the PWM for operation. VCC undervoltage-lockout (UVLO) circuitry inhibits switching, forces PGOOD_{_} low, and forces the DL_{_} gate drivers low.

If VCC drops low enough to trip the UVLO comparator while ON_{_} is high, the MAX8716/MAX8717/MAX8757 immediately force DH_{_} and DL_{_} low on both controllers. The output discharges to 0V at a rate dependent on the load and the total output capacitance. This prevents negative output voltages, eliminating the need for a Schottky diode to GND at the output.

Thermal Fault Protection

The MAX8716/MAX8717/MAX8757 feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor sets the fault latches, pulls PGOOD low, and shuts down both SMPS controllers using the soft-shutdown sequence (see the *Sort-Start and Soft-Shutdown* section). Cycle VCC below 1V or toggle ON₁ and ON₂ to clear the fault latches and restart the controllers after the junction temperature cools by 15°C.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range.** The maximum value (VIN(MAX)) must accommodate the worst-case, high AC-adapter voltage. The minimum value (VIN(MIN)) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.

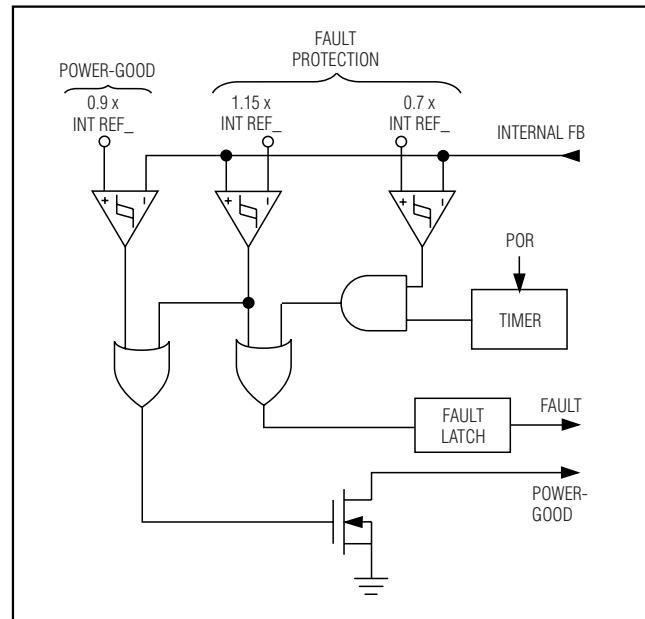


Figure 7. Power-Good and Fault Protection

- **Maximum Load Current.** There are two values to consider. The peak load current (ILOAD(MAX)) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (ILOAD) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2 . The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values

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lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse-skipping (SKIP low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}f_{OSCL}I_{LOAD(MAX)}LIR}$$

For example: $I_{LOAD(MAX)} = 5A$, $V_{IN} = 12V$, $V_{OUT} = 5V$, $f_{OSCL} = 300kHz$, 30% ripple current or $LIR = 0.3$:

$$L = \frac{5V \times (12V - 5V)}{12V \times 300kHz \times 5A \times 0.3} = 6.50\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as $1.0\mu H$, $1.5\mu H$, $2.2\mu H$, $3.3\mu H$, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}f_{OSCL}L}$$

Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

Transient Response

The inductor ripple current also impacts transient-response performance, especially at low $V_{IN} - V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The total output voltage sag is the sum of the voltage sag while the inductor is ramping up and the voltage sag before the next pulse can occur:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2}{2C_{OUT}(V_{IN} \times D_{MAX} - V_{OUT})} + \frac{\Delta I_{LOAD(MAX)}(T - \Delta T)}{C_{OUT}}$$

where D_{MAX} is maximum duty factor (see the *Electrical Characteristics*), T is the switching period ($1 / f_{OSC}$), and ΔT equals $V_{OUT} / V_{IN} \times T$ when in PWM mode, or $L \times 0.2 \times I_{MAX} / (V_{IN} - V_{OUT})$ when in skip mode. The amount of overshoot during a full-load to no-load transient due to stored inductor energy can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The peak inductor current occurs at $I_{LOAD(MAX)}$ plus half the ripple current; therefore:

$$I_{LIMIT} > I_{LOAD(MAX)} + \left(\frac{\Delta I_{INDUCTOR}}{2} \right)$$

where I_{LIMIT} equals the minimum current-limit threshold voltage divided by the current-sense resistance (R_{SENSE}). For the 50mV default setting, the minimum current-limit threshold is 50mV.

Connect $ILIM_{-}$ to V_{CC} for a default 50mV current-limit threshold. In adjustable mode, the current-limit threshold is precisely 1/10 the voltage seen at $ILIM_{-}$. For an adjustable threshold, connect a resistive divider from REF to analog ground (GND) with $ILIM_{-}$ connected to the center tap. The external 500mV to 2V adjustment range corresponds to a 50mV to 200mV current-limit threshold. When adjusting the current limit, use 1% tolerance resistors and a divider current of approximately $10\mu A$ to prevent significant inaccuracy in the current-limit tolerance.

The current-sense method (Figure 8) and magnitude determines the achievable current-limit accuracy and power loss. Typically, higher current-sense limits provide tighter accuracy, but also dissipate more power. Most applications employ a current-limit threshold (V_{LIM}) of 50mV to 100mV, so the sense resistor can be determined by:

$$R_{SENSE_{-}} = V_{LIM} / I_{LIM_{-}}$$

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 8a.

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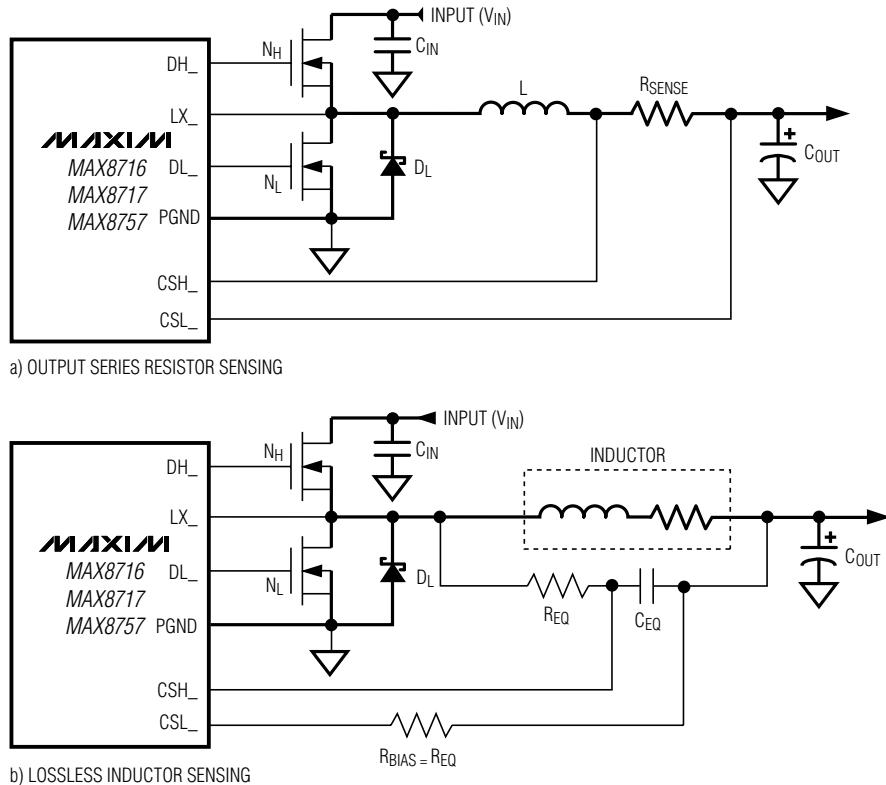


Figure 8. Current-Sense Configurations

This configuration constantly monitors the inductor current, allowing accurate current-limit protection.

Alternatively, high-power applications that do not require highly accurate current-limit protection may reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 8b) with an equivalent time constant:

$$\frac{L}{R_L} = C_{EQ} \times R_{EQ}$$

where R_L is the inductor's series DC resistance. In this configuration, the current-sense resistance equals the inductor's DC resistance ($R_{SENSE} = R_L$). Use the worst-case inductance and R_L values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault protection. When using high-capacitance, low-ESR capacitors (see the *Output-Capacitor Stability Considerations* section), the filter capacitor's ESR dominates the output voltage ripple. So the output capacitor's size depends on the maximum ESR required to meet the output-voltage-ripple ($V_{RIPPLE(P-P)}$) specifications:

$$V_{RIPPLE(P-P)} = R_{SENSE} \times I_{LOAD(MAX)} \times L_{IR}$$

In idle mode, the inductor current becomes discontinuous, with peak currents set by the idle-mode current-

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sense threshold ($V_{IDLE} = 0.2V_{LIMIT}$). In idle mode, the no-load output ripple can be determined as follows:

$$V_{RIPPLE(P-P)} = \frac{V_{IDLE}R_{ESR}}{R_{SENSE}}$$

The actual capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, polymers, and other electrolytics). When using low-capacity filter capacitors, such as ceramic capacitors, size is usually determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). However, low-capacity filter capacitors typically have high-ESR zeros that may effect the overall stability (see the *Output-Capacitor Stability Considerations* section).

Output-Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The boundary of instability is given by the following equation:

$$f_{ESR} \leq \frac{f_{SW}}{\pi}$$

where:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 25kHz. In the design example used for inductor selection, the ESR needed to support 25mVp-p ripple is $25mV/1.5A = 16.7m\Omega$. One 220 μ F/4V Sanyo polymer (TPE) capacitor provides 15m Ω (max) ESR. This results in a zero at 48kHz, well within the bounds of stability.

For low input-voltage applications where the duty cycle exceeds 50% ($V_{OUT} / V_{IN} \geq 50\%$), the output ripple voltage should not be greater than twice the internal slope-compensation voltage:

$$V_{RIPPLE} \leq 0.02 \times V_{OUT}$$

where V_{RIPPLE} equals $\Delta I_{INDUCTOR} \times R_{ESR}$. The worst-case ESR limit occurs when $V_{IN} = 2 \times V_{OUT}$, so the

above equation can be simplified to provide the following boundary condition:

$$R_{ESR} \leq 0.04 \times L \times f_{OSC}$$

Do not put high-value ceramic capacitors directly across the feedback sense point without taking precautions to ensure stability. Large ceramic capacitors can have a high-ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the feedback sense point, which should be as close as possible to the inductor.

Unstable operation manifests itself in two related but distinctly different ways: short/long pulses or cycle skipping resulting in a lower switching frequency. Instability occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering too early or skipping a cycle. Cycle skipping is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. For an out-of-phase regulator, the total RMS current in the input capacitor is a function of the load currents, the input currents, the duty cycles, and the amount of overlap as defined in Figure 9.

The 40/60 optimal interleaved architecture of the MAX8716/MAX8717/MAX8757 allows the input voltage to go as low as 8.3V before the duty cycles begin to overlap. This offers improved efficiency over a regular 180° out-of-phase architecture where the duty cycles begin to overlap below 10V. Figure 9 shows the input-capacitor RMS current vs. input voltage for an application that requires 5V/5A and 3.3V/5A. This shows the improvement of the 40/60 optimal interleaving over 50/50 interleaving and in-phase operation.

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For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents typical of systems with a mechanical switch or connector in series with the input. Choose a capacitor that has less than 10°C temperature rise at the RMS input current for optimal reliability and lifetime.

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H . Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H . If V_{IN} does not vary over a wide range, optimum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D²PAK), and is reasonably priced. Ensure that the MAX8716/MAX8717/MAX8757 DL_{gate} driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power MOSFET Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD(N_H \text{ RESISTIVE}) = \frac{V_{OUT}}{V_{IN}} (I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching

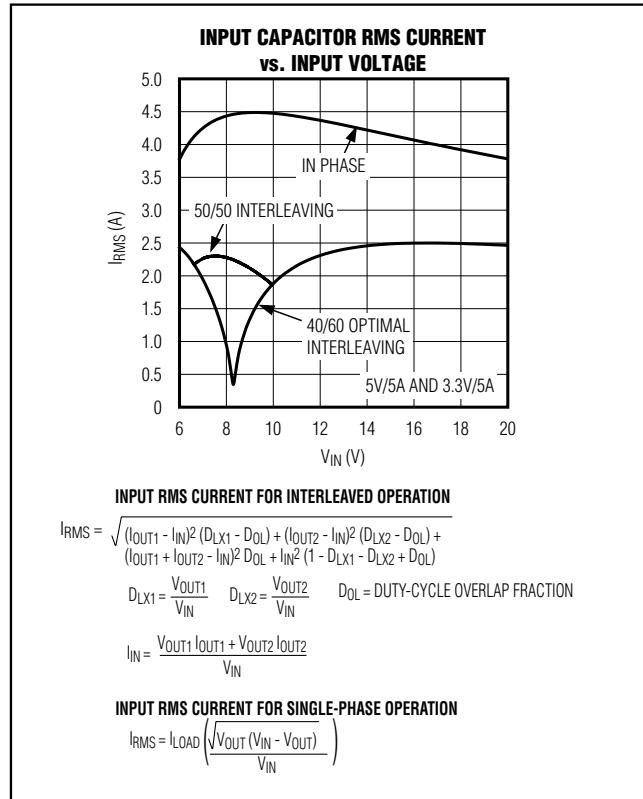


Figure 9. Input RMS Current

losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H :

$$PD(N_H \text{ SWITCHING}) = \left(\frac{V_{IN(MAX)} I_{LOAD} f_{SW}}{\eta_{TOTAL}} \right) \left(\frac{Q_{G(SW)}}{I_{GATE}} \right) + \frac{C_{OSS} V_{IN}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}^2$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

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Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied, due to the squared term in the switching-loss equation ($C \times V_{IN}^2 \times f_{SW}$). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(N_L \text{ RESISTIVE}) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}} \right) \right] (I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy-overload conditions that are greater than $I_{LOAD(MAX)}$ but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT} - \left(\frac{\Delta I_{INDUCTOR}}{2} \right)$$

where I_{LIMIT} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward-voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3rd of the load current. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1 μ F ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1 μ F. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{Q_{GATE}}{200mV}$$

where Q_{GATE} is the total gate charge specified in the high-side MOSFET's data sheet. For example, assume the FDS6612A n-channel MOSFET is used on the high side. According to the manufacturer's data sheet, a single FDS6612A has a maximum gate charge of 13nC ($V_{GS} = 5V$). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{13nC}{100mV} = 0.065\mu F$$

Selecting the closest standard value, this example requires a 0.1 μ F ceramic capacitor.

Applications Information

Duty-Cycle Limits

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by the maximum duty-cycle specification (see the *Electrical Characteristics* table). For the best dropout performance, use the slowest switching-frequency setting (200kHz, $FSEL = GND$). However, keep in mind that the transient performance gets worse as the step-down regulators approach the dropout voltage, so bulk output capacitance must be added (see the voltage sag and soar equations in the *Design Procedure* section). The absolute point of dropout occurs when the inductor current ramps down during the off-time (Δt_{DOWN}) as much as it ramps up during the on-time (Δt_{UP}). This results in a minimum operating voltage defined by the following equation:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + h \left(\frac{1}{D_{MAX}} - 1 \right) (V_{OUT} + V_{DIS})$$

where V_{CHG} and V_{DIS} are the parasitic voltage drops in the charge and discharge paths, respectively. A reasonable minimum value for h is 1.5, while the absolute minimum input voltage is calculated with $h = 1$.

Maximum Input Voltage

The MAX8716/MAX8717/MAX8757 controller includes a minimum on-time specification, which determines the maximum input operating voltage that maintains the selected switching frequency (see the *Electrical Characteristics* table). Operation above this maximum input voltage results in pulse-skipping operation, regardless of the operating mode selected by $SKIP$. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse, effectively skipping a cycle. This allows the controller to maintain regulation

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above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT} \left(\frac{1}{f_{OSC} t_{ON(MIN)}} \right)$$

where f_{OSC} is the switching frequency selected by FSEL.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 10). If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single $m\Omega$ of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSH_{-} and CSL_{-} directly across the current-sense resistor ($R_{SENSE_{-}}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.

- Route high-speed switching nodes (BST_{-} , LX_{-} , DH_{-} , and DL_{-}) away from sensitive analog areas (REF_{-} , FB_{-} , CSH_{-} , CSL_{-}).

Layout Procedure

- 1) Place the power components first, with ground terminals adjacent (N_L source, C_{IN} , $C_{OUT_{-}}$, and D_L anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
- 2) Mount the controller IC adjacent to the low-side MOSFET, preferably on the back side opposite N_L and N_H to keep LX_{-} , GND , DH_{-} , and the DL_{-} gate-drive lines short and wide. The DL_{-} and DH_{-} gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC) to keep the driver impedance low and for proper adaptive dead-time sensing.
- 3) Group the gate-drive components (BST_{-} diode and capacitor and LDO5 bypass capacitor) together near the controller IC.
- 4) Make the DC-DC controller ground connections as shown in Figures 1 and 10. This diagram can be viewed as having two separate ground planes: power ground, where all the high-power components go; and an analog ground plane for sensitive analog components. The analog ground plane and power ground plane must meet only at a single point directly at the IC.
- 5) Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Chip Information

TRANSISTOR COUNT: 5879

PROCESS: BiCMOS

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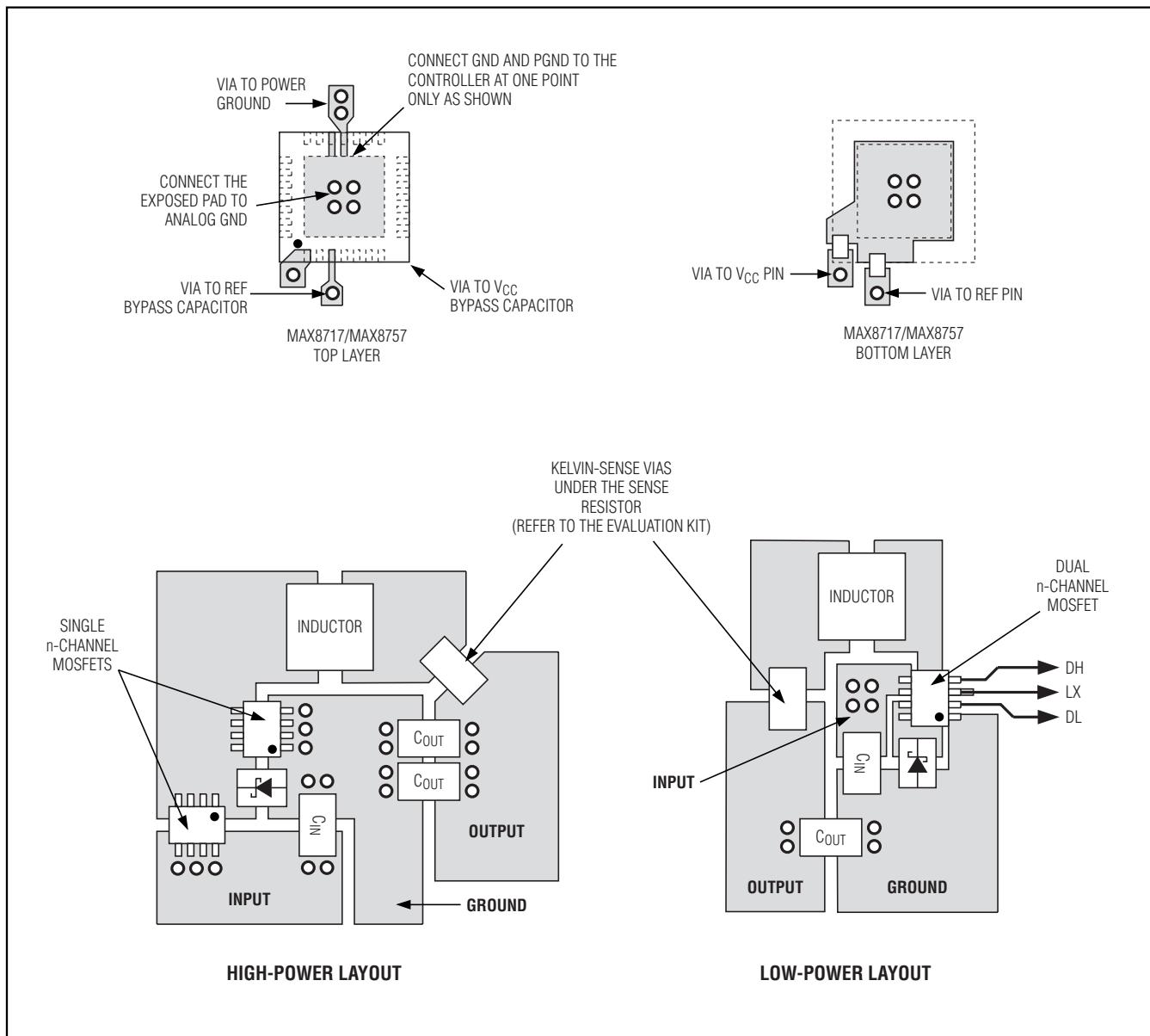
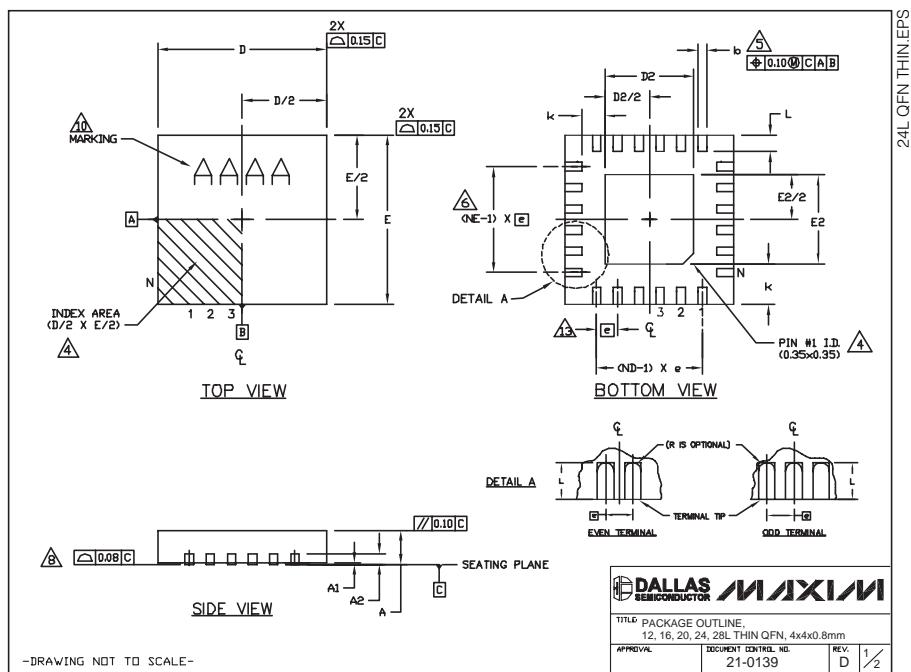


Figure 10. PC Board Layout Example

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS												EXPOSED PAD VARIATIONS											
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4			PKG	D2		E2		DOWN BOND ALLOWED		
REF.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	CODES	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	
A2	0.25	0.26	0.27	0.25	0.26	0.27	0.25	0.26	0.27	0.25	0.26	0.27	0.25	0.26	0.27	T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25	T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	
e	0.60	BSC.	0.65	BSC.	0.60	BSC.	0.65	BSC.	0.60	0.65	BSC.	0.60	0.65	BSC.	0.60	T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	
k	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	0.25	T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	
N	12	-	16	-	20	-	24	-	28	-	-	-	-	-	T2044-4	1.95	2.10	2.25	1.95	2.10	2.25		
ND	3	-	4	-	5	-	6	-	7	-	-	-	-	-	T2444-1	2.45	2.60	2.63	2.45	2.60	2.63		
NE	3	-	4	-	5	-	6	-	7	-	-	-	-	-	T2444-2	1.95	2.10	2.25	1.95	2.10	2.25		
Wdec	VGG	-	VGGC	-	WGDD-1	-	WGDD-2	-	WGGE	-	-	-	-	-	T2444-3	2.45	2.60	2.63	2.45	2.60	2.63		
Var.	-	-	-	-	-	-	-	-	-	-	-	-	-	-	T2444-4	2.45	2.60	2.63	2.45	2.60	2.63		
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	T2844-1	2.50	2.60	2.70	2.50	2.60	2.70		

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEED 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ± 0.05 .

DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM					
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm					
APPROVAL	DOCUMENT CONTROL NO.	REV.	D	2	/2
21-0139					

