19-3439; Rev 0; 10/04

EVALUATION KIT AVAILABLE

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

General Description

The MAX6872/MAX6873 EEPROM-configurable, multivoltage supply sequencers/supervisors monitor several voltage detector inputs and four general-purpose logic inputs. The MAX6872/MAX6873 feature programmable outputs for highly configurable power-supply sequencing applications. The MAX6872 features six voltage detector inputs and eight programmable outputs, while the MAX6873 features four voltage detector inputs and five programmable outputs. Manual reset and margin disable inputs offer additional flexibility.

All voltage detectors offer two configurable thresholds for undervoltage/overvoltage or dual undervoltage detection. One high voltage input (IN1) provides detector threshold voltages from +2.5V to +13.2V in 50mV increments, or from +1.25V to +7.625V in 25mV increments. A bipolar input (IN2) provides detector threshold voltages from ±2.5V to ±15.25V in 50mV increments, or from ±1.25V to ±7.625V in 25mV increments. Positive inputs (IN3–IN6) provide detector threshold voltages from +1V to +5.5V in 20mV increments, or from +0.5V to +3.05V in 10mV increments.

Programmable output stages control power-supply sequencing or system resets/interrupts. Programmable output options include: active-high, active-low, open-drain, weak pullup, push-pull, and charge pump. Programmable timing delay blocks configure each output to wait between 25µs and 1600ms before deasserting. A fault register logs the condition that caused each output to assert (undervoltage, overvoltage, manual reset, etc.).

An SMBus™-/I²C™-compatible, serial data interface programs and communicates with the configuration EEPROM, the configuration registers, the internal 4kb user EEPROM, and the fault registers of the MAX6872/MAX6873.

The MAX6872/MAX6873 are available in a 7mm x 7mm x 0.8mm 32-pin thin QFN package and operate over the extended -40°C to +85°C temperature range.

Applications

Telecommunications/Central Office Systems
Networking Systems
Servers/Workstations
Base Stations
Storage Equipment
Multimicroprocessor/Voltage Systems

Pin Configurations, Typical Operating Circuit, and Selector Guide appear at end of data sheet.

Features

- **Six (MAX6872) or Four (MAX6873) Configurable Input Voltage Detectors**
  - **One High Voltage Input (+1.25V to +7.625V or +2.5V to +13.2V Thresholds)**
  - **One Bipolar Voltage Input (±1.25V to ±7.625V or ±2.5V to ±15.25V Thresholds)**
  - **Four (MAX6872) or Two (MAX6873) Positive Voltage Inputs (+0.5V to +3.05V or +1V to +5.5V Thresholds)**
- **Four General-Purpose Logic Inputs**
- **Two Configurable Watchdog Timers**
- **Eight (MAX6872) or Five (MAX6873) Programmable Outputs**
  - **Active-High, Active-Low, Open-Drain, Weak Pullup, Push-Pull, Charge-Pump**
  - **Timing Delays from 25µs to 1600ms**
- **Margining Disable and Manual Reset Controls**
- **4kb Internal User EEPROM**
  - **Endurance: 100,000 Erase/Write Cycles**
  - **Data Retention: 10 Years**
- **I²C/SMBus-Compatible Serial Configuration/Communication Interface**
- **±1% Threshold Accuracy**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX6872ETJ	-40°C to +85°C	32 Thin QFN	T3277-2
MAX6873ETJ	-40°C to +85°C	32 Thin QFN	T3277-2

SMBus is a trademark of Intel Corp.

Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associate Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
IN3–IN6, ABP, SDA, SCL, A0, A1, GPI1–GPI4, MR, MARGIN, PO5–PO8 (MAX6872), PO3–PO5 (MAX6873).....-0.3V to +6V
IN1, PO1–PO4 (MAX6872), PO1–PO2 (MAX6873)...-0.3V to +14V
IN2.....-20V to +20V
DBP .....-0.3V to +3V
Input/Output Current (all pins).....±20mA

Continuous Power Dissipation (T_A = +70°C)
32-Pin 7mm x 7mm Thin QFN (derate 33.3mW/°C above +70°C).....2667mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 3)	V_{IN1}	Voltage on IN1 to ensure the device is fully operational, IN3–IN6 = GND		4.0		13.2	V
	V_{IN3} to V_{IN6}	Voltage on any one of IN3–IN6 to ensure the device is fully operational, IN1 = GND		2.7		5.5	
IN1 Supply Voltage (Note 3)	V_{IN1P}	Minimum voltage on IN1 to guarantee that the device is powered through IN1				6.5	V
Undervoltage Lockout	V_{UVLO}	Minimum voltage on one of IN3–IN6 to guarantee the device is EEPROM configured.				2.5	V
Supply Current	I_{CC}	V_{IN1} = +13.2V, IN2–IN6 = GND, no load			1.2	1.5	mA
		Writing to configuration registers or EEPROM, no load			1.3	2	mA
Threshold Range	V_{TH}	V_{IN1} (50mV increments)		2.5		13.2	V
		V_{IN1} (25mV increments)		1.250		7.625	
		V_{IN2} (50mV increments)		±2.50		±15.25	
		V_{IN2} (25mV increments)		±1.250		±7.625	
		V_{IN3}–V_{IN6} (20mV increments)		1.0		5.5	
		V_{IN3}–V_{IN6} (10mV increments)		0.50		3.05	
Threshold Accuracy		IN1–IN6 positive, $V_{IN\_}$ falling	T_A = +25°C	-1.0		+1.0	%
			T_A = -40°C to +85°C	-1.5		+1.5	
		-15.25V V_{IN2} -5V, V_{IN2} falling	T_A = +25°C	-1.5		+1.5	
			T_A = -40°C to +85°C	-2		+2	
		-5V V_{IN2} 0, V_{IN2} falling	T_A = +25°C	-75		+75	mV
			T_A = -40°C to +85°C	-100		+100	
Threshold Hysteresis	$V_{TH-HYST}$				0.3		% V_{TH}
Reset Threshold Temperature Coefficient	V_{TH}/°C				10		ppm/°C
Threshold-Voltage Differential Nonlinearity	V_{TH} DNL			-1		+1	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN1 Input Leakage Current	I_{LIN1}	For V_{IN1} < the highest of V_{IN3}–V_{IN6}			100	140	µA
IN2 Input Impedance	R_{IN2}			160	230	320	k
IN3–IN6 Input Impedance	R_{IN3} to R_{IN6}	V_{IN1} > 6.5V		70	100	145	k
Power-Up Delay	t_{PU}	V_{ABP} V_{UVLO}				3.5	ms
IN_ to PO_ Delay	t_{DPO}	$V_{IN\_}$ falling or rising, 100mV overdrive			25		µs
PO_ Timeout Period	t_{RP}	Register contents (Table 23)	000		25		µs
			001	1.406	1.5625	1.719	ms
			010	5.625	6.25	6.875	
			011	22.5	25	27.5	
			100	45	50	55	
			101	180	200	220	
			110	360	400	440	
			111	1440	1600	1760	
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Output Low (Note 3)	V_{OL}	V_{ABP} +2.5V, I_{SINK} = 500µA				0.3	V
		V_{ABP} +4.0V, I_{SINK} = 2mA				0.4	
PO5–PO8 (MAX6872), PO3–PO5 (MAX6873) Output Low (Note 3)	V_{OL}	V_{ABP} +2.5V, I_{SINK} = 1mA				0.3	V
		V_{ABP} +4.0V, I_{SINK} = 4mA				0.4	
PO1–PO8 Output Initial Pulldown Current	I_{PD}	V_{ABP} V_{UVLO}, $V_{PO\_}$ = 0.8V			10	40	µA
PO1–PO8 Output Open-Drain Leakage Current	I_{LKG}	Output high impedance		-1		+1	µA
PO1–PO8 Output Pullup Resistance, Weak Pullup Selected	R_{PU}	$V_{PO\_}$ = 2V		6.6	10	15	k
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Turn-On Time, Charge Pump Selected (Note 4)	t_{ON}	$C_{PO\_}$ = 1500pF, V_{ABP} = +3.3V, $V_{PO\_}$ = +7.8V		0.5	1.5	3.0	ms
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Turn-Off Time, Charge Pump Selected	t_{OFF}	$C_{PO\_}$ = 1500pF, V_{ABP} = +3.3V, $V_{PO\_}$ = +0.5V			30		µs
PO1–PO4 (MAX6872), PO1–PO2 (MAX6873) Output High, Charge Pump Selected (Notes 3, 4)	V_{OHCP}	With respect to V_{ABP}, $I_{PO\_}$ < 100nA			5.5		V
		With respect to V_{ABP}, $I_{PO\_}$ < 1µA		4.0	5.0	6.0	
PO5–PO8 (MAX6872), PO3–PO5 (MAX6873) Output High, Push-Pull Selected (Note 3)	V_{OH}	Any one of V_{IN3}–V_{IN6} +2.7V, I_{SOURCE} = 10mA, output pulled up to the same IN_		1.5			V
		Any one of V_{IN3}–V_{IN6} +2.7V, I_{SOURCE} = 1mA, output pulled up to the same IN_		0.8 x $V_{IN\_}$			
		Any one of V_{IN3}–V_{IN6} +4.5V, I_{SOURCE} = 2mA, output pulled up to the same IN_		0.8 x $V_{IN\_}$			

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MR, MARGIN, GPI_ Input Voltage	V_{IL}					0.8	V
	V_{IH}			1.4			
MR Input Pulse Width	t_{MR}			1			µs
MR Glitch Rejection					100		ns
MR to PO_ Delay	t_{DMR}				2		µs
MR to V_{DBP} Pullup Current	I_{MR}	V_{MR} = +1.4V		5	10	15	µA
MARGIN to V_{DBP} Pullup Current	I_{MARGIN}	V_{MARGIN} = +1.4V		5	10	15	µA
GPI_ to PO_ Delay	$t_{DGPI\_}$				200		ns
GPI_ Pulldown Current	$I_{GPI\_}$	$V_{GPI\_}$ = +0.8V		5	10	15	µA
Watchdog Input Pulse Width	t_{WDI}	GPI_ configured as a watchdog input		50			ns
Watchdog Timeout Period	t_{WD}	Register contents (Table 26)	000	5.625	6.25	6.875	ms
			001	22.5	25	27.5	
			010	90	100	110	
			011	360	400	440	
			100	1.44	1.6	1.76	s
			101	5.76	6.4	7.04	
			110	23.04	25.6	28.16	
			111	92.16	102.4	112.64	
SERIAL INTERFACE LOGIC (SDA, SCL, A0, A1)							
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input High Voltage	V_{IH}			2.0			V
Input Leakage Current	I_{LKG}			-1		+1	µA
Output Voltage Low	V_{OL}	I_{SINK} = 3mA				0.4	V
Input/Output Capacitance	$C_{I/O}$				10		pF

TIMING CHARACTERISTICS

(IN1 = GND, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 2)						
Serial Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Bus-Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Data-In Setup Time	$t_{SU:DAT}$		100			ns
Data-In Hold Time	$t_{HD:DAT}$		0		900	ns
Receive SCL/SDA Minimum Rise Time	t_R	(Note 5)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Rise Time	t_R	(Note 5)		300		ns
Receive SCL/SDA Minimum Fall Time	t_F	(Note 5)		20 + 0.1 x C_{BUS}		ns
Receive SCL/SDA Maximum Fall Time	t_F	(Note 5)		300		ns
Transmit SDA Fall Time	t_F	C_{BUS} = 400pF	20 + 0.1 x C_{BUS}		300	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 6)		50		ns
EEPROM Byte Write Cycle Time	t_{WR}	(Note 7)			11	ms

Note 1: Specifications guaranteed for the stated global conditions. The device also meets the parameters specified when 0 < V_{IN1} < +6.5V, and at least one of V_{IN3} through V_{IN6} is between +2.7V and +5.5V, while the remaining V_{IN3} through V_{IN6} are between 0 and +5.5V.

Note 2: Device may be supplied from any one of IN_, except IN2.

Note 3: The internal supply voltage, measured at ABP, equals the maximum of IN3–IN6 if V_{IN1} = 0, or equals +5.4V if V_{IN1} > +6.5V. For +4V < V_{IN1} < +6.5V and V_{IN3} through V_{IN6} > +2.7V, the input that powers the device cannot be determined.

Note 4: 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 5: C_{BUS} = total capacitance of one bus line in pF. Rise and fall times are measured between 0.1 x V_{BUS} and 0.9 x V_{BUS}.

Note 6: Input filters on SDA, SCL, A0, and A1 suppress noise spikes < 50ns.

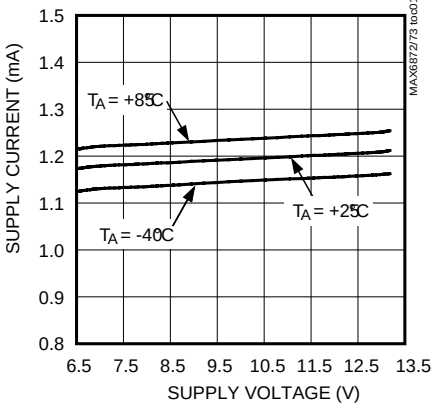
Note 7: An additional cycle is required when writing to configuration memory for the first time.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

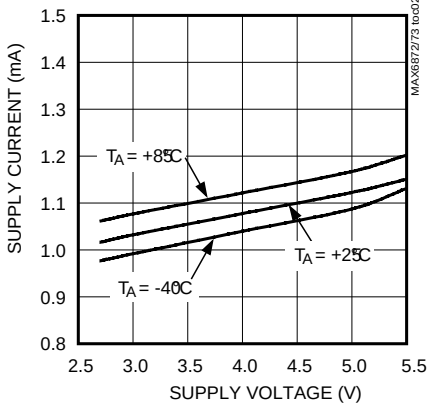
Typical Operating Characteristics

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, T_A = +25°C, unless otherwise noted.)

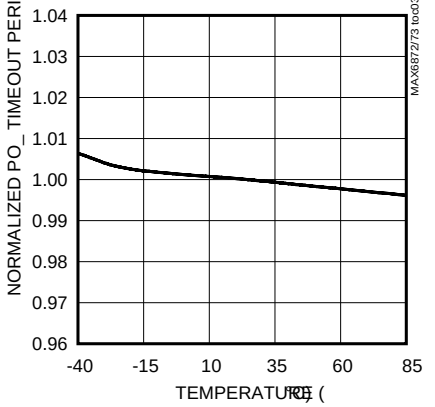
SUPPLY CURRENT vs. SUPPLY VOLTAGE (IN1)



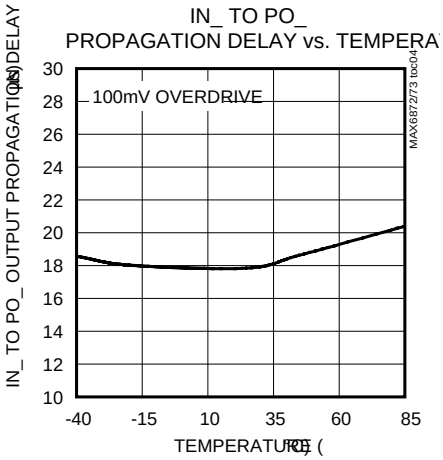
SUPPLY CURRENT vs. SUPPLY VOLTAGE (IN3—IN6)



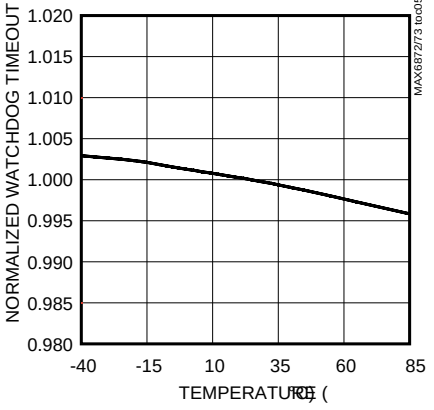
NORMALIZED PO_ TIMEOUT PERIOD vs. TEMPERATURE



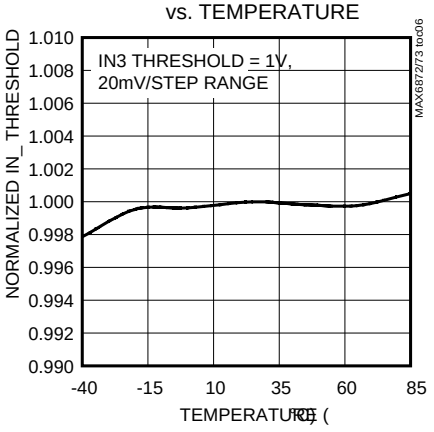
IN_ TO PO_ PROPAGATION DELAY vs. TEMPERATURE



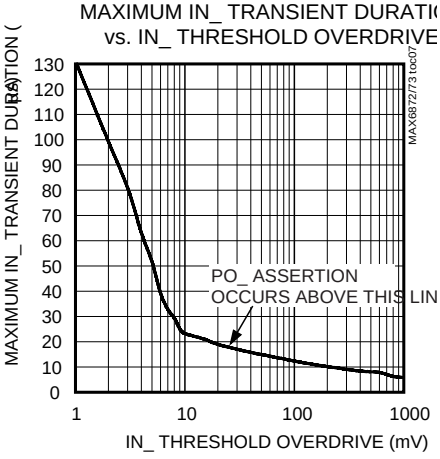
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



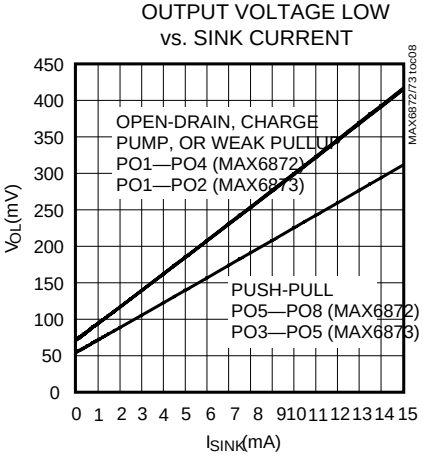
NORMALIZED IN_ THRESHOLD vs. TEMPERATURE



MAXIMUM IN_ TRANSIENT DURATION vs. IN_ THRESHOLD OVERDRIVE



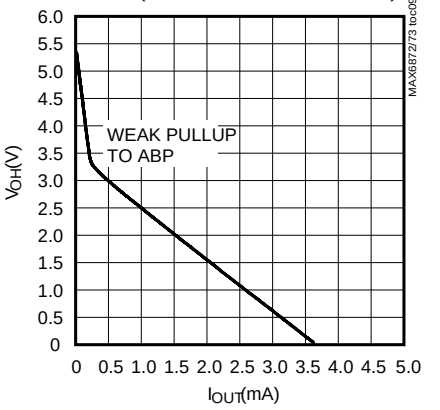
OUTPUT VOLTAGE LOW vs. SINK CURRENT



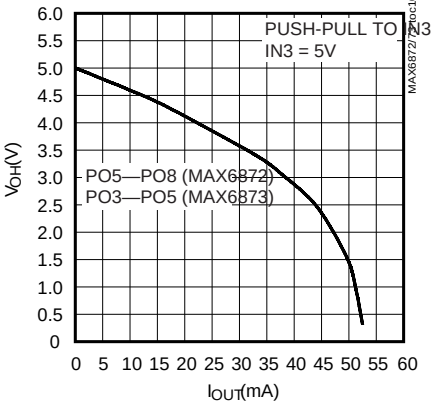
Typical Operating Characteristics (continued)

(V_{IN1} = +6.5V to +13.2V, V_{IN2} = +10V, V_{IN3}–V_{IN6} = +2.7V to +5.5V, GPI_ = GND, MARGIN = MR = DBP, T_A = +25°C, unless otherwise noted.)

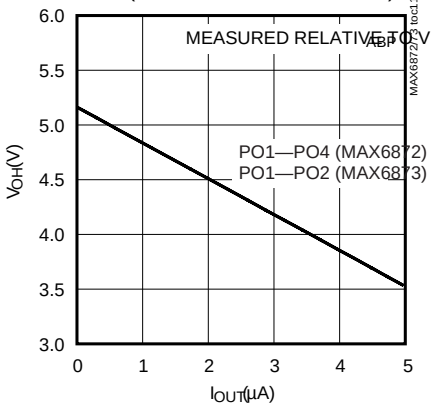
OUTPUT VOLTAGE HIGH vs. SOURCE (
(WEAK PULLUP OUTPUT)



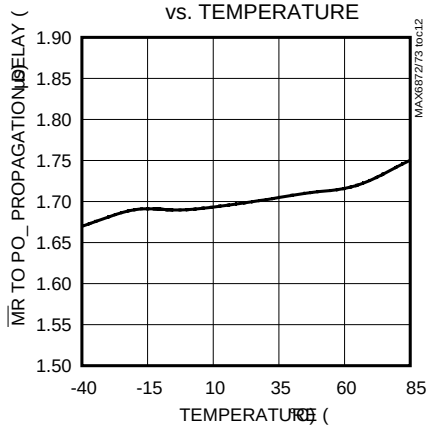
OUTPUT VOLTAGE HIGH vs. SOURCE (
(PUSH-PULL OUTPUT)



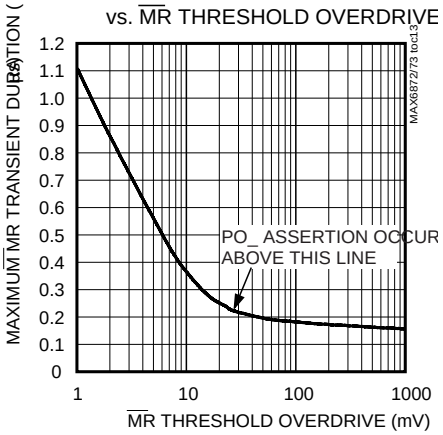
OUTPUT VOLTAGE HIGH vs. SOURCE CU
(CHARGE-PUMP OUTPUT)



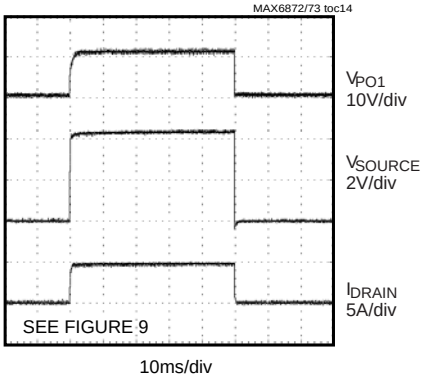
MR TO PO_ PROPAGATION DELA
vs. TEMPERATURE



MAXIMUM MR TRANSIENT DURATI
vs. MR THRESHOLD OVERDRIVE



FET (IRF7811W)
TURN-ON WITH CHARGE PUMP



Pin Description

PIN		NAME	FUNCTION
MAX6872	MAX6873		
1	3	PO2	Programmable Output 2. Configurable, active-high, active-low, open-drain, weak pullup, or charge-pump output. PO2 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO2 assumes its programmed conditional output state when ABP exceeds UVLO.
2	5	PO3	Programmable Output 3. Configurable, active-high, active-low, open-drain, weak pullup (MAX6872), push-pull (MAX6873), or charge-pump (MAX6872) output. PO3 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO3 assumes its programmed conditional output state when ABP exceeds UVLO.
3	6	PO4	Programmable Output 4. Configurable, active-high, active-low, open-drain, weak pullup (MAX6872), push-pull (MAX6873), or charge-pump (MAX6872) output. PO4 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO4 assumes its programmed conditional output state when ABP exceeds UVLO.
4	4	GND	Ground
5	7	PO5	Programmable Output 5. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO5 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO5 assumes its programmed conditional output state when ABP exceeds UVLO.
6	—	PO6	Programmable Output 6. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO6 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO6 assumes its programmed conditional output state when ABP exceeds UVLO.
7	—	PO7	Programmable Output 7. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO7 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO7 assumes its programmed conditional output state when ABP exceeds UVLO.
8	—	PO8	Programmable Output 8. Configurable, active-high, active-low, open-drain, weak pullup, or push-pull output. PO8 pulls low with a 10µA internal current sink for 1V < V_{ABP} < V_{UVLO}. PO8 assumes its programmed conditional output state when ABP exceeds UVLO.
9, 10, 23, 24	1, 8, 9, 10, 23–26, 32	N.C.	No Connection. Not internally connected.
11	11	MARGIN	Margin Input. Configure MARGIN to either assert PO_ into a programmed state or to hold PO_ in its existing state when driving MARGIN low (see Table 7). Leave MARGIN unconnected or connect to DBP if unused. MARGIN overrides MR if both assert at the same time. MARGIN is internally pulled up to DBP through a 10µA current source.
12	12	MR	Manual Reset Input. Configure MR to either assert PO_ into a programmed state or to have no effect on PO_ when driving MR low (see Table 6). Leave MR unconnected or connect to DBP if unused. MR is internally pulled up to DBP through a 10µA current source.
13	13	SDA	Serial Data Input/Output (Open-Drain). SDA requires an external pullup resistor.
14	14	SCL	Serial Clock Input. SCL requires an external pullup resistor.
15	15	A0	Address Input 0. Address inputs allow up to four MAX6872/MAX6873 connections on one common bus. Connect A0 to GND or to the serial interface power supply.
16	16	A1	Address Input 1. Address inputs allow up to four MAX6872/MAX6873 connections on one common bus. Connect A1 to GND or to the serial interface power supply.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX6872	MAX6873		
17	17	GPI4	General-Purpose Logic Input 4. An internal 10µA current source pulls GPI4 to GND. Configure GPI4 to control watchdog timer functions or the programmable outputs.
18	18	GPI3	General-Purpose Logic Input 3. An internal 10µA current source pulls GPI3 to GND. Configure GPI3 to control watchdog timer functions or the programmable outputs.
19	19	GPI2	General-Purpose Logic Input 2. An internal 10µA current source pulls GPI2 to GND. Configure GPI2 to control watchdog timer functions or the programmable outputs.
20	20	GPI1	General-Purpose Logic Input 1. An internal 10µA current source pulls GPI1 to GND. Configure GPI1 to control watchdog timer functions or the programmable outputs.
21	21	ABP	Internal Power-Supply Output. Bypass ABP to GND with a 1µF ceramic capacitor. ABP powers the internal circuitry of the MAX6872/MAX6873. ABP supplies the input voltage to the internal charge pumps when the programmable outputs are configured as charge-pump outputs. Do not use ABP to supply power to external circuitry.
22	22	DBP	Internal Digital Power-Supply Output. Bypass DBP to GND with a 1µF ceramic capacitor. DBP supplies power to the EEPROM memory and the internal logic circuitry. Do not use DBP to supply power to external circuitry.
25	—	IN6	Voltage Input 6. Configure IN6 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN6 to GND with a 0.1µF capacitor installed as close to the device as possible.
26	—	IN5	Voltage Input 5. Configure IN5 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN5 to GND with a 0.1µF capacitor installed as close to the device as possible.
27	27	IN4	Voltage Input 4. Configure IN4 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN4 to GND with a 0.1µF capacitor installed as close to the device as possible.
28	28	IN3	Voltage Input 3. Configure IN3 to detect voltage thresholds between 1V and 5.5V in 20mV increments, or 0.5V to 3.05V in 10mV increments. For improved noise immunity, bypass IN3 to GND with a 0.1µF capacitor installed as close to the device as possible.
29	29	IN2	Bipolar Voltage Input 2. Configure IN2 to detect negative voltage thresholds from -2.5V to -15.25V in 50mV increments or -1.25V to -7.625V in 25mV increments. Alternatively, configure IN2 to detect positive voltage thresholds from 2.5V to 15.25V in 50mV increments or 1.25V to 7.625V in 25mV increments. For improved noise immunity, bypass IN2 to GND with a 0.1µF capacitor installed as close to the device as possible.
30	30	IN1	High-Voltage Input 1. Configure IN1 to detect voltage thresholds from 2.5V to 13.2V in 50mV increments or 1.25V to 7.625V in 25mV increments. For improved noise immunity, bypass IN1 to GND with a 0.1µF capacitor installed as close to the device as possible.
31	31	I.C.	Internal Connection. Leave unconnected.
32	2	PO1	Programmable Output 1. Configurable active-high, active-low, open-drain, weak pullup, or charge-pump output. PO1 pulls low with a weak 10µA internal current sink for $1V < V_{ABP} < V_{UVLO}$. PO1 assumes its programmed conditional output state when ABP exceeds UVLO.
—	—	EP	Exposed Paddle. Exposed paddle is internally connected to GND.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Detailed Description

The MAX6872/MAX6873 EEPROM-configurable, multi-voltage supply sequencers/supervisors monitor several voltage-detector inputs and four general-purpose logic inputs, and feature programmable outputs for highly configurable, power-supply sequencing applications. The MAX6872 features six voltage-detector inputs and eight programmable outputs, while the MAX6873 features four voltage-detector inputs and five programmable outputs. Manual reset and margin disable inputs simplify board-level testing during the manufacturing process. The MAX6872/MAX6873 feature an accurate internal 1.25V reference.

All voltage detectors provide two configurable thresholds for undervoltage/overvoltage or dual undervoltage detection. One high-voltage input (IN1) provides detector threshold voltages from +1.25V to +7.625V in 25mV increments or +2.5V to +13.2V in 50mV increments. A bipolar input (IN2) provides detector threshold voltages from ±1.25V to ±7.625V in 25mV increments, or ±2.5V to ±15.25V in 50mV increments. Positive inputs (IN3–IN6) provide detector threshold voltages from +0.5V to +3.05V in 10mV increments, or +1.0V to +5.5V in 20mV increments.

The host controller communicates with the MAX6872/MAX6873s' internal 4kb user EEPROM, configuration EEPROM, configuration registers, and fault registers through an SMBus/I^{2}C-compatible serial interface (see Figure 1).

Programmable output options include active-high, active-low, open-drain, weak pullup, push-pull, and charge pump. Select the charge-pump output feature to drive n-channel FETs for power-supply sequencing (see the *Applications Information* section). The outputs swing between 0 and (V_{ABP} + 5V) when configured for charge-pump operation.

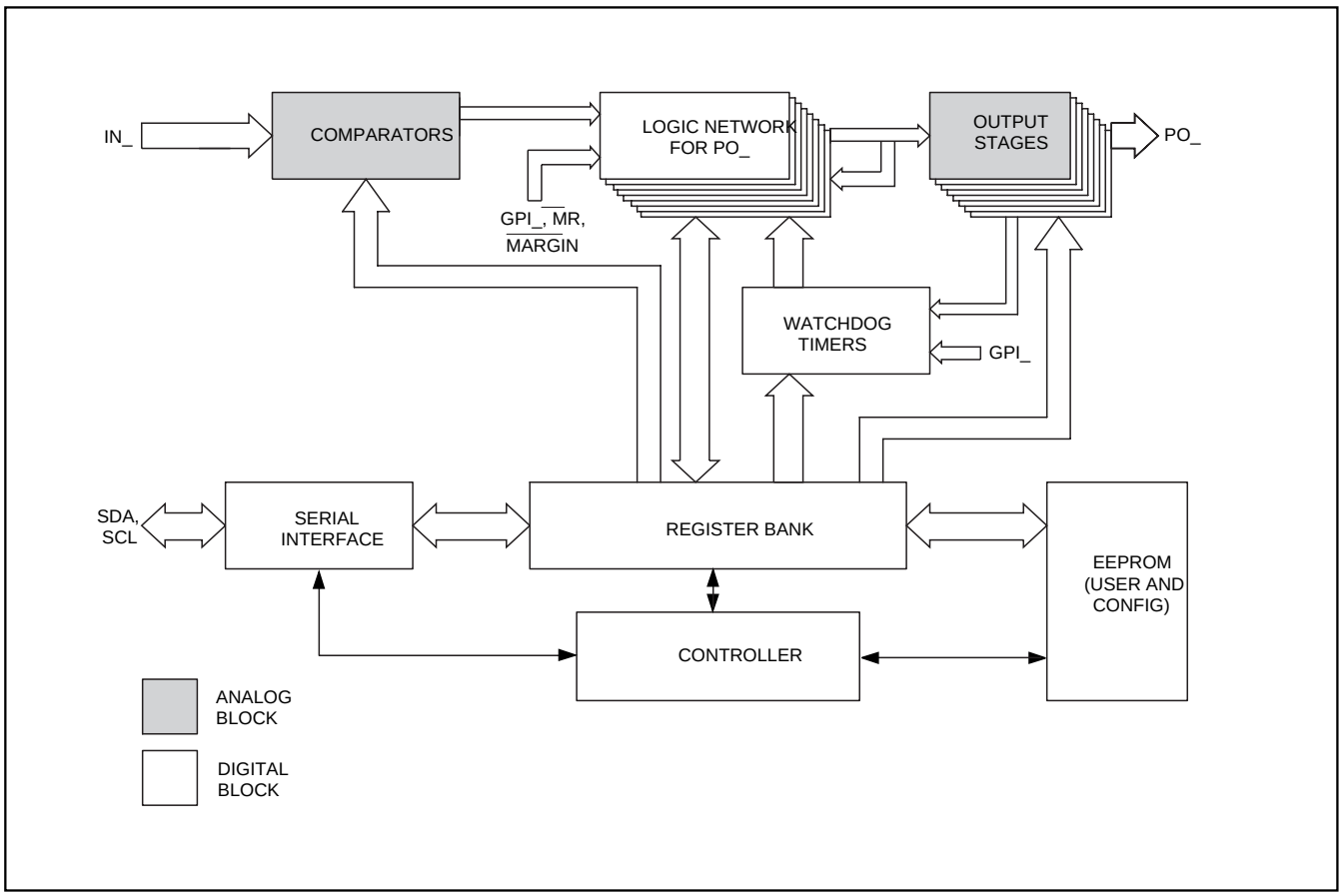
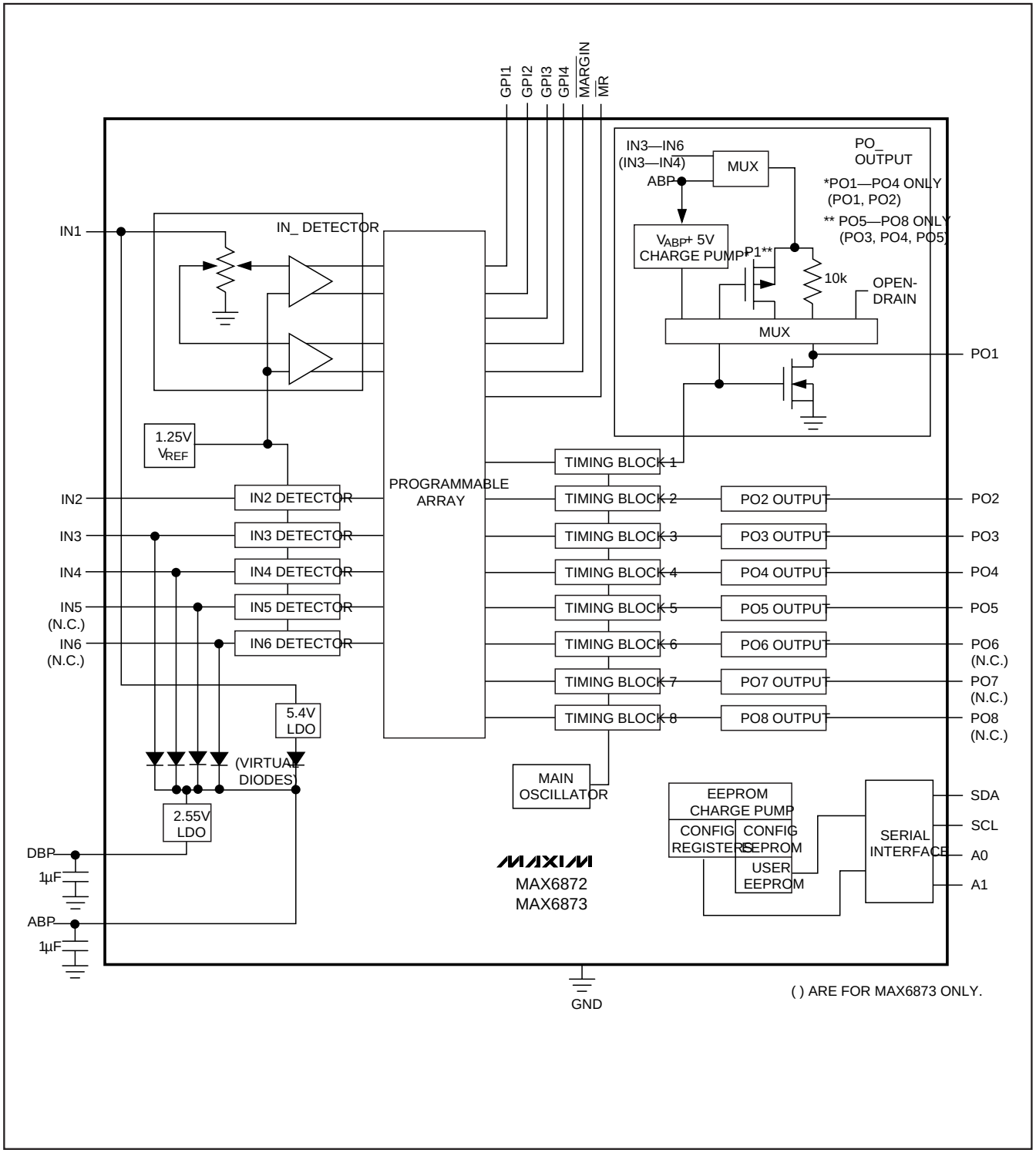


Figure 1. Top-Level Block Diagram

Functional Diagram



EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

Program each output to assert on any voltage-detector input, general-purpose logic input, watchdog timer, manual reset, or other output stages. Programmable timing-delay blocks configure each output to wait between 25µs and 1600ms before deasserting. A fault register logs the conditions that caused each output to assert (undervoltage, overvoltage, manual reset, etc.).

The MAX6872/MAX6873 feature two watchdog timers, adding flexibility. Program each watchdog timer to assert one or more programmable outputs. Program each watchdog timer to clear on a combination of one GPI_ input and one programmable output, one of the GPI_ inputs only, or one of the programmable outputs only. The initial and normal watchdog timeout periods are independently programmable from 6.25ms to 102.4s.

A virtual diode-ORing scheme selects the input that powers the MAX6872/MAX6873. The MAX6872/MAX6873 derive power from IN1 if V_{IN1} > +6.5V or from the highest voltage on IN3–IN6 if V_{IN1} < +2.7V. The power source cannot be determined if +4V < V_{IN1} < +6.5V and one of V_{IN3} through V_{IN6} > +2.7V. The programmable outputs maintain the correct programmed logic state for V_{ABP} > V_{UVLO}. One of IN3 through IN6 must be greater than +2.7V or IN1 must be greater than +4V for device operation.

Powering the MAX6872/MAX6873

The MAX6872/MAX6873 derive power from the positive voltage-detector inputs: IN1 or IN3–IN6. A virtual diode-ORing scheme selects the positive input that supplies power to the device (see the *Functional Diagram*). IN1 must be at least +4V or one of IN3–IN6 (MAX6872)/ IN3–IN4 (MAX6873) must be at least +2.7V to ensure device operation. An internal LDO regulates IN1 down to +5.4V.

The highest input voltage on IN3–IN6 (MAX6872)/ IN3–IN4 (MAX6873) supplies power to the device, unless V_{IN1} +6.5V, in which case IN1 supplies power to the device. For +4V < V_{IN1} < +6.5V and one of V_{IN3} through V_{IN6} > +2.7V, the input power source cannot be determined due to the dropout voltage of the LDO. Internal hysteresis ensures that the supply input that initially powered the device continues to power the device when multiple input voltages are within 50mV of each other.

ABP powers the analog circuitry; bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The internal supply voltage, measured at ABP, equals the maximum of IN3–IN6 (MAX6872)/IN3–IN4 (MAX6873) if V_{IN1} = 0, or equals +5.4V when V_{IN1} > +6.5V. Do not use ABP to provide power to external circuitry.

The MAX6872/MAX6873 also generate a digital supply voltage (DBP) for the internal logic circuitry and the EEPROM; bypass DBP to GND with a 1µF ceramic capacitor installed as close to the device as possible. The nominal DBP output voltage is +2.55V. Do not use DBP to provide power to external circuitry.

Inputs

The MAX6872/MAX6873 contain multiple logic and voltage-detector inputs. Each voltage-detector input is simultaneously monitored for primary and secondary thresholds. The primary threshold must be an undervoltage threshold. The secondary threshold may be an undervoltage or overvoltage threshold. Table 1 summarizes these various inputs.

Set the primary and secondary threshold voltages for each voltage-detector input with registers 00h–0Bh. Each primary threshold voltage must be an undervoltage threshold. Configure each secondary threshold voltage as an undervoltage or overvoltage threshold (see register 0Ch). Set the threshold range for each voltage detector with register 0Dh.

High-Voltage Input (IN1)

IN1 offers threshold voltages of +2.5V to +13.2V in 50mV increments, or +1.25V to +7.625V in 25mV increments. Use the following equations to set the threshold voltages for IN1:

$$x = \frac{V_{TH} \quad 2.5V}{0.05V} \text{ for } +2.5V \text{ to } +13.2V \text{ range}$$

$$x = \frac{V_{TH} \quad 1.25V}{0.025V} \text{ for } +1.25V \text{ to } +7.625V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 2). For the +2.5V to +13.2V range, x must equal 214 or less, otherwise the threshold exceeds the maximum operating voltage of IN1.

Bipolar-Voltage Input (IN2)

IN2 offers negative thresholds from -2.5V to -15.25V in 50mV increments, or from -1.25V to -7.625V in 25mV increments. Alternatively, IN2 offers positive thresholds from +2.5V to +15.25V in 50mV increments, or +1.25V to +7.625V in 25mV increments. Use the following equations to set the threshold voltages for IN2:

$$x = \frac{\left(V_{TH} \quad 2.5V\right)}{0.05V} \text{ for } 2.5V \text{ to } 15.25V \text{ range}$$

Table 1. Programmable Features

FEATURE	DESCRIPTION
High-Voltage Input (IN1)	Primary undervoltage threshold Secondary overvoltage or undervoltage threshold +2.5V to +13.2V threshold in 50mV increments +1.25V to +7.625V threshold in 25mV increments
Bipolar-Voltage Input (IN2)	Primary undervoltage threshold Secondary overvoltage or undervoltage threshold ±2.5V to ±15.25V threshold in 50mV increments ±1.25V to ±7.625V threshold in 25mV increments
Positive-Voltage Input IN3–IN6 (MAX6872), IN3–IN4 (MAX6873)	Primary undervoltage threshold Secondary overvoltage or undervoltage threshold +1V to +5.5V threshold in 20mV increments +0.5V to +3.05V threshold in 10mV increments
Programmable Outputs PO1–PO4 (MAX6872), PO1–PO2 (MAX6873)	Active high or active low Open-drain, weak pullup, or charge-pump output Weak pullup to IN3–IN6 (IN3 or IN4 for MAX6873) or ABP Dependent on MR, MARGIN, IN_, GPI1–GPI4 , WD1 and WD2, and/or PO_ Programmable timeout periods of 25µs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s
Programmable Outputs PO5–PO8 (MAX6872), PO3–PO5 (MAX6873)	Active high or active low Open-drain, weak pullup, or push-pull output Weak pullup to IN3–IN6 (IN3 or IN4 for MAX6873) or ABP Push-pull to IN3–IN6 (IN3 or IN4 for MAX6873) Dependent on MR, MARGIN, IN_, GPI1–GPI4 , WD1 and WD2, and/or PO_ Programmable timeout periods of 25µs, 1.5625ms, 6.25ms, 25ms, 50ms, 200ms, 400ms, or 1.6s
General-Purpose Logic Inputs (GPI1–GPI4)	Active high or active low logic levels Configure GPI_ as inputs to watchdog timers or programmable output stages
Watchdog Timers	Clear dependent on any combination of one GPI_ input and one programmable output, a GPI_ input only, or a programmable output only Initial watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s Normal watchdog timeout period of 6.25ms, 25ms, 100ms, 400ms, 1.6s, 6.4s, 25.6s, or 102.4s Watchdog enable/disable Initial watchdog timeout period enable/disable
Manual Reset Input (MR)	Forces PO_ into the active output state when MR = GND PO_ deassert after MR releases high and the PO_ timeout period expires PO_ cannot be a function of MR only
Margining Input (MARGIN)	Holds PO_ in existing state or asserts PO_ to a programmed output state, independent of changes in monitored inputs or watchdog timers, when MARGIN = GND Overrides MR when both assert at the same time
Write Disable	Locks user EEPROM based on PO_
Configuration Lock	Locks configuration EEPROM

Table 2. IN1 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
00h	8000h	[7:0]	IN1 primary undervoltage detector threshold (V1A) (see equations in the *High-Voltage Input (IN1)* section).
06h	8006h	[7:0]	IN1 secondary undervoltage/overvoltage detector threshold (V1B) (see equations in the *High-Voltage Input (IN1)* section).
0Ch	800Ch	[0]	IN1 secondary overvoltage/undervoltage selection: 0 = overvoltage threshold. 1 = undervoltage threshold.
0Dh	800Dh	[0]	IN1 range selection: 0 = 2.5V to 13.2V range in 50mV increments. 1 = 1.25V to 7.625V range in 25mV increments.

Table 3. IN2 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
01h	8001h	[7:0]	IN2 primary undervoltage detector threshold (V2A) (see equations in the *Bipolar-Voltage Input (IN2)* section).
07h	8007h	[7:0]	IN2 secondary undervoltage/overvoltage detector threshold (V2B) (see equations in the *Bipolar-Voltage Input (IN2)* section).
0Ch	800Ch	[1]	IN2 secondary overvoltage/undervoltage selection: 0 = overvoltage threshold. 1 = undervoltage threshold.
0Dh	800Dh	[7:6]	IN2 range selection: 00 = -2.5V to -15.25V range in 50mV increments. 01 = -1.25V to -7.625V range in 25mV increments. 10 = +2.5V to +15.25V range in 50mV increments. 11 = +1.25V to +7.625V range in 25mV increments.

$$x = \frac{(V_{TH} \quad 1.25V)}{0.025V} \text{ for } 1.25V \text{ to } 7.625V \text{ range}$$

$$x = \frac{V_{TH} \quad 2.5V}{0.05V} \text{ for } +2.5V \text{ to } +15.25V \text{ range}$$

$$x = \frac{V_{TH} \quad 1.25V}{0.025V} \text{ for } +1.25V \text{ to } +7.625V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 3).

IN3–IN6

IN3–IN6 offer positive voltage detectors monitor voltages from +1V to +5.5V in 20mV increments, or +0.5V to +3.05V in 10mV increments. Use the following equations to set the threshold voltages for IN_:

$$x = \frac{V_{TH} \quad 1V}{0.02V} \text{ for } +1V \text{ to } +5.5V \text{ range}$$

$$x = \frac{V_{TH} \quad 0.5V}{0.01V} \text{ for } +0.5V \text{ to } +3.05V \text{ range}$$

where V_{TH} is the desired threshold voltage and x is the decimal code for the desired threshold (Table 4). For the +1V to +5.5V range, x must equal 225 or less, oth-

Table 4. IN3–IN6 Threshold Settings

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
02h	8002h	[7:0]	IN3 primary undervoltage detector threshold (V3A) (see equations in the *IN3–IN6* section).
03h	8003h	[7:0]	IN4 primary undervoltage detector threshold (V4A) (see equations in the *IN3–IN6* section).
04h	8004h	[7:0]	IN5 (MAX6872 only) primary undervoltage detector threshold (V5A) (see equations in the *IN3–IN6* section).
05h	8005h	[7:0]	IN6 (MAX6872 only) primary undervoltage detector threshold (V6A) (see equations in the *IN3–IN6* section).
08h	8008h	[7:0]	IN3 secondary undervoltage/overvoltage detector threshold (V3B) (see equations in the *IN3–IN6* section).
09h	8009h	[7:0]	IN4 secondary undervoltage/overvoltage detector threshold (V4B) (see equations in the *IN3–IN6* section).
0Ah	800Ah	[7:0]	IN5 (MAX6872 only) secondary undervoltage/overvoltage detector threshold (V5B) (see equations in the *IN3–IN6* section).
0Bh	800Bh	[7:0]	IN6 (MAX6872 only) secondary undervoltage/overvoltage detector threshold (V6B) (see equations in the *IN3–IN6* section).
0Ch	800Ch	[2]	IN3 secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[3]	IN4 secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[4]	IN5 (MAX6872 only) secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[5]	IN6 (MAX6872 only) secondary overvoltage/undervoltage selection. 0 = overvoltage threshold. 1 = undervoltage threshold.
		[7:6]	Not used.
0Dh	800Dh	[1]	IN3 range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[2]	IN4 range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[3]	IN5 (MAX6872 only) range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[4]	IN6 (MAX6872 only) range selection. 0 = +1V to +5.5V range in 20mV increments. 1 = +0.5V to +3.05V range in 10mV increments.
		[5]	Not used.

erwise the threshold exceeds the maximum operating voltage of IN3–IN6.

GPI1–GPI4

The GPI1–GPI4 programmable logic inputs control power-supply sequencing (programmable outputs), reset/interrupt signaling, and watchdog functions (see the *Configuring the Watchdog Timers (Registers 3Ch–3Fh)* section). Configure GPI1–GPI4 for active-low or active-high logic (Table 5). GPI1–GPI4 internally pull down to GND through a 10µA current sink.

EEPROM-Programmable, Hex/Quad, Power-Supply Sequencers/Supervisors

MR

The manual reset (MR) input initiates a reset condition. Register 40h determines the programmable outputs that assert while MR is low (Table 6). All affected programmable outputs remain asserted (see the *Programmable Outputs* section) for their PO_ timeout periods after MR releases high. An internal 10µA current source pulls MR to DBP. Leave MR unconnected or connect to DBP if unused. A programmable output cannot depend solely on MR.

MARGIN

MARGIN allows system-level testing while power supplies exceed the normal ranges. Registers 41h and 42h determine whether the programmable outputs assert to a predetermined state or hold the last state as MARGIN is driven low (Table 7). Drive MARGIN low to set the programmable outputs in a known state while system-level testing occurs. Leave MARGIN unconnected or connect to DBP if unused. An internal 10µA current source pulls MARGIN to DBP. The state of each programmable output does not change while MARGIN = GND. MARGIN overrides MR if both assert at the same time.

Programmable Outputs

The MAX6872 features eight programmable outputs, while the MAX6873 features five programmable outputs. Selectable output-stage configurations include: active low or active high, open drain, weak pullup, push-pull, or charge pump. During power-up, the programmable outputs pull to GND with an internal 10µA current sink for $1V < V_{ABP} < V_{UVLO}$. The programmable outputs remain in their active states until their respective PO_ timeout periods expire, and all of the programmed conditions are met for each output. Any output programmed to depend on no condition always remains in its active state (Table 20). An active-high configured output is considered asserted

Table 5. GPI1–GPI4 Active Logic States

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
3Bh	803Bh	[0]	GPI1. 0 = active low. 1 = active high.
		[1]	GPI2. 0 = active low. 1 = active high.
		[2]	GPI3. 0 = active low. 1 = active high.
		[3]	GPI4. 0 = active low. 1 = active high.

Table 6. Programmable Output Behavior and MR

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	DESCRIPTION
40h	8040h	[0]	PO1 (MAX6872 only). 0 = PO1 independent of MR. 1 = PO1 asserts when MR = low.
		[1]	PO2 (MAX6872 only). 0 = PO2 independent of MR. 1 = PO2 asserts when MR = low.
		[2]	PO3 (MAX6872)/PO1 (MAX6873). 0 = PO3/PO1 independent of MR. 1 = PO3/PO1 asserts when MR = low.
		[3]	PO4 (MAX6872)/PO2 (MAX6873). 0 = PO4/PO2 independent of MR. 1 = PO4/PO2 asserts when MR = low.
		[4]	PO5 (MAX6872)/PO3 (MAX6873). 0 = PO5/PO3 independent of MR. 1 = PO5/PO3 asserts when MR = low.
		[5]	PO6 (MAX6872)/PO4 (MAX6873). 0 = PO6/PO4 independent of MR. 1 = PO6/PO4 asserts when MR = low.
		[6]	PO7 (MAX6872)/PO5 (MAX6873). 0 = PO7/PO5 independent of MR. 1 = PO7/PO5 asserts when MR = low.
		[7]	PO8 (MAX6872 only). 0 = PO8 independent of MR. 1 = PO8 asserts when MR = low.

when that output is logic-high. No output can depend solely on MR.

The positive voltage monitors generate fault signals (logical 0) to the MAX6872/MAX6873s' logic array when an input voltage is below the programmed undervoltage threshold, or when that voltage is above the overvoltage threshold. The negative voltage monitor (IN2) generates a fault signal to the logic array when the input voltage is less negative than the undervoltage threshold, or when that voltage is more negative than the overvoltage threshold.

Registers 0Eh through 3Ah and 40h configure each of the programmable outputs. Programmable timing blocks set the PO_ timeout period from 25µs to 1600ms

Table 7. Programmable Output Behavior and MARGIN

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT RANGE	AFFECTED OUTPUT	DESCRIPTION
41h	8041h	[0]	PO1 (MAX6872 only)	0 = output held in existing state. 1 = output asserts high or low (see 42h[0]).
		[1]	PO2 (MAX6872 only)	0 = output held in existing state. 1 = output asserts high or low (see 42h[1]).
		[2]	PO3 (MAX6872) PO1 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[2]).
		[3]	PO4 (MAX6872) PO2 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[3]).
		[4]	PO5 (MAX6872) PO3 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[4]).
		[5]	PO6 (MAX6872) PO4 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[5]).
		[6]	PO7 (MAX6872) PO5 (MAX6873)	0 = output held in existing state. 1 = output asserts high or low (see 42h[6]).
		[7]	PO8 (MAX6872 only)	0 = output held in existing state. 1 = output asserts high or low (see 42h[7]).
42h	8042h	[0]	PO1 (MAX6872 only)	0 = output asserts low if 41h[0] = 1. 1 = output asserts high if 41h[0] = 1.
		[1]	PO2 (MAX6872 only)	0 = output asserts low if 41h[1] = 1. 1 = output asserts high if 41h[1] = 1.
		[2]	PO3 (MAX6872) PO1 (MAX6873)	0 = output asserts low if 41h[2] = 1. 1 = output asserts high if 41h[2] = 1.
		[3]	PO4 (MAX6872) PO2 (MAX6873)	0 = output asserts low if 41h[3] = 1. 1 = output asserts high if 41h[3] = 1.
		[4]	PO5 (MAX6872) PO3 (MAX6873)	0 = output asserts low if 41h[4] = 1. 1 = output asserts high if 41h[4] = 1.
		[5]	PO6 (MAX6872) PO4 (MAX6873)	0 = output asserts low if 41h[5] = 1. 1 = output asserts high if 41h[5] = 1.
		[6]	PO7 (MAX6872) PO5 (MAX6873)	0 = output asserts low if 41h[6] = 1. 1 = output asserts high if 41h[6] = 1.
		[7]	PO8 (MAX6872 only)	0 = output asserts low if 41h[7] = 1. 1 = output asserts high if 41h[7] = 1.

Table 8. PO1 (MAX6872 Only) Output Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
0Eh	800Eh	[0]	1 = PO1 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO1 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO1 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO1 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO1 assertion depends on IN5 primary undervoltage threshold (Table 4).
		[5]	1 = PO1 assertion depends on IN6 primary undervoltage threshold (Table 4).
		[6]	1 = PO1 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO1 assertion depends on watchdog 2 (Tables 25 and 26).
0Fh	800Fh	[0]	1 = PO1 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO1 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO1 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO1 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO1 assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4).
		[5]	1 = PO1 assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4).
		[6]	1 = PO1 assertion depends on GPI1 (Table 5).
		[7]	1 = PO1 assertion depends on GPI2 (Table 5).
10h	8010h	[0]	1 = PO1 assertion depends on GPI3 (Table 5).
		[1]	1 = PO1 assertion depends on GPI4 (Table 5).
		[2]	1 = PO1 assertion depends on PO2 (Table 9).
		[3]	1 = PO1 assertion depends on PO3 (Tables 10 and 11).
		[4]	1 = PO1 assertion depends on PO4 (Tables 12 and 13).
		[5]	1 = PO1 assertion depends on PO5 (Tables 14 and 15).
		[6]	1 = PO1 assertion depends on PO6 (Tables 16 and 17).
		[7]	1 = PO1 assertion depends on PO7 (Table 18).
11h	8011h	[0]	1 = PO1 assertion depends on PO8 (Table 19).
40h	8040h	[0]	1 = PO1 asserts when MR = low (Table 6).

for each programmable output. See register 3Ah (Table 20) to set the active state (active-high or active-low) for each programmable output and registers 11h, 15h, 1Ch, 23h, 2Ah, 31h, 35h, and 39h to select the output stage types (Tables 21 and 22), and PO_ timeout periods (Table 23) for each output.

Control selected programmable outputs with a sum of products (Tables 8–19). Each product allows a different set of conditions to assert each output. Outputs PO3 (MAX6872)/PO1 (MAX6873) and PO6 (MAX6872)/PO4 (MAX6873) allow two sets of different conditions to assert each output. Outputs PO1 and PO2 (MAX6872 only), PO7 (MAX6872)/PO5 (MAX6873), and PO8 (MAX6872 only) allow only one set of conditions to assert each output.

For example, Product 1 of the PO3 (MAX6872—Table 10) programmable output may depend on the IN1 primary undervoltage threshold, and the states of GPI1, PO1, and PO2. Write a one to R16h[0], R17h[6], and R18h[3:2] to configure Product 1 as indicated. IN1 must be above the primary undervoltage threshold (Table 2), GPI1 must be inactive (Table 5), and PO1 (Tables 8 and 20) and PO2 (Tables 10 and 21) must be in their deasserted states for Product 1 to be a logical 1. Product 1 is equivalent to the logic statement: V1A GPI1 PO1 PO2.

Product 2 of PO3 (MAX6872, Table 11) may depend on an entirely different set of conditions, or the same conditions, depending on the system requirements. For example, Product 2 may depend on the IN1 undervolt-

Table 9. PO2 (MAX6872 Only) Output Dependency

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
12h	8012h	[0]	1 = PO2 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO2 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO2 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO2 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO2 assertion depends on IN5 primary undervoltage threshold (Table 4).
		[5]	1 = PO2 assertion depends on IN6 primary undervoltage threshold (Table 4).
		[6]	1 = PO2 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO2 assertion depends on watchdog 2 (Tables 25 and 26).
13h	8013h	[0]	1 = PO2 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO2 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO2 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO2 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO2 assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4).
		[5]	1 = PO2 assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4).
		[6]	1 = PO2 assertion depends on GPI1 (Table 5).
		[7]	1 = PO2 assertion depends on GPI2 (Table 5).
14h	8014h	[0]	1 = PO2 assertion depends on GPI3 (Table 5).
		[1]	1 = PO2 assertion depends on GPI4 (Table 5).
		[2]	1 = PO2 assertion depends on PO1 (Table 8).
		[3]	1 = PO2 assertion depends on PO3 (Tables 10 and 11).
		[4]	1 = PO2 assertion depends on PO4 (Tables 12 and 13).
		[5]	1 = PO2 assertion depends on PO5 (Tables 14 and 15).
		[6]	1 = PO2 assertion depends on PO6 (Tables 16 and 17).
		[7]	1 = PO2 assertion depends on PO7 (Table 18).
15h	8015h	[0]	1 = PO2 assertion depends on PO8 (Table 19).
40h	8040h	[1]	1 = PO2 asserts when MR = low (Table 6).

age threshold, and the states of GPI2 and WD1. Write ones to R19h[6, 0] and R1Ah[7] to configure Product 2 as indicated. IN1 must be above the primary undervoltage threshold (Table 2), GPI2 must be inactive (Table 5), and the WD1 timer must not have expired (Tables 25 and 26) for Product 2 to be a logical 1. Product 2 is equivalent to the logic statement: V1A GPI2 WD1. PO3 deasserts if either Product 1 or Product 2 is a logical 1. The logical statement: Product 1 + Product 2 determines the state of PO3.

Table 8 only applies to PO1 of the MAX6872. Write a 0 to a bit to make the PO1 output independent of the respective signal (IN1–IN6 primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, MR, or other programmable outputs).

Table 9 only applies to PO2 of the MAX6872. Write a 0 to a bit to make the PO2 output independent of the respective signal (IN1–IN6 primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, MR, or other programmable outputs).

Table 10. PO3 (MAX6872)/PO1 (MAX6873) Output Dependency (Product 1)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
16h	8016h	[0]	1 = PO3/PO1 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO3/PO1 assertion depends on watchdog 2 (Tables 25 and 26).
17h	8017h	[0]	1 = PO3/PO1 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on GPI1 (Table 5).
		[7]	1 = PO3/PO1 assertion depends on GPI2 (Table 5).
18h	8018h	[0]	1 = PO3/PO1 assertion depends on GPI3 (Table 5).
		[1]	1 = PO3/PO1 assertion depends on GPI4 (Table 5).
		[2]	1 = PO3 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO3 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO3/PO1 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[5]	1 = PO3/PO1 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[6]	1 = PO3/PO1 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO3/PO1 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
1Ch	801Ch	[0]	1 = PO3 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[2]	1 = PO3/PO1 asserts when MR = low (Table 6).

Table 10 only applies to PO3 of the MAX6872 and PO1 of the MAX6873. Write a 0 to a bit to make the PO3/PO1 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, MR, or other programmable outputs). See Table 11 for Product 2. PO3 (MAX6872)/PO1 (MAX6873) deasserts when Product 1 or Product 2 = 1.

Table 11. PO3 (MAX6872)/PO1 (MAX6873) Output Dependency (Product 2)

REGISTER ADDRESS	EEPROM MEMORY ADDRESS	BIT	OUTPUT ASSERTION CONDITIONS
19h	8019h	[0]	1 = PO3/PO1 assertion depends on IN1 primary undervoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 primary undervoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 primary undervoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 primary undervoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 primary undervoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on watchdog 1 (Tables 25 and 26).
		[7]	1 = PO3/PO1 assertion depends on watchdog 2 (Tables 25 and 26).
1Ah	801Ah	[0]	1 = PO3/PO1 assertion depends on IN1 secondary undervoltage/overvoltage threshold (Table 2).
		[1]	1 = PO3/PO1 assertion depends on IN2 secondary undervoltage/overvoltage threshold (Table 3).
		[2]	1 = PO3/PO1 assertion depends on IN3 secondary undervoltage/overvoltage threshold (Table 4).
		[3]	1 = PO3/PO1 assertion depends on IN4 secondary undervoltage/overvoltage threshold (Table 4).
		[4]	1 = PO3 (MAX6872 only) assertion depends on IN5 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[5]	1 = PO3 (MAX6872 only) assertion depends on IN6 secondary undervoltage/overvoltage threshold (Table 4). Must be set to 0 for the MAX6873.
		[6]	1 = PO3/PO1 assertion depends on GPI1 (Table 5).
		[7]	1 = PO3/PO1 assertion depends on GPI2 (Table 5).
1Bh	801Bh	[0]	1 = PO3/PO1 assertion depends on GPI3 (Table 5).
		[1]	1 = PO3/PO1 assertion depends on GPI4 (Table 5).
		[2]	1 = PO3 (MAX6872 only) assertion depends on PO1 (Table 8). Must be set to 0 for the MAX6873.
		[3]	1 = PO3 (MAX6872 only) assertion depends on PO2 (Table 9). Must be set to 0 for the MAX6873.
		[4]	1 = PO3/PO1 assertion depends on PO4 (MAX6872)/PO2 (MAX6873) (Tables 12 and 13).
		[5]	1 = PO3/PO1 assertion depends on PO5 (MAX6872)/PO3 (MAX6873) (Tables 14 and 15).
		[6]	1 = PO3/PO1 assertion depends on PO6 (MAX6872)/PO4 (MAX6873) (Tables 16 and 17).
		[7]	1 = PO3/PO1 assertion depends on PO7 (MAX6872)/PO5 (MAX6873) (Table 18).
1Ch	801Ch	[1]	1 = PO3 (MAX6872 only) assertion depends on PO8 (Table 19). Must be set to 0 for the MAX6873.
40h	8040h	[2]	1 = PO3/PO1 asserts when MR = low (Table 6).

Table 11 only applies to PO3 of the MAX6872 and PO1 of the MAX6873. Write a 0 to a bit to make the PO3/PO1 output independent of the respective signal (IN_ primary or secondary thresholds, WD1 or WD2, GPI1–GPI4, MR, or other programmable outputs). See Table 10 for Product 1. PO3 (MAX6872)/PO1 (MAX6873) deasserts when Product 1 or Product 2 = 1.

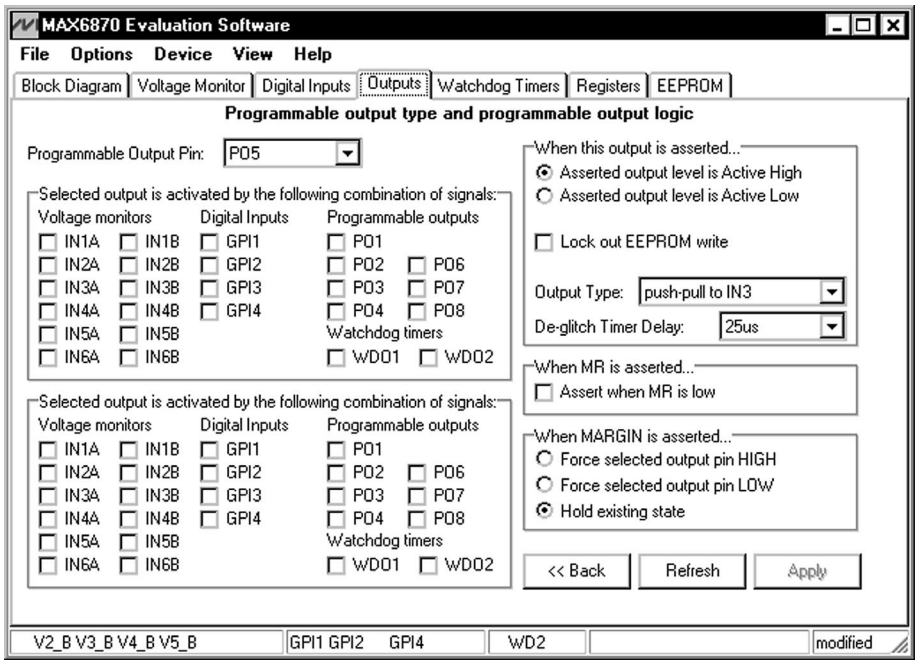


Figure 5. Programmable Outputs

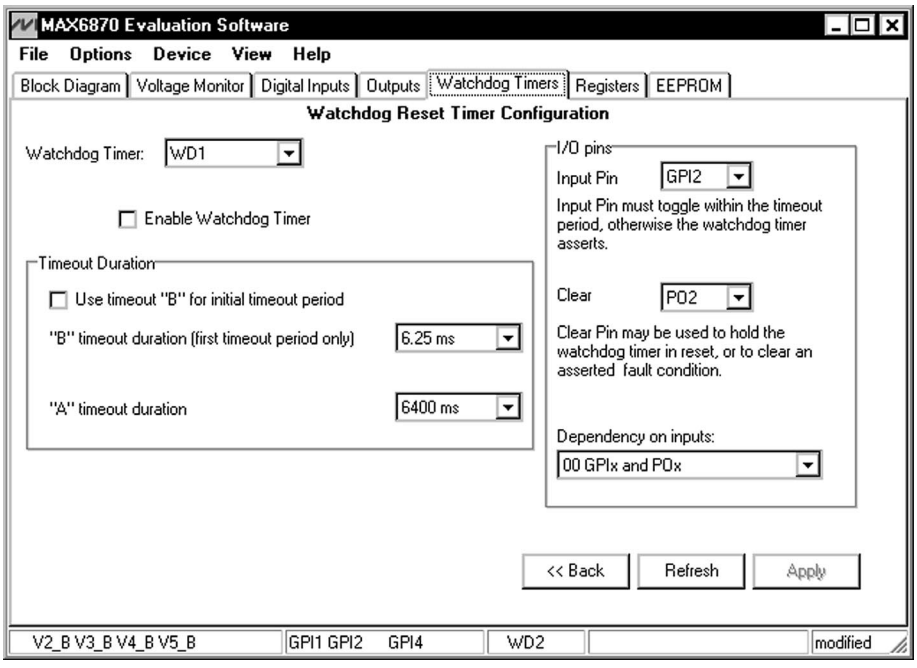


Figure 6. Watchdog Timers

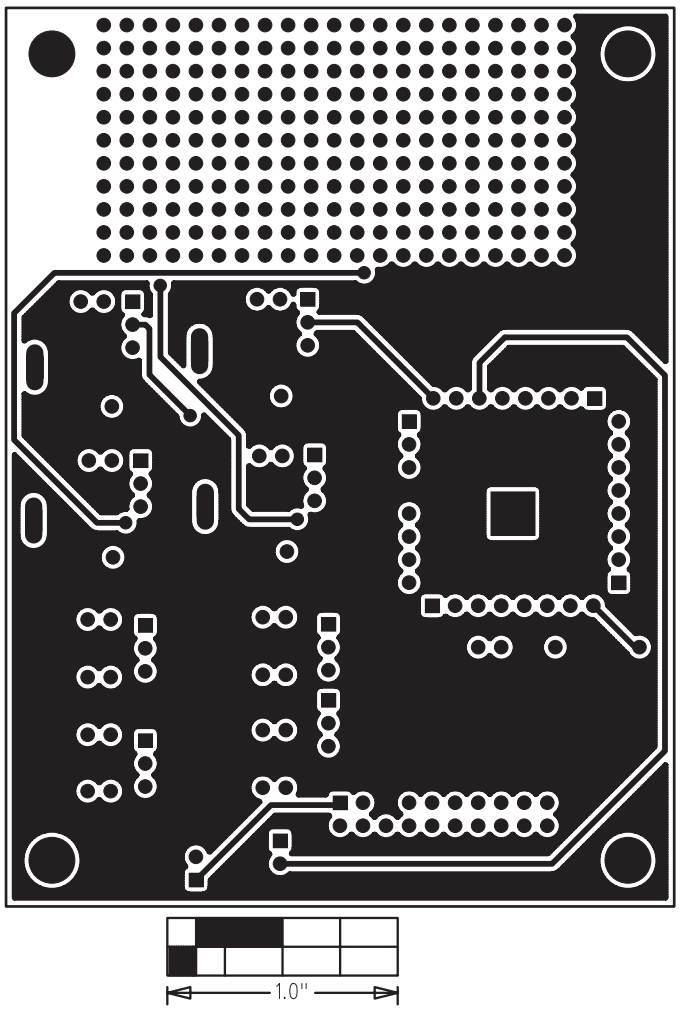


Figure 12. MAX6870 EV Kit PC Board Layout—Solder Side