19-3320; Rev 1; 1/05

MAXIM

-48V Hot-Swap Controller with V_{IN} Step Immunity, No R_{SENSE}, and Overvoltage Protection

MAX5938

General Description

The MAX5938 is a hot-swap controller for -10V to -80V rails. The MAX5938 allows circuit line cards to be safely hot-plugged into a live backplane without causing a glitch on the power supply. It integrates an adjustable circuit-breaker function requiring no R_{SENSE}.

The MAX5938 provides a controlled turn-on for circuit cards, which limits inrush current and prevents both glitches on the power-supply rail and damage to board connectors and components. Before startup, the MAX5938 performs a Load Probe™ test to detect the presence of a short-circuit condition. If a short-circuit condition does not exist, the device limits the inrush current drawn by the load by gradually turning on the external MOSFET. Once the external MOSFET is fully enhanced, the MAX5938 provides overcurrent and short-circuit protection by monitoring the voltage drop across the $R_{DS(ON)}$ of the external power MOSFET. The MAX5938 integrates a 400mA fast GATE pulldown to guarantee that the external MOSFET is rapidly turned off in the event of an overcurrent or short-circuit condition.

The MAX5938 also protects the system against input voltage (V_{IN}) steps. During an input voltage step, the device limits the current drawn by the load to a safe level without shutting down the load. The device also includes ON/OFF control, selectable PGOOD output polarity, undervoltage (UV) and overvoltage (OV) protection.

The device offers latched (MAX5938L) or autoretry (MAX5938A) fault management. Both the MAX5938A and MAX5938L are available in a 16-pin QSOP package and are specified for the extended (-40°C to +85°C) temperature range.

Applications

- Servers
- Telecom Line Cards
- Network Switches
- Solid-State Circuit Breakers
- Network Routers

Typical Operating Circuit appears at end of data sheet.

Load Probe is a trademark of Maxim Integrated Products, Inc.

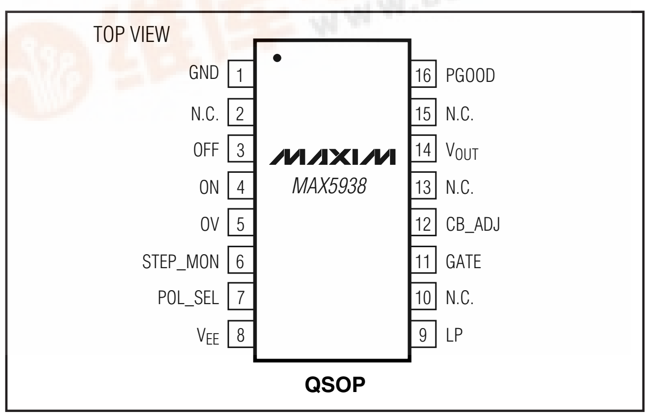
Features

- ♦ -10V to -80V Operation
- ♦ No External R_{SENSE} Required
- ♦ Drives Large Power MOSFETS
- ♦ Eliminates Inrush Current Spikes During Hot Plug into Powered Backplane
- ♦ Eliminates Inrush Current Spikes and Dropping of Load During Large V_{IN} Steps
- ♦ Adjustable Circuit-Breaker Threshold with Temperature Compensation
- ♦ Circuit-Breaker Fault with Transient Rejection
- ♦ Shorted Load Detection (Load Probe) Before Power MOSFET Turn-On
- ♦ Programmable Load-Voltage Slew Rate Controls Inrush Current
- ♦ ±2.4% Accuracy, Programmable Turn-On/Off Voltage (UVLO)
- ♦ Overvoltage Fault Protection with Transient Rejection
- ♦ Autoretry and Latched Fault Management Available
- ♦ Low Quiescent Current (1mA)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5938AEEE	-40°C to +85°C	16 QSOP
MAX5938LEEE	-40°C to +85°C	16 QSOP

Pin Configuration



-48V Hot-Swap Controller with V_{IN} Step Immunity, No R_{SENSE}, and Overvoltage Protection

ABSOLUTE MAXIMUM RATINGS

V_{EE}, V_{OUT}, PGOOD, LP,
STEP_MON to GND .... +0.3V to -85V
PGOOD to V_{OUT} .... -0.3V to +85V
V_{OUT}, LP, STEP_MON to V_{EE} .... -0.3V to +85V
GATE to V_{EE} .... -0.3V to +20V
ON, OFF, OV, POL_SEL, CB_ADJ to V_{EE} .... -0.3V to +6V
Input Current
LP (internally duty-cycle limited) 1A
PGOOD (continuous) 80mA
GATE (during 15V clamp, continuous) 30mA
GATE (during 2V clamp, continuous) 50mA
GATE (during gate pulldown, continuous) 50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -10V to -80V, V_{IN} = (GND - V_{EE}), V_{STEP_MON} = V_{EE}, R_{LP} = 200Ω, V_{ON} = V_{OFF} = 2V, V_{OV} = V_{CB_ADJ} = V_{EE}, POL_SEL open, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{EE} = -48V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{EE}	Referenced to GND		-80		-10	V
Operating Supply Current	I_{CC}				0.95	1.4	mA
ON/OFF, OV							
ON Reference Threshold Rising	$V_{ON\_REF,R}$	V_{ON} increasing		1.219	1.25	1.281	V
ON Reference Threshold Falling	$V_{ON\_REF,F}$	V_{ON} decreasing		1.069	1.125	1.181	V
ON Glitch Rejection (Note 3)	t_{REJ}	V_{ON} decreasing		0.80	1.5	2.25	ms
OFF Reference Threshold	V_{OFF_REF}			1.219	1.25	1.281	V
ON/OFF/OV Input Bias Current	I_{BIAS}			-25		+25	nA
OV Reference Threshold, Rising	$V_{OV\_REF,R}$	V_{OV} increasing		1.219	1.25	1.281	V
OV Reference Threshold, Falling	$V_{OV\_REF,F}$	V_{OV} decreasing		1.069	1.125	1.181	V
OV Transient Rejection	t_{OVREJ}	OV increasing		0.80	1.5	2.25	ms
Power-Up Delay (Note 4)	t_{ONDLY}			80	220	380	ms
V_{OUT} to V_{EE} Leakage Current		V_{OFF} = V_{EE} = -80V, V_{OUT} = GND, PGOOD open			0.01	1	µA
LP to V_{EE} Leakage Current		V_{OFF} = V_{EE} = -80V, LP = GND			0.01	1	µA
POL_SEL to V_{EE} Input Current		POL_SEL = V_{EE}		-50	-34	-20	µA
GATE DRIVE							
External Gate-Drive Voltage	V_{GS}	V_{GATE} - V_{EE}	V_{IN} = 10V	6.5	6.8	7.2	V
			14V < V_{IN} < 80V	8.1	10	12.8	
GATE to V_{EE} Clamp Voltage		MOSFET fully enhanced	I_{CLAMP} = 9mA	13.5	16		V
			I_{CLAMP} = 20mA		17	19.5	
		Power-off, V_{EE} = GND	I_{CLAMP} = 1mA		2.1	2.55	
			I_{CLAMP} = 10mA		2.5	2.93	
Open-Loop Gate Charge Current	$I_{G,ON}$	V_{GATE} = V_{EE}, V_{OUT} = GND		-66	-52	-35	µA
GATE Pulldown Switch On-Resistance	$R_{G,OFF}$	V_{GATE} - V_{EE} = 500mV	V_{IN} > 10V		9.0	14.1	mA
			V_{IN} > 14V		7.5	12.5	
Output-Voltage Slew Rate	SR	I dV_{OUT}/dt I, C_{SLEW} = 0		2.4	9.0	14.8	V/ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -10V to -80V, V_{IN} = (GND - V_{EE}), V_{STEP_MON} = V_{EE}, R_{LP} = 200Ω, V_{ON} = V_{OFF} = 2V, V_{OV} = V_{CB_ADJ} = V_{EE}, POL_SEL open, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{EE} = -48V, T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CIRCUIT BREAKER AND SHORT CIRCUIT							
CB_ADJ Bias Current	I_{CB_ADJ}	CB_ADJ = V_{EE}	T_A = +85°C	55	72	89	µA
			T_A = +25°C	39	50	61	
			T_A = -40°C		33		
Circuit-Breaker Threshold	V_{CB}	CB_ADJ = V_{EE}	T_A = +85°C	59	72	85	mV
			T_A = +25°C	41	50	59	
			T_A = -40°C		33		
		R_{CB_ADJ} = 2kΩ	T_A = +85°C	123	144	165	
			T_A = +25°C	85	100	115	
			T_A = -10°C	66	82	98	
			T_A = -40°C		66		
I_{CB_ADJ} Temperature Coefficient		-40°C < T_A < +85°C			6000		ppm/°C
Circuit-Breaker Glitch Rejection	t_{CB_DLY}			1.0	1.2	1.6	ms
Short-Circuit Threshold (Note 5)	V_{SC}	CB_ADJ = V_{EE}	T_A = +85°C	112	144	176	mV
			T_A = +25°C	75	100	125	
			T_A = -10°C	50	82	114	
			T_A = -40°C		66		
		R_{CB_ADJ} = 2kΩ	T_A = +85°C	224	288	352	
			T_A = +25°C	159	200	241	
			T_A = -10°C	108	164	220	
			T_A = -40°C		132		
Short-Circuit Response Time		150mV overdrive, C_{LOAD} = 0, to GATE below 1V			330	500	ns
INPUT-VOLTAGE STEP PROTECTION							
Input-Voltage-Step Detection Threshold	$STEP_{TH}$			1.219	1.25	1.281	V
Input-Voltage-Step Threshold Offset Current	I_{STEP_OS}			-10.8	-10	-9.2	µA
LOAD-PROBE CIRCUIT							
Load-Probe Switch On-Resistance		V_{LP} - V_{EE} = 1V			7.5	11	Ω
Load-Probe Timeout	t_{LP}			80	220	380	ms
Load-Probe Retry Time	t_{LP_OFF}				16 x t_{LP}		s
Shorted Load Detection Voltage Threshold	V_{TH_LP}	Referenced to GND		-220	-200	-180	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -10V to -80V, V_{IN} = (GND - V_{EE}), V_{STEP_MON} = V_{EE}, R_{LP} = 200Ω, V_{ON} = V_{OFF} = 2V, V_{OV} = V_{CB_ADJ} = V_{EE}, POL_SEL open, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{EE} = -48V, T_A = +25°C.) (Notes 1, 2)

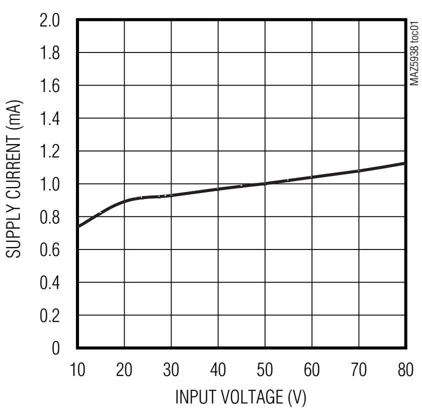
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND FAULT MANAGEMENT						
Autoretry Delay	t_{RETRY}			16 x t_{LP}		s
PGOOD Assertion Threshold		$\lvert V_{OUT} - V_{EE} \rvert$ falling		0.74 x V_{CB}		mV
		Hysteresis		0.26 x V_{CB}		
PGOOD Assertion Delay Time (Note 6)	t_{PGOOD}		0.70	1.26	1.85	ms
PGOOD Low Voltage	V_{OL}	I_{SINK} = 1mA, referenced to V_{OUT}, V_{OUT} < (GND - 5V)		0.05	0.4	V
PGOOD Open-Drain Leakage	I_L	V_{EE} = -80V, PGOOD = GND		0.01	1	µA

Note 1: All currents into pins are positive and all currents out of pins are negative. All voltages referenced to V_{EE}, unless otherwise specified.
Note 2: All limits are 100% tested at +25°C and +85°C. Limits at -40°C and -10°C are guaranteed by characterization.
Note 3: V_{ON} drops below the $V_{ON\_REF,F}$ threshold are ignored during this time.
Note 4: Delay time from a valid on condition until the load-probe test begins.
Note 5: The short-circuit threshold is V_{SC} = 2 x V_{CB}.
Note 6: The time when PGOOD condition is met until PGOOD signal is asserted.

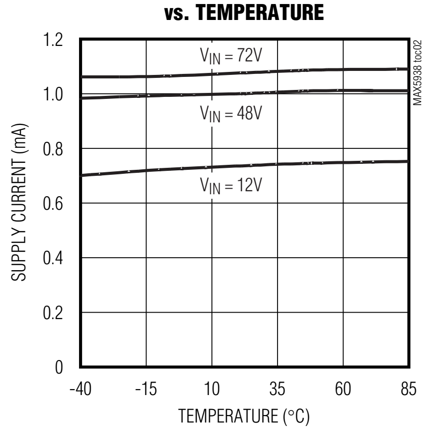
Typical Operating Characteristics

(V_{EE} = -48V, GND = 0V, V_{IN} = GND - V_{EE}, POL_SEL = floating, all voltages are referenced to V_{EE}, unless otherwise noted. T_A = +25°C, unless otherwise noted.)

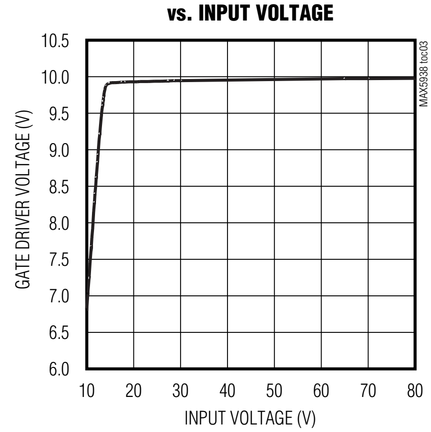
SUPPLY CURRENT vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



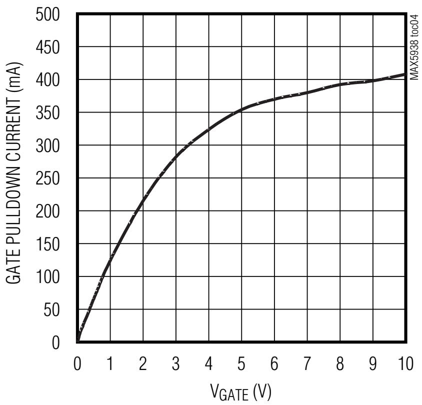
GATE-DRIVE VOLTAGE vs. INPUT VOLTAGE



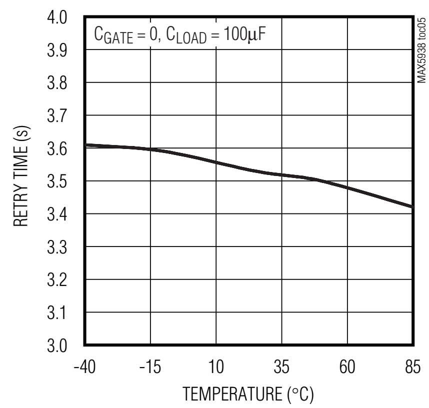
Typical Operating Characteristics (continued)

(V_{EE} = -48V, GND = 0V, V_{IN} = GND - V_{EE}, POL_SEL = floating, all voltages are referenced to V_{EE}, unless otherwise noted. T_A = +25°C, unless otherwise noted.)

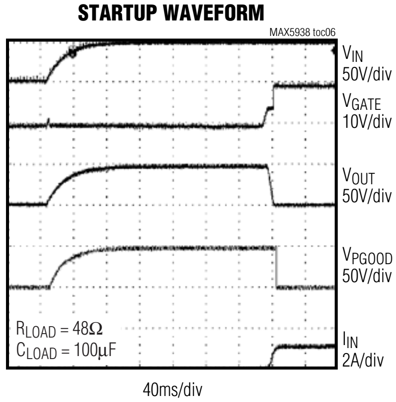
GATE PULLDOWN CURRENT vs. GATE VOLTAGE



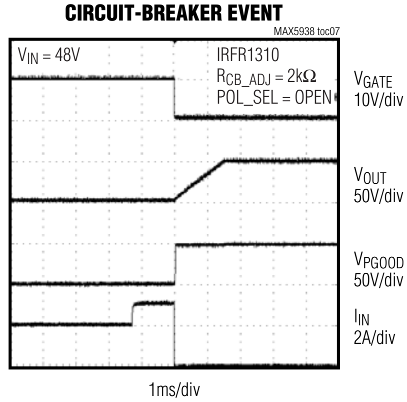
RETRY TIME vs. TEMPERATURE



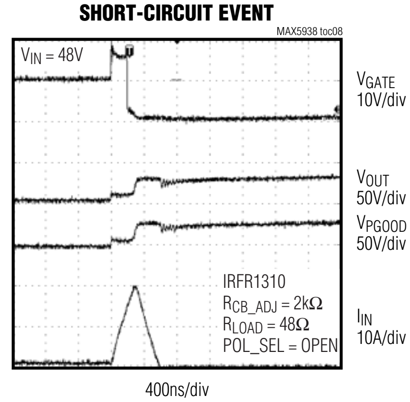
STARTUP WAVEFORM



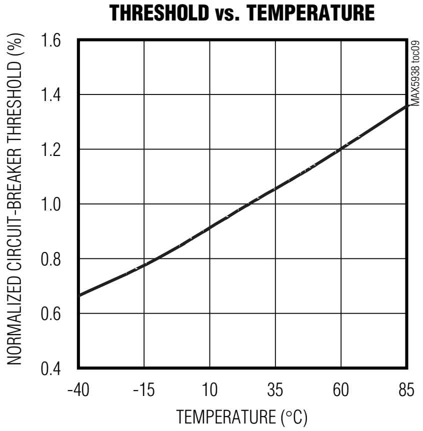
CIRCUIT-BREAKER EVENT



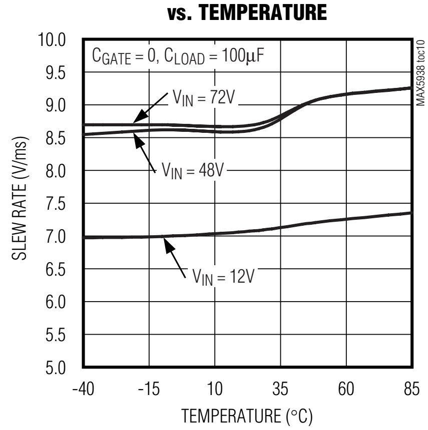
SHORT-CIRCUIT EVENT



NORMALIZED CIRCUIT-BREAKER THRESHOLD vs. TEMPERATURE



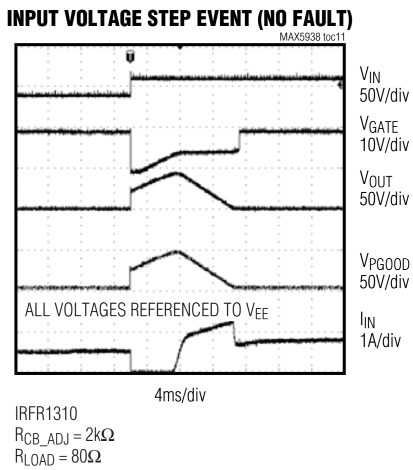
V_{OUT} SLEW RATE vs. TEMPERATURE

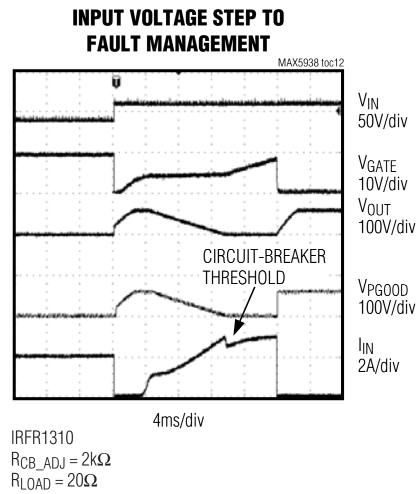


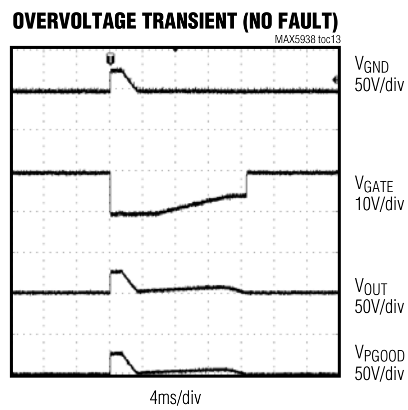
-48V Hot-Swap Controller with V_{IN} Step Immunity, No R_{SENSE}, and Overvoltage Protection

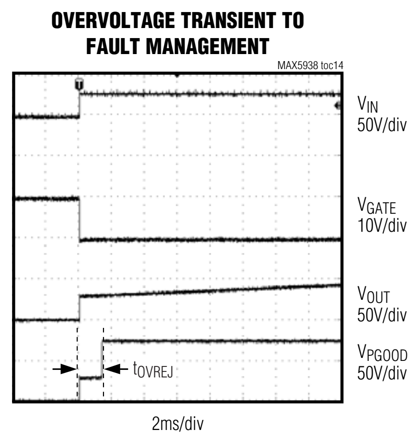
Typical Operating Characteristics (continued)

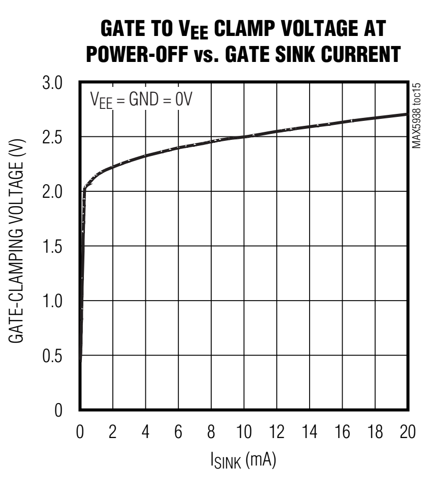
(V_{EE} = -48V, GND = 0V, V_{IN} = GND - V_{EE}, POL_SEL = floating, all voltages are referenced to V_{EE}, unless otherwise noted. T_A = +25°C, unless otherwise noted.)

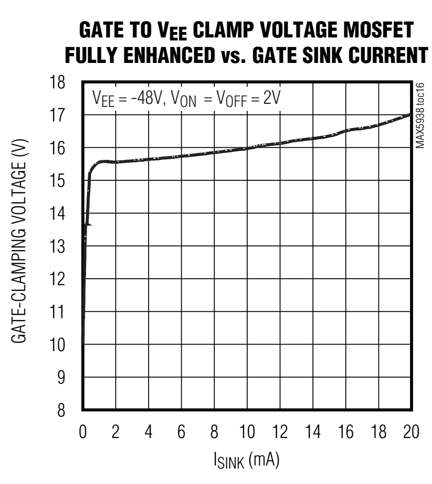












Pin Description

PIN	NAME	FUNCTION
1	GND	Ground. The high supply connection for a negative rail hot-swap controller.
2, 10, 13, 15	N.C.	No Connection. Not internally connected. Leave open.
3	OFF	Off Control Input. Referenced to V_{EE}. Drive OFF and ON above 1.25V (typ) to turn on the MAX5938. When the ON input low requirements are met and OFF falls below 1.25V (typ), the MAX5938 turns off.
4	ON	On Control Input. Referenced to V_{EE}. Drive ON and OFF above the 1.25V rising thresholds to turn on the MAX5938. When the voltage at OFF falls below its 1.25V (typ) threshold and the voltage at ON falls below 1.125V for longer than the ON 1.5ms glitch rejection period, the MAX5938 turns off.
5	OV	Overvoltage Control Input. Referenced to V_{EE}. When the voltage at OV rises above the 1.25V rising threshold, GATE pulls to V_{EE} until OV falls below the 1.125V falling threshold. If the overvoltage condition remains longer than 1.5ms, fault management initiates and PGOOD deasserts (see the *Detailed Description*).
6	STEP_MON	Input Voltage Step Monitor. Connect a resistor between STEP_MON and V_{EE} to set the step sensitivity. Connect a capacitor from GND to STEP_MON to adjust the step response relative to a negative step at V_{EE} to eliminate false circuit-breaker and short-circuit faults. Connect to V_{EE} to disable the step immunity function. See the *Selecting Resistor and Capacitor Values for Step Monitor* section in the *Applications Information*.
7	POL_SEL	PGOOD Output Polarity Select. Leave POL_SEL open for an active-low PGOOD assertion. Connect POL_SEL to V_{EE} for an active-high open-drain PGOOD assertion.
8	V_{EE}	Negative Input Voltage
9	LP	Load-Probe Detect. Connect a resistor from LP to V_{OUT} to set the load-probe test current. **Limit load-probe test current to 1A.** Connect to V_{EE} to disable load-probe function.
11	GATE	Gate-Drive Output. Connect to the gate of the external n-channel MOSFET.
12	CB_ADJ	Circuit-Breaker Adjust. Connect a resistor from CB_ADJ to V_{EE} to adjust the circuit-breaker threshold. Short CB_ADJ to V_{EE} for the default circuit-breaker 50mV (typ) threshold. Leave CB_ADJ open to disable circuit-breaker and short-circuit fault detection.
14	V_{OUT}	Output Voltage Sense. V_{OUT} is the negative rail of the load. Connect to the drain of the external n-channel MOSFET.
16	PGOOD	Power-Good Open-Drain Output. Referenced to V_{OUT}. PGOOD asserts high (POL_SEL = V_{EE}) or low (POL_SEL open) when V_{OUT} is within limits and there is no fault condition. PGOOD is deasserted when ON and OFF are cycled low.

Detailed Description

The MAX5938 hot-swap controller incorporates overcurrent and overvoltage fault management and is intended for negative-supply-rail applications. The MAX5938 eliminates the need for an external R_{SENSE} and includes V_{IN} input step protection and load probe, which prevents powering up into a shorted load. It is intended for negative 48V telecom power systems where low cost, flexibility, multifault management, and compact size are required. The MAX5938 is ideal for the widest range of systems from those requiring low current with small MOSFETs to high-current systems requiring large power MOSFETs and low on-resistance.

The MAX5938 controls an external n-channel power MOSFET placed in the negative supply path of an external load. When no power is applied, the GATE output of the MAX5938 clamps the V_{GS} of the MOSFET to 2V keeping the MOSFET turned off (Figure 2). When power is applied to the MAX5938, the 2V clamp at the GATE output is replaced by a strong pulldown device, which pulls GATE to V_{EE} and the V_{GS} of the MOSFET to 0. As shown in Figure 2, this transition enables the MAX5938 to keep the power MOSFET continually off during the board insertion phase when the circuit board first makes contact with the backplane. Without this clamp, the GATE output of a powered-down controller would be floating and the MOSFET reverse transfer

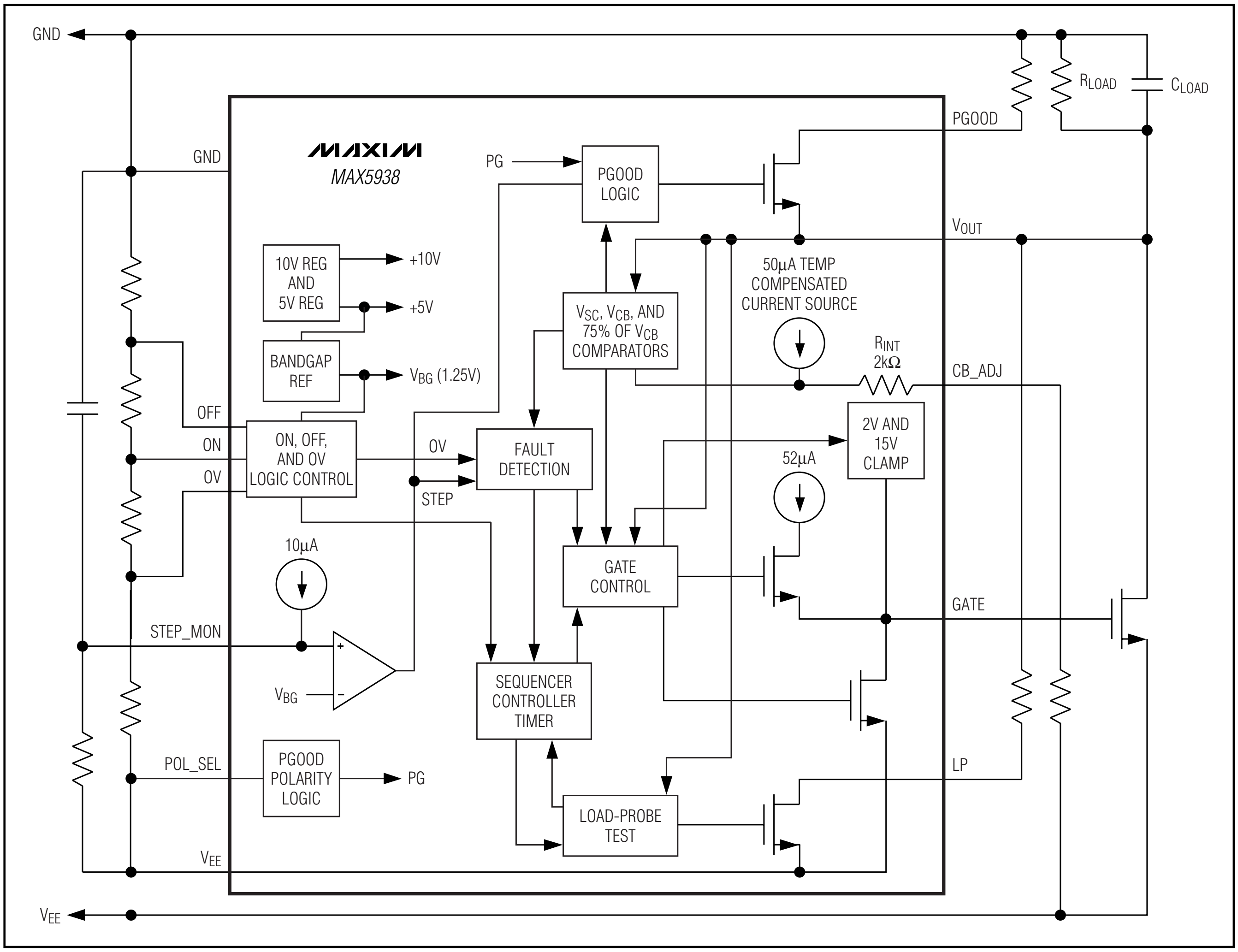


Figure 1. Functional Diagram

capacitance (gate-to-drain) would pull up and turn on the MOSFET gate when the MOSFET drain is rapidly pulled up by the V_{IN} step during backplane contact. The MAX5938 GATE clamp can overcome the gate-to-drain capacitance of large power MOSFETs with added slew-rate control (C_{SLEW}) capacitors while eliminating the need for additional gate-to-source capacitance. The MAX5938 keeps the MOSFET off indefinitely if the supply voltage is below the user-set ON and OFF thresholds, if the supply voltage is above the user-set overvoltage (OV) threshold, or if a short circuit (user-defined) is detected in the load connected to the drain of the power MOSFET.

The MAX5938 conducts a load-probe test after contact transients from the hot plug-in have settled. This follows the MAX5938 power-up (when the ON, OFF, and OV conditions have been met for 220ms (t_{LP})) and prior to the turn-on of the power MOSFET. This test pulls a user-programmable current through the load (1A, max) for up to 220ms (t_{LP}) and tests for a voltage of 200mV across the load at V_{OUT} (Figure 3). This current is set by an external resistor, R_{LP} (Figure 17) between V_{OUT} and LP. When the voltage across the load exceeds 200mV, the test is truncated and the GATE turn-on sequence is started. If at the end of the 200ms (t_{LP}) test period the voltage across the load has not reached 200mV, the load is assumed to be shorted and the current to the load from

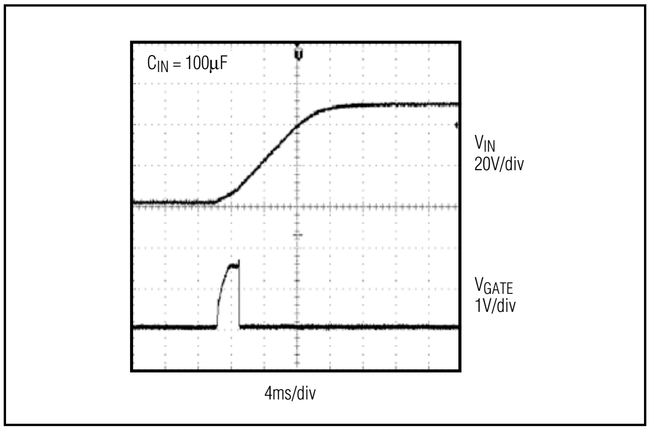


Figure 2. GATE Voltage Clamp During Power-Up

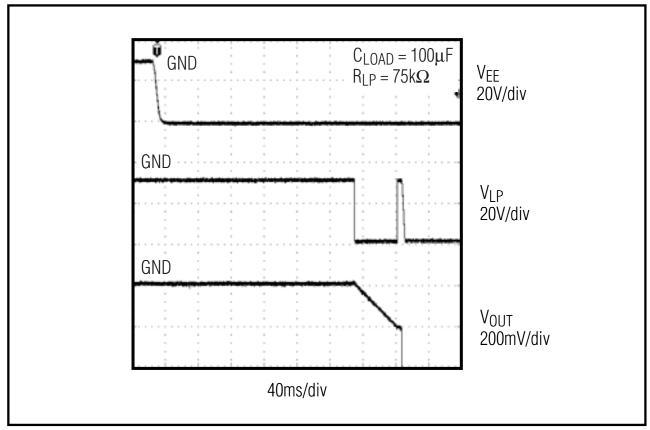


Figure 3. Load-Probe Test During Initial Power-Up

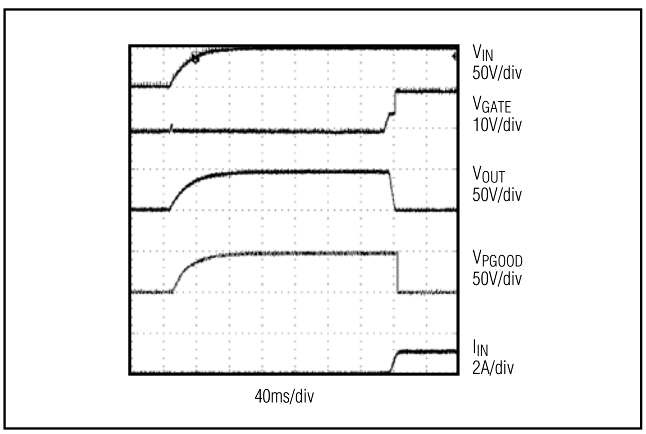


Figure 4. MAX5938 Normal Startup (POL_SEL = Floating)

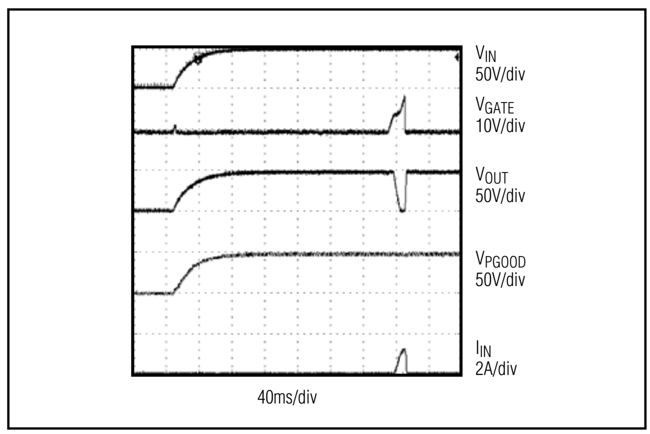


Figure 5. MAX5938 Startup into Fault Condition (POL_SEL = Floating)

LP is shut off. The MAX5938A times out for 16 x t_{LP} then retry the load-probe test. The MAX5938L latches the fault condition indefinitely until ON and OFF are cycled low for 1.5ms or the power is recycled. See the *Applications Information* for recommendations on selecting R_{LP} to set the load-probe current level.

Upon successful completion of the load-probe test, the MAX5938 enters the power-up GATE cycle and begins ramping the GATE voltage with a 52μA current source. This current source is restricted if V_{OUT} begins to ramp down faster than the default 9V/ms slew rate. The V_{OUT} slew rate can be reduced to below 9V/ms by adding C_{SLEW} from GATE to V_{OUT}. Charging up GATE enhances the power MOSFET in a controlled manner and ramping V_{OUT} at a user-settable rate controls the inrush current from the backplane. The MAX5938 continues to charge up the GATE until one of two events occurs: a normal power-up GATE cycle is completed or a power-up-to-fault-management fault is detected (see the *GATE Cycles* section in *Appendix A*). In a normal power-up GATE cycle, the voltage at V_{OUT} (referenced to V_{EE}) ramps to below 74% of the programmed circuit-breaker threshold voltage, V_{CB}. At this time, the remaining GATE voltage is rapidly pulled up to full enhancement. PGOOD is asserted 1.26ms after GATE is fully enhanced (see Figure 4). If the voltage at V_{OUT} remains above 74% of the programmed V_{CB} (when GATE reaches 90% of full enhancement), then a power-up-to-fault-management fault has occurred). GATE is rapidly pulled to V_{EE}, turning off the power MOSFET and disconnecting the load. PGOOD remains deasserted and the MAX5938 enters the fault management mode (Figure 5).

When the power MOSFET is fully enhanced, the MAX5938 monitors the drain voltage (V_{OUT}) for circuit-breaker and short-circuit faults. The MAX5938 makes use of the power MOSFET's $R_{DS(ON)}$ as the current-sense resistance to detect excessive current through the load. The short-circuit threshold voltage, V_{SC}, is twice V_{CB} ($V_{SC} = 2 \times V_{CB}$) and is set by adjusting the resistance between CB_ADJ and V_{EE}. There is an internal 2kΩ precision-trimmed resistor and an internal 50µA current source at CB_ADJ, which results in the minimum or default V_{SC} of 100mV when CB_ADJ is connected to V_{EE}. The current source is temperature compensated (increasing with temperature) to track the normalized temperature coefficient of $R_{DS(ON)}$ for typical power MOSFETs.

When the load current is increased during full enhancement, this causes V_{OUT} to exceed V_{CB} but remains less than V_{SC}, and starts the 1.2ms circuit-breaker glitch rejection timer. At the end of the glitch rejection period, if V_{OUT} still exceeds V_{CB}, the GATE is immediately pulled to V_{EE} (330ns), PGOOD is deasserted, and the part enters fault management. Alternatively, during full enhancement when V_{OUT} exceeds V_{SC}, there is no glitch rejection timer. GATE is immediately pulled to V_{EE}, PGOOD is deasserted, and the part enters fault management.

The V_{IN} step immunity provides a means for transitioning through a large step increase in V_{IN} with minimal backplane inrush current and without shutting down the load. Without V_{IN} step immunity (when the power MOSFET is fully enhanced), a step increase in V_{IN} will result in a high inrush current and a large step in V_{OUT}, which can trip the circuit breaker.

With V_{IN} step immunity, the STEP_MON input detects the step before a short circuit is detected at V_{OUT} and alters the MAX5938 response to V_{OUT} exceeding V_{SC} due to the step. The 1.25V voltage threshold at STEP_MON and a 10µA current source at STEP_MON allow the user to set the sensitivity of the step detection with an external resistor to V_{EE}. A capacitor is placed between GND and the STEP_MON input, which in conjunction with the resistor, sets the STEP_MON time constant.

When a step is detected by the STEP_MON input rising above its threshold ($STEP_{TH}$), the overcurrent fault management is blocked and remains blocked as long as $STEP_{TH}$ is exceeded. When $STEP_{TH}$ is exceeded, the MAX5938 takes no action until V_{OUT} rises above V_{SC} or above V_{CB} for the 1.2ms circuit-breaker glitch rejection period. When either of these conditions occurs, a step GATE cycle begins and the GATE is immediately brought to V_{EE}, which turns off the power MOSFET to minimize the resulting inrush current surge from the backplane. PGOOD remains asserted. GATE is held at V_{EE} for 350µs, and after about 1ms, begins to ramp up, enhancing the power MOSFET in a controlled manner as in the power-up GATE cycle. This provides a controlled inrush current to charge the load capacitance to the new supply voltage (see the *GATE Cycles* section in *Appendix A*).

As in the case of the power-up GATE cycle, if V_{OUT} drops to less than 74% of the programmed V_{CB}, independent of the state of STEP_MON, the GATE voltage is rapidly pulled to full enhancement. PGOOD remains asserted throughout the step (Figure 6). Otherwise, if the STEP_MON input has decayed below its threshold but V_{OUT} remains above 74% of the programmed V_{CB} (when GATE reaches 90% of full enhancement), a step-to-fault-management fault has occurred. GATE is rapidly pulled to V_{EE}, turning off the power MOSFET and disconnecting the load; PGOOD is deasserted and the MAX5938 enters the fault management mode (Figure 7).

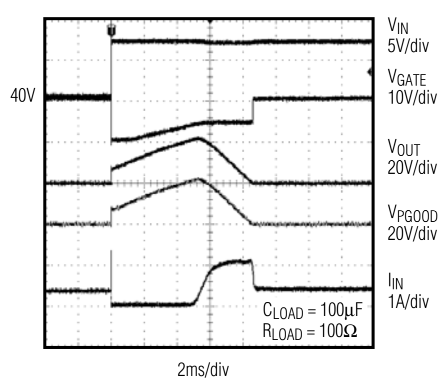


Figure 6. MAX5938 Response to a Step Input with No Fault ($V_{OUT} < 0.75V_{CB}$)

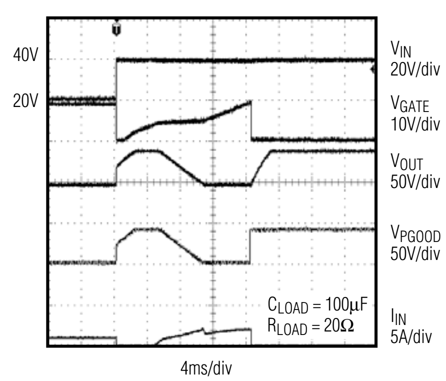


Figure 7. MAX5938 Response to a Step Input Ending in a Fault ($V_{OUT} > 0.75V_{CB}$)

Fault Management

Fault management can be triggered by the following conditions:

- V_{OUT} exceeds 74% of V_{CB} during GATE ramp at 90% of full enhancement,
- V_{OUT} exceeds the V_{CB} for longer than 1.2ms during full enhancement,
- V_{OUT} exceeds the V_{SC} during full enhancement,
- Load-probe test fails,
- V_{IN} exceeds the programmed overvoltage (OV) limit for more than 1.5ms.

Once in the fault management mode, GATE will always be pulled to V_{EE}, which turns off the external MOSFET and always deasserts PGOOD. If CB_ADJ is left open, short-circuit and circuit-breaker faults are ignored. The MAX5938A version has automatic retry following a fault while the MAX5938L remains latched in the fault condition.

Autoretry Fault Management (MAX5938A)

If the MAX5938A entered fault management due to an OV fault, it will start the autoretry timer when the OV fault is removed. For circuit-breaker and short-circuit faults, the autoretry timer starts immediately. The timer times out in 3.5s (typ) after which the sequencer initiates a load-probe test and if successful, initiates a normal power-up GATE cycle.

Latched Fault Management (MAX5938L)

When the MAX5938L enters fault management it remains in this condition indefinitely until the power is recycled or until OFF is brought below 1.25V (no time dependence) and ON is brought below 1.125V for 1.5ms (typ). In addition, if the MAX5938L enters fault management due to an overvoltage fault, the overvoltage fault must be removed. When the last of these conditions has been met, the sequencer initiates a load-probe test and if successful, a normal power-up GATE cycle begins. A manual reset circuit as in Figure 2 can be used to clear the latch.

Circuit-Breaker Threshold

The MAX5938 has a minimum circuit-breaker threshold voltage of 50mV when CB_ADJ is connected to V_{EE}. The V_{CB} is half V_{SC} and can be increased by placing a resistor between CB_ADJ and V_{EE} according to the following:

$$V_{CB}(mV) = 1/2 \times V_{SC}(mV) = 1/2 \times I_{CB\_ADJ}(\mu A) \times [R_{INT}(k\Omega) + R_{CB\_ADJ}(k\Omega)]$$

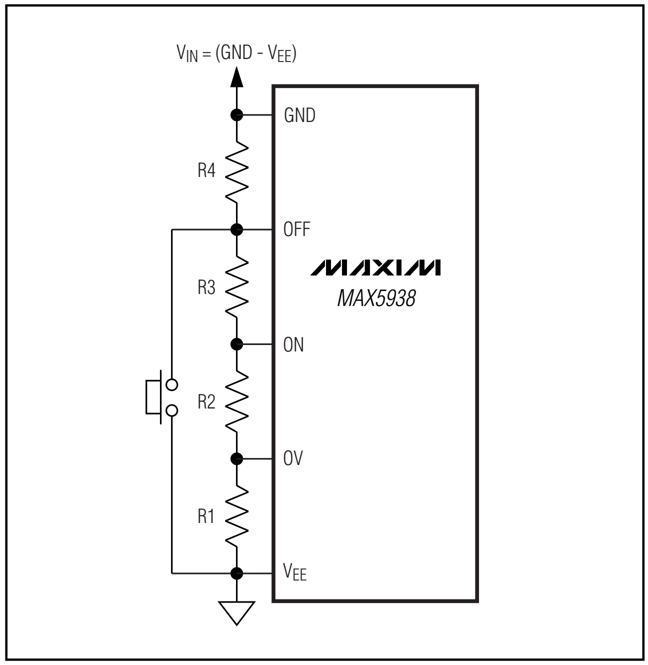


Figure 8. Resetting the MAX5938L after a Fault Condition Using a Push-Button Switch

where I_{CB_ADJ} = 50µA (typ at +25°C), R_{INT} is an internal precision, ±0.5%, 2kΩ resistor at CB_ADJ and R_{CB_ADJ} is the external resistor between CB_ADJ and V_{EE}. The current source I_{CB_ADJ} is temperature-compensated (increasing with temperature) to track the normalized temperature coefficient of typical power MOSFETs.

The proper circuit-breaker threshold for an application depends on the $R_{DS(ON)}$ of the external power MOSFET and the maximum current the load is expected to draw. To avoid false fault indication and dropping of the load, the designer must take into account the load response to voltage ripples and noise from the backplane power supply as well as switching currents in the downstream DC-DC converter that is loading the circuit. While the circuit-breaker threshold has glitch rejection that ignores ripples and noise lasting less than 1.2ms, the short-circuit detection is designed to respond very quickly (less than 330ns) to a short circuit. For this reason, set V_{SC} and V_{CB} with an adequate margin to cover all possible ripples, noise, and system current transients (see the *Setting the Circuit-Breaker and Short-Circuit Thresholds* section in the *Applications Information*).

Disabling Circuit-Breaker and Short-Circuit Functions

In the MAX5938, the circuit-breaker and short-circuit functions can be disabled, if desired, although this is not recommended. (See Warning note in the *PGOOD Open-Drain Output* section). This can be accomplished by leaving CB_ADJ open. In this case, PGOOD asserts 1.26ms after GATE has ramped to 90% of full enhancement, after which V_{OUT} is ignored, resulting in the circuit-breaker and short-circuit faults being ignored.

PGOOD Open-Drain Output

The power-good output, PGOOD, is open drain and is referenced to V_{OUT}. It asserts and latches if V_{OUT} ramps below 74% of V_{CB}, and with the built-in delay, this occurs 1.26ms after the external MOSFET becomes fully enhanced. PGOOD deasserts any time the part enters fault management. PGOOD has a delayed response to ON and OFF. The GATE will go to V_{EE} when OFF is brought below 1.25V (no time dependence) while ON is brought below 1.125V for 1.5ms. This turns off the power MOSFET and allows V_{OUT} to rise depending on the RC time constant of the load. PGOOD, in this situation, deasserts when V_{OUT} rises above V_{CB} for more than 1.4ms or above V_{SC}, whichever occurs first (see Figure 9b).

Since PGOOD is open drain, it requires an external pullup resistor to GND. Due to this external pullup, PGOOD does not follow positive V_{IN} steps as well as if it were driven by an active pullup. As a result, when PGOOD is asserted high, an apparent negative glitch appears at PGOOD during a positive V_{IN} step. This negative glitch is a result of the RC time constant of the external resistor and the PGOOD pin capacitance lagging the V_{IN} step. It is not due to switching of the internal logic. To minimize this negative transient, it may be necessary to increase the pullup current and/or to add a small amount of capacitance from PGOOD to GND to compensate for the pin capacitance.

The PGOOD output logic polarity is selected using POL_SEL input. For an active-high output, connect POL_SEL to V_{EE}. Leave POL_SEL open for an active-low output.

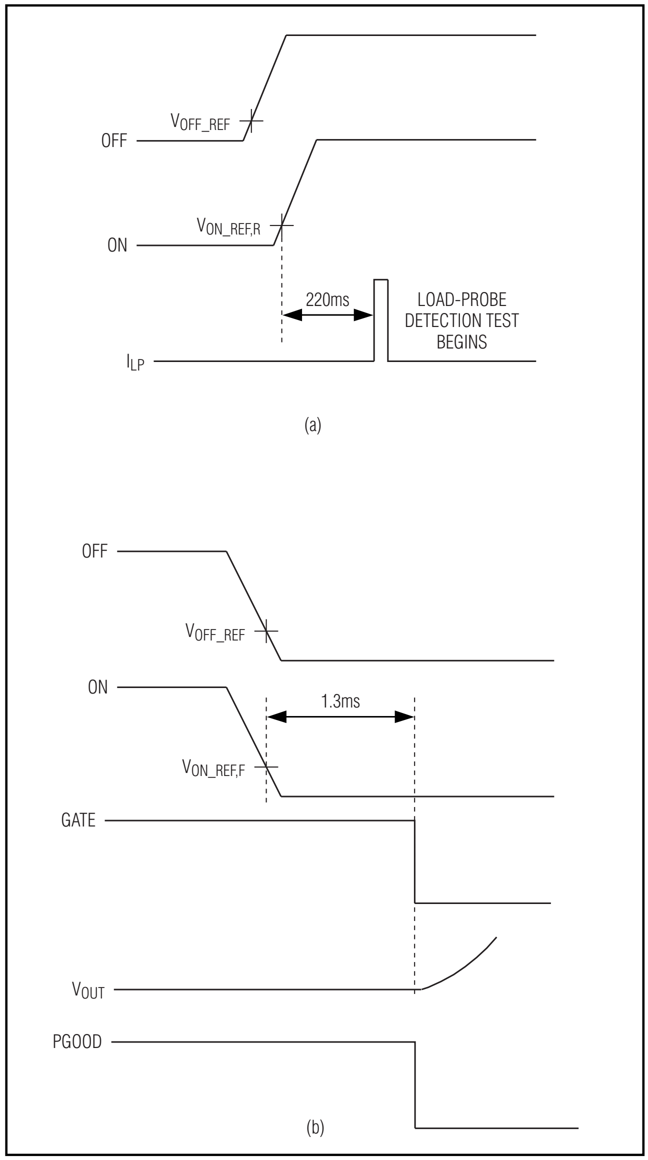


Figure 9. ON and OFF Timing Diagram

WARNING: When disabling the circuit-breaker and short-circuit functions (CB_ADJ open), PGOOD asserts 1.26ms after the power MOSFET is fully enhanced independent of V_{OUT}. Once the MOSFET is fully enhanced and ON and OFF are pulled below their respective thresholds, the GATE will be pulled to V_{EE} to turn off the power MOSFET and disconnect the load. When the circuit-breaker and short-circuit functions are disabled and ON and OFF are cycled low, PGOOD is deasserted. In summary, when CB_ADJ is open (once the MOSFET is fully enhanced), the MAX5938 ignores V_{OUT} and deasserts PGOOD only for an overvoltage fault, when ON and OFF are cycled low or when the power to the MAX5938 is fully recycled.

Undervoltage Lockout (OFF and ON) and OV Functions

OV, ON, and OFF provide an accurate means to set the overvoltage, turn-on, and turn-off voltage levels. All three are high-impedance inputs and by use of a 4-element resistor-divider from GND to V_{EE}, the user can set an upper V_{EE} threshold for triggering an overvoltage fault, a middle threshold for turning the part on, and a lower threshold for turning the part off.

The input voltage threshold at OFF is 1.25V. ON has hysteresis with a rising threshold of 1.25V and a falling threshold of 1.125V. The logic of the inputs is such that both OFF and ON must be above their thresholds to latch the part on. Both OFF and ON must be below their respective thresholds to latch the part off, otherwise the part stays in its current state. There is glitch rejection on the ON input going low, which additionally requires that ON remain below its falling threshold for 1.5ms to turn off the part. A startup delay of 220ms allows contacts and voltages to settle prior to initiating the startup sequence. This startup delay is from a valid ON condition until the start of the load-probe test.

The OV input has hysteresis with a rising threshold of 1.25V and a falling threshold of 1.125V. The OV input also has a rising fault transient delay of 1.5ms. When OV rises above its threshold, an OV GATE cycle is immediately initiated (see the *GATE Cycles* section in *Appendix A*). The GATE output is brought to V_{EE} with about 300ns of propagation delay. If the OV input drops below its falling threshold before the fault transient delay of about 1.5ms, the device will not enter fault management mode and the GATE output will ramp up to fully enhance the external MOSFET (Figure 10). Otherwise, an OV fault occurs (Figure 11). See the *Setting ON, OFF, and OV Voltage Levels* section in the *Applications Information*.

Output Voltage (V_{OUT}) Slew-Rate Control

The V_{OUT} slew rate controls the inrush current required to charge the load capacitor. The MAX5938 has a default internal slew rate set for 9V/ms. The internal circuit establishing this slew rate accommodates up to about 1000pF of reverse transfer capacitance (Miller Capacitance) in the external power MOSFET without effecting the default slew rate. Using the default slew rate, the inrush current required to charge the load capacitance is given by:

$$I_{INRUSH}\ (mA) = C_{LOAD}\ (\mu F) \times SR\ (V/ms)$$

where SR = 9V/ms (default, typ).

The slew rate can be reduced by adding an external slew-rate control capacitor (C_{SLEW}) from V_{OUT} (the drain of the power MOSFET) to the GATE output of the MAX5938 (Figure 19). Values of C_{SLEW} < 4700pF have little effect on the slew rate because of the default slew-rate control circuit. For C_{SLEW} > 4700pF, the combination of C_{SLEW} and reverse transfer capacitance of the external power MOSFET dominate the slew rate. When C_{SLEW} > 4700pF, SR and C_{SLEW} are inversely related as follows (Figure 18):

$$SR\ (V/ms) = 23 / C_{SLEW}\ (nF)$$

If the reverse transfer capacitance of the external power MOSFET is large compared to the externally added C_{SLEW}, then it should be added to C_{SLEW} in the equation above.

See the *Adjusting the V_{OUT} Slew Rate* section in the *Applications Information* and Figure 18, which graphically displays the relation between C_{SLEW} and slew rate. This section discusses specific recommendations for compensating power MOSFET parasitics that may lead to oscillation when an external C_{SLEW} is added.

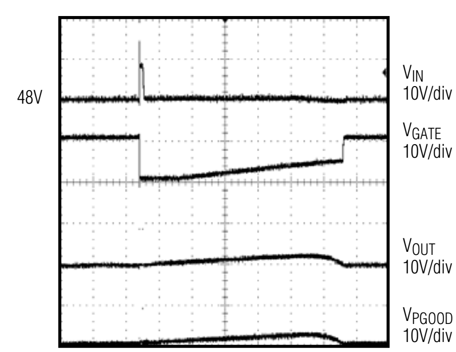


Figure 10. Overvoltage Gate Cycle Without a Fault (t_{OV} < 1.3ms)

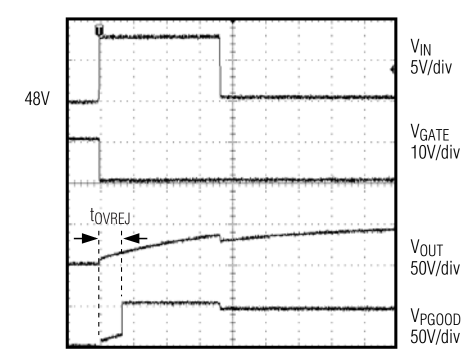


Figure 11. Overvoltage Fault (t_{OV} > 1.3ms)

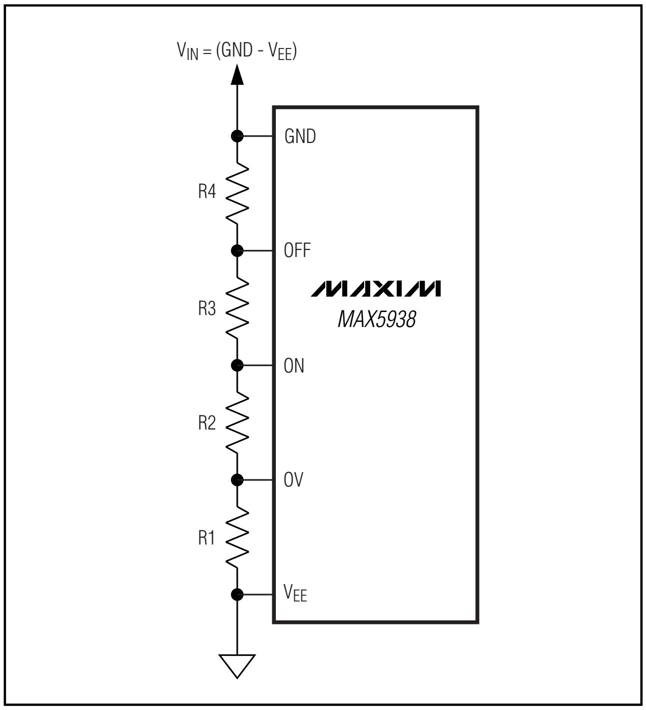


Figure 12. Programming the MAX5938's ON, OFF, and OV Thresholds

Applications Information

Setting ON, OFF, and OV Voltage Levels

The trip levels for ON, OFF, and OV can readily be set with a 4-element resistor-divider. Total resistance is a trade off of quiescent current, threshold tolerance due to pin input bias current (25nA), and the ability to follow very fast supply transients. Both ON and OV have hysteresis on the reference threshold voltage: the rising reference threshold is 1.25V and the falling threshold is 1.125V. The reference threshold voltage for OFF is 1.25V. In determining a set of resistors, use V_{REF} = 1.25V for ON, OFF, and OV and an R_{TOT} = 100kΩ in this example. See Figure 12 for nomenclature. For this example, use V_{OV} = 80V, V_{ON} = 42V, and V_{OFF} = 38V as the desired voltage trip levels.

1) $R_4 = R_{TOT} \times V_{REF} / V_{OV}$

2) $R_3 = R_{TOT} \times V_{REF} / V_{ON} - R_4$

3) $R_2 = R_{TOT} \times V_{REF} / V_{OFF} - R_3 - R_4$

4) $R_1 = R_{TOT} - R_2 - R_3 - R_4$

The exact result to three decimal places is R1 = 96.711kΩ, R2 = 313Ω, R3 = 1.414kΩ, and R4 = 1.563kΩ. When converted to the nearest 1% standard resistor, the values become R1 = 97.6kΩ, R2 = 316Ω, R3 = 1.40kΩ, and R4 = 1.58kΩ.

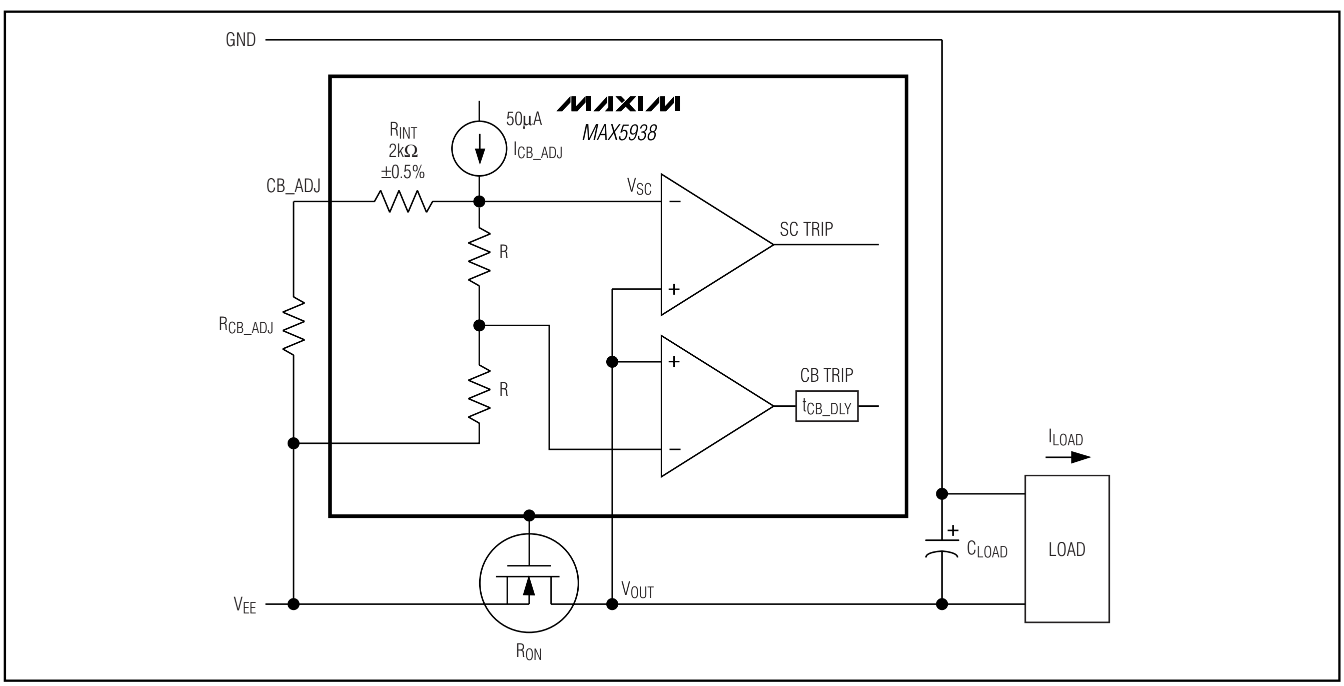


Figure 13. MAX5938 Circuit-Breaker Threshold Adjustment

Determine the trip voltages these values will actually yield for rising and falling voltages. Rising voltages use the V_{REF} = 1.25V reference threshold, while falling voltages use V_{LO} = 1.125V reference threshold.

1) $R_{TOT} = R_1 + R_2 + R_3 + R_4$

2) $V_{OV,RISING} = V_{REF} \times R_{TOT} / R_4$

3) $V_{OV,FALLING} = V_{LO} \times R_{TOT} / R_4$

4) $V_{ON,RISING} = V_{REF} \times R_{TOT} / (R_3 + R_4)$

5) $V_{ON,FALLING} = V_{LO} \times R_{TOT} / (R_3 + R_4)$

6) $V_{OFF} = V_{REF} \times R_{TOT} / (R_2 + R_3 + R_4)$

The resulting voltage levels are $V_{OV,RISING}$ = 79.82V ±2.5%, $V_{OV,FALLING}$ = 71.84V ±5%, $V_{ON,RISING}$ = 42.32V ±2.5%, $V_{ON,FALLING}$ = 38.09V ±5%, and V_{OFF} = 38.26V ±2.5%. The voltage tolerance does not account for the tolerance of the resistors.

Setting the Circuit-Breaker and Short-Circuit Thresholds

The MAX5938 can operate with a wide range of power MOSFETs to meet the requirements of almost any application. MOSFETs mentioned here are done to demonstrate certain capabilities and features of the MAX5938. They should not be construed as a recommendation or a limitation of the interoperability of the MAX5938.

In the implementation of the circuit-breaker and short-circuit functions, the MAX5938 eliminates the need for an external current-sense resistor at the source of the power MOSFET. As in any other hot-swap controller, the proper circuit-breaker threshold for an application must take into account the DC level of V_{OUT}, while at the same time accommodating the AC response of V_{OUT} to the modulation of V_{IN}. The AC response from V_{IN} to V_{OUT} is dependent on the parasitics of the load, especially the load capacitor, in conjunction with the $R_{DS(ON)}$ of the power MOSFET. It behaves as a highly dampened second-order system. As such, this system functions as a bandpass filter from V_{IN} to V_{OUT}. The response of V_{OUT} to load-switching currents and voltage ripple and noise from the backplane power supply must be taken into account. Adequate margin must be provided between V_{CB}, V_{SC}, and the DC level of V_{OUT}, which depends on the $R_{DS(ON)}$ of the power MOSFET (with V_{GS} at 10V) and the maximum current the load is expected to draw. While the circuit-breaker threshold has glitch rejection for V_{OUT} excursions lasting less than 1.4ms, the short-circuit detection is designed to respond very quickly (less than 330ns) to a short circuit. In the application, select a value for R_{CB_ADJ} resulting in a V_{CB} that exceeds the product of $R_{DS(ON)}$ and the maximum load current plus one half the peak-to-peak AC response of V_{OUT} to load-switching currents and the noise and ripple at V_{IN}:

$$R_{DS(ON)}\,(\Omega) \times I_{LOAD,MAX}(\text{mA}) + 1/2 \times VOUT_{AC} < V_{CB}(\text{mV})$$

where

$$V_{CB}(\text{mV}) = 1/2 \times I_{CB\_ADJ}(\mu\text{A}) \times [R_{INT}(\text{k}\Omega) + R_{CB\_ADJ}(\text{k}\Omega)]$$

$R_{DS(ON)}$ in a power MOSFET has a positive temperature coefficient and the MAX5938, when placed adjacent to the power MOSFET, tracks and compensates for this temperature coefficient. In the MAX5938, V_{CB} is half of V_{SC}, which is set by placing an external resistance between CB_ADJ and V_{EE}. The minimum (default) short-circuit threshold voltage, V_{SC}, is set by an internal 2kΩ precision-trimmed (±0.5%) resistor providing a minimum series resistance and a temperature-compensated 50µA (+25°C) current source. When CB_ADJ is connected to V_{EE} this gives a 50mV circuit-breaker threshold. When an external resistor, R_{CB_ADJ}, is placed between CB_ADJ and V_{EE}, the new circuit-breaker threshold becomes:

$$V_{CB}\,(\text{mV}) = 1/2 \times V_{SC}\,(\text{mV}) = 1/2 \times I_{CB\_ADJ}\,(\mu\text{A}) \times (2\text{k}\Omega + R_{CB\_ADJ})$$

and at +25°C, it becomes:

$$V_{CB}\,(\text{mV}) = 1/2 V_{SC}\,(\text{mV}) = 1/2 \times 50\mu\text{A} \times (2\text{k}\Omega + R_{CB\_ADJ})$$

The short-circuit and circuit-breaker voltages are sensed at V_{OUT}, which is the drain of the power MOSFET. The $R_{DS(ON)}$ of the MOSFET is the current-sense resistance and so the total current through the load and load capacitance is the drain current of the power MOSFET. Accordingly, the voltage at V_{OUT} as a function of MOSFET drain current is:

$$V_{OUT} = I_{D,MOSFET} \times R_{DS(ON)}$$

The temperature compensation of the MAX5938 is designed to track the $R_{DS(ON)}$ of the typical power MOSFET. Figure 14 shows the typical normalized tempco of the circuit-breaker threshold along with the normalized tempco of $R_{DS(ON)}$ for several typical power MOSFETS. When determining the circuit-breaker threshold in an application go to the power MOSFET manufacturer's data sheet and locate the maximum $R_{DS(ON)}$ at +25°C with a V_{GS} of 10V. Next, find the figure presenting the tempco of normalized $R_{DS(ON)}$ or on-resistance vs. temperature. Since this curve is in normalized units, typically with a value of 1 at +25°C, it is possible to multiply the curve by the drain voltage at +25°C and convert the curve to drain voltage. Now compare this curve to that of the MAX5938 normalized tempco of the circuit-breaker threshold to make a determination of the tracking error in mV between the power MOSFET [$I_{D,MOSFET}$ x $R_{DS(ON)}$] and the MAX5938 [I_{CB_ADJ} (µA) x (2kΩ + R_{CB_ADJ})] over the operating temperature range of the application.

If the tempco of the power MOSFET is greater than the MAX5938's, then additional margin in setting the circuit-breaker and short-circuit voltages will be required at higher temperatures as compared to +25°C (Figure 15). When dissipation in the power MOSFET is expected to lead to local temperature elevation relative to ambient conditions, it becomes imperative that the MAX5938 be located as close as possible to the power MOSFET. The marginal effect of temperature differences on circuit-breaker and short-circuit voltages can be estimated from a comparative plot such as Figure 14.

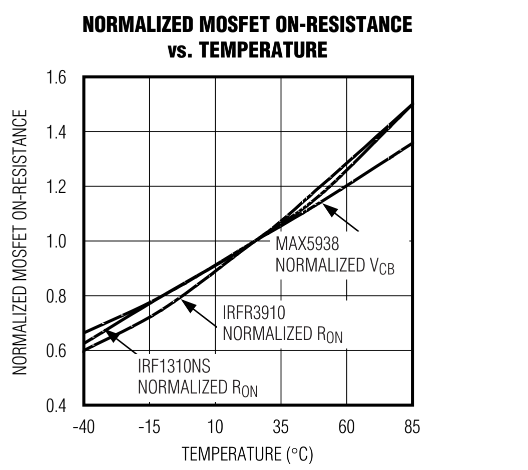


Figure 14. MAX5938 Normalized Circuit Breaker

Selecting a Resistor and Capacitor for Step Monitor

When a positive V_{IN} step or ramp occurs, the V_{IN} increase results in a voltage rise at both STEP_MON and V_{OUT} relative to V_{EE}. When the voltage at STEP_MON is above $STEP_{TH}$, the MAX5938 blocks short-circuit and circuit-breaker faults. During this STEP_MON high condition, if V_{OUT} rises above V_{SC}, the MAX5938 will immediately and very rapidly pull GATE to V_{EE}. This turns off the power MOSFET to avoid inrush current spiking. GATE is held low for 350µs. About 1ms after the start of GATE pulldown, the MAX5938 begins to ramp GATE up to turn on the MOSFET in a controlled manner that results in ramping V_{OUT} down to the new supply level (see the *GATE Cycles* section in *Appendix A*). This occurs with the least possible disturbance to V_{OUT}, although during the brief period that the MOSFET is off, the voltage across the load droops slightly depending on the load current and load storage capacitance. PGOOD remains asserted throughout the V_{IN} step event.

The objective in selecting the resistor and capacitor for the step monitor function is to ensure that the V_{IN} steps of all anticipated slopes and magnitudes will be properly detected and blocked, which otherwise would result in a circuit-breaker or short-circuit fault. The following is a brief analysis for finding the resistor and capacitor. For a more complete analysis, see *Appendix B*.

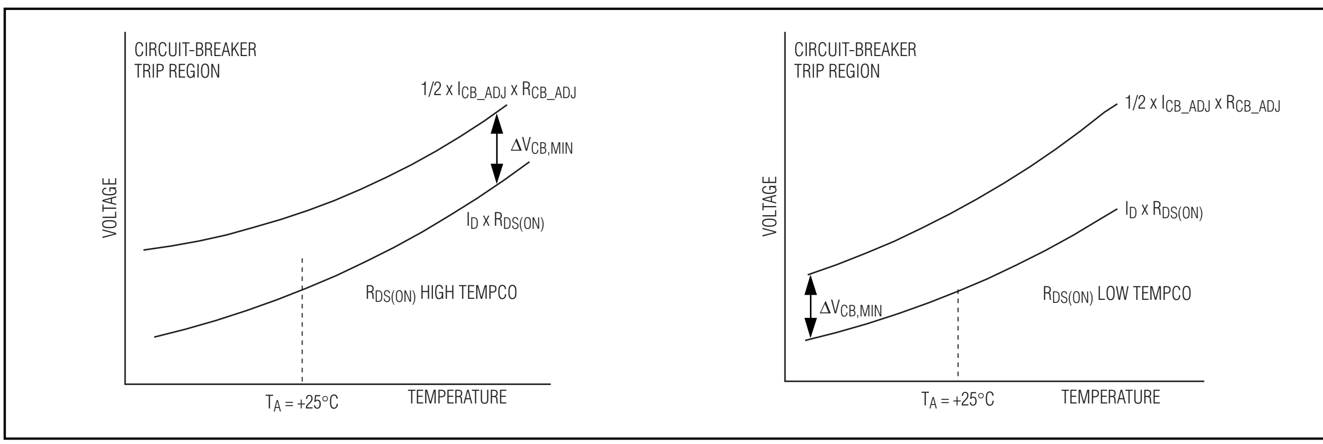


Figure 15. Circuit-Breaker Voltage Margin For High and Low Tempco Power MOSFETS

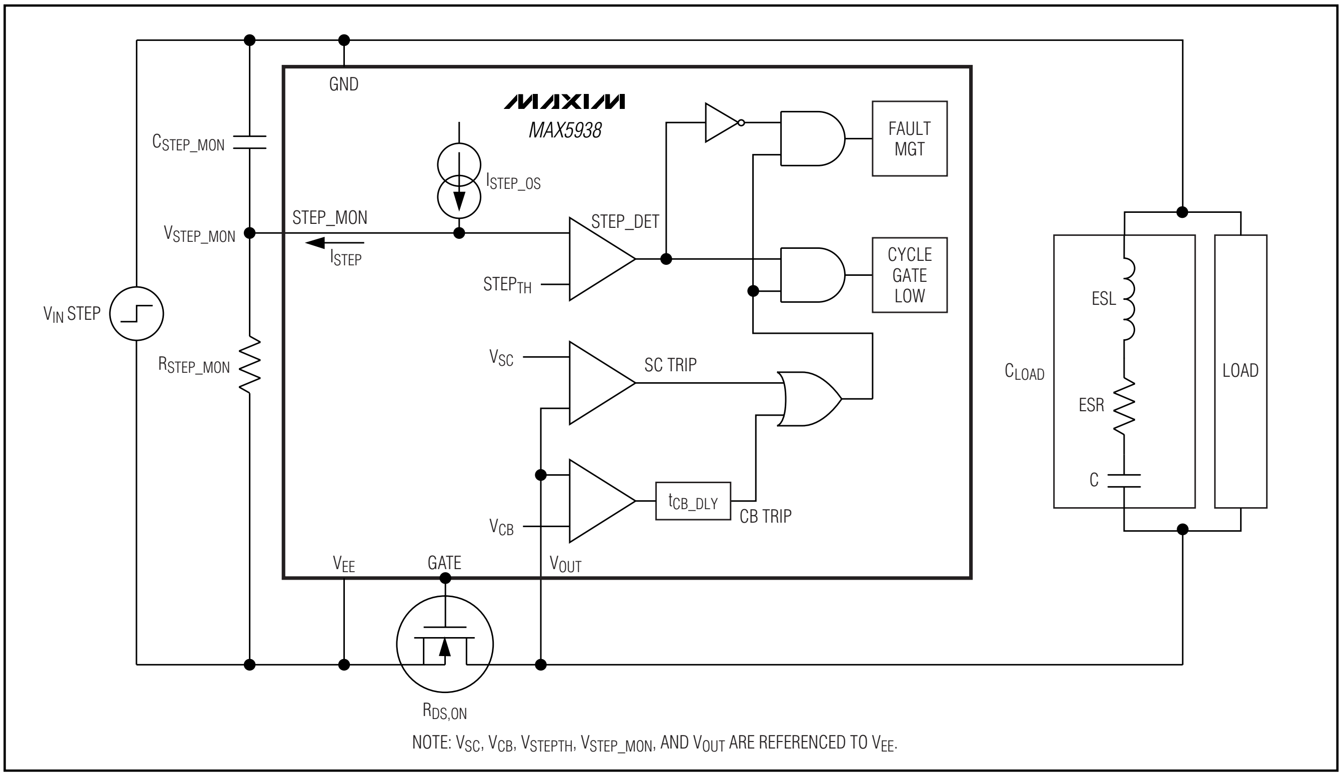


Figure 16. MAX5938 Step Immunity Functional Diagram

Figure 16 is a functional diagram exhibiting the elements of the MAX5938 involved in the step immunity function. This functional diagram shows the parallel relationship between V_{OUT} and $V_{STEP\text{-}MON}$. Each has an I*R component establishing the DC level prior to a step. While it is referred to as a V_{IN} step, it is the dynamic response to a finite voltage ramp that is of interest.

Given a positive V_{IN} ramp with a ramp rate of dV/dt, the approximate response of V_{OUT} to V_{IN} is:

$$V_{OUT}(t) = (dV/dt) \times \tau_C \times (1-e^{(-t\,/\,\tau L,eqv)}) + R_{DS(ON)}\, I_{LOAD}$$

where $\tau_C = C_{LOAD} \times R_{DS(ON)}$ and $\tau L,eqv$ is the equivalent time constant of the load that must be found empirically (see *Appendix B*).

Similarly, the response of STEP_MON to a V_{IN} ramp is:

$$V_{STEP\_MON}(t) = (dV/dt) \times \tau_{STEP} \times (1-e^{(-t\,/\,\tau STEP)}) + 10\mu A \times R_{STEP}$$

where $\tau_{STEP} = R_{STEP\_MON} \times C_{STEP\_MON}$.

For proper step detection, V_{STEP_MON} must exceed $STEP_{TH}$ prior to V_{OUT} reaching V_{SC} or within 1.4ms of V_{OUT} reaching V_{CB} (over all V_{IN} ramp rates anticipated in the application). V_{STEP_MON} must be set below $STEP_{TH}$ with an adequate margin, ΔV_{STEP_MON}, to accommodate the tolerance of both I_{STEP_OS} (±8%) and R_{STEP_MON}. R_{STEP_MON} is typically set to 100kΩ, which gives a ΔV_{STEP_MON} for a worst-case high of 0.36V.

The margin of V_{OUT}, with respect to V_{SC} and V_{CB}, was set when R_{CB_ADJ} was selected as described in the *Setting the Circuit-Breaker and Short-Circuit Thresholds* section. This margin may be lower at one of the temperature extremes and if so, that value should be used in the following discussion. These margins will be called ΔV_{CB} and ΔV_{SC} and they represent the minimum V_{OUT} excursion required to trip the respective fault.

To set τ_{STEP} to block all V_{CB} and V_{SC} faults for any ramp rate, find the ratio of ΔV_{STEP_MON} to ΔV_{CB} and choose τ_{STEP} so:

$$\tau_{STEP} = 1.2 \times \tau_C \times \Delta V_{STEP\_MON} / \Delta V_{CB}$$

And since R_{STEP_MON} = 100kΩ. This results in $C_{STEP\_MON} = \tau_{STEP}$ / 100kΩ.

After the first-pass component selection, if sufficient timing margin exists (see *Appendix B*), it is possible but not necessary to lower R_{STEP_MON} below 100kΩ to reduce the sensitivity of STEP_MON to V_{IN} noise.

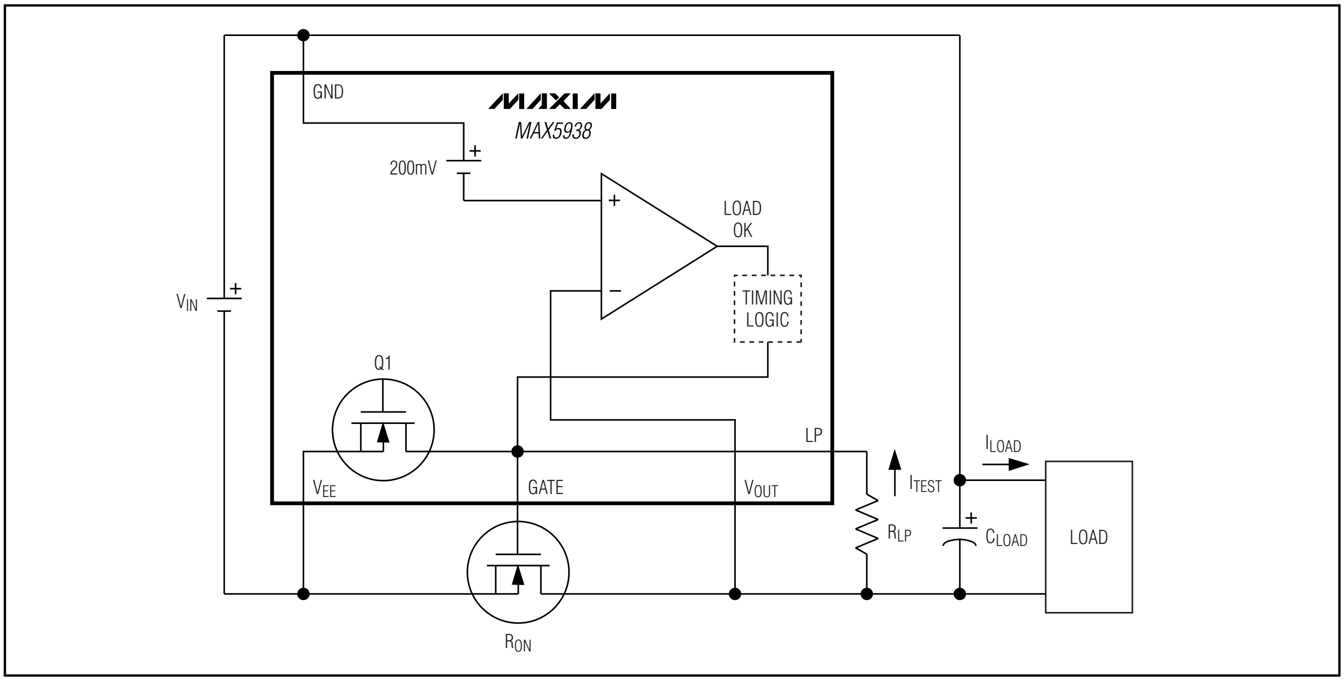


Figure 17. Load Probe Functional Diagram

Appendix B gives a more complete analysis and discussion of the step monitor function. It provides methods for the characterization of the load response to a V_{IN} ramp and graphical verification of the step monitor timing margins for a set of design parameters.

Selecting the PGOOD Pullup Resistor

Due to the open-drain driver, PGOOD requires an external pullup resistor to GND. This resistor should be selected to minimize the current load while PGOOD is low. The PGOOD output specification for V_{OL} is 0.4V at 1mA. As described in the *Detailed Description*, the external pullup interferes with the ability of PGOOD to follow positive V_{IN} steps as well as if it were driven by an active pullup. When PGOOD is asserted high, an apparent negative glitch appears at PGOOD during a positive V_{IN} step. To minimize this negative transient it may be necessary to increase the pullup current and/or to add a small amount of capacitance from PGOOD to GND to compensate for the pin capacitance.

Setting the Test Current Level for Load-Probe Test

The load-probe test is a current test of the load that avoids turning on the power MOSFET. The MAX5938 has an internal switch (Q1 in Figure 17) that pulls current through the load and through an external current-limiting resistor, R_{LP}. During the test, this switch is pulsed on for up to 220ms (typ). Current is pulled through the load, which should charge up the load capacitance unless there is a short. If the voltage across the load exceeds 200mV, the test is truncated and normal power-up is allowed to proceed. If the voltage across the load does not reach 200mV in the 220ms period that the current is on, the load is assumed to be shorted and the current to the load from LP is shut off. The MAX5938A will timeout for 16 x t_{LP} then retry the load-probe test. The MAX5938L will latch the fault condition indefinitely until ON and OFF are cycled low for 1.5ms or the power is recycled.

In the application, the current-limiting resistor should be selected to minimize the current pulled through the load while guaranteeing that it will charge the maximum expected load capacitance to 220mV in 90ms. These parameters are the maximum load-probe test voltage and the minimum load-probe current pulse period, respectively. The maximum current possible is 1A, which is adequate to test a load capacitance as large as 190,000µF over the typical telecom operating voltage range.

$$I_{TEST}\ (A) = C_{LOAD,MAX}\ (F) \times 220mV / 90ms$$

Since the minimum intended V_{IN} for the application will result in the lowest I_{TEST} during the load-probe test, this $V_{IN,MIN}$ should be used to set the R_{LP}. This voltage will likely be near $V_{ON,FALLING}$ or V_{OFF} for the application.

$$R_{TEST}(\Omega) = V_{IN,MIN} / I_{TEST} = V_{IN,MIN} \times 90ms / (C_{LOAD(MAX)} \times 220mV)$$

Example: V_{IN} operating range = 36V to 72V, C_{LOAD} = 10,000µF. First, find the R_{LP} that will guarantee a successful test of the load.

$$R_{LP} = 36V \times 90ms / (10{,}000µF \times 220mV) = 1.472\Omega \Rightarrow 1.47k\Omega \pm 1\%$$

Next, evaluate the R_{LP} at the maximum operating voltage to verify that it will not exceed the 1A current limit for the load-probe test.

$$I_{TEST,MAX} = V_{IN,MAX} / R_{LP} = 72V / 1.47k\Omega = 49.0mA$$

If the $C_{LOAD(MAX)}$ is increased to 190,000µF, the test current will approach the limit. In this case, R_{LP} will be a much lower value and must include the internal switch resistance. To find the external series resistor value that will guarantee a successful test at the lowest supply voltage, the maximum value for the load-probe switch on-resistance of 11Ω should be used:

$$R_{LP,TOT} = 36V \times 90ms / (190{,}000µF \times 220mV) = 90\Omega = 11\Omega + R_{LP}$$

$$R_{LP} = 77.51\Omega - 11\Omega = 66.51\Omega \Rightarrow 66.5\Omega \pm 1\%$$

Again R_{LP} must be evaluated at the maximum operating voltage to verify that it will not exceed the 1A current limit for the load-probe test. In this case, the minimum value for the load-probe switch on-resistance of 6Ω should be used:

$$I_{TEST,MAX} = V_{IN,MAX} / R_{LP,TOT} = 72V / (66.5\Omega + 6\Omega) = 993mA$$

Adjusting the V_{OUT} Slew Rate

The default slew rate is set internally for 9V/ms. The slew rate can be reduced by placing an external capacitor from the drain of the power MOSFET to the GATE output of the MAX5938. Figure 18 shows a graph of Slew Rate vs. C_{SLEW}. This graph shows that for C_{SLEW} < 4700pF there is very little effect to the addition of external slew-rate control capacitance. This is intended so the GATE output can drive large MOSFETs with significant gate capacitance and still achieve the default slew rate. To select a slew-rate control capacitor, go into the graph with the desired slew rate and find the value of the Miller Capacitance. When C_{SLEW} > 4700pF, SR and C_{SLEW} are inversely related. Given the desired slew rate, the required C_{SLEW} is found as follows:

$$C_{SLEW}(nF) = 23 / SR (V/ms)$$

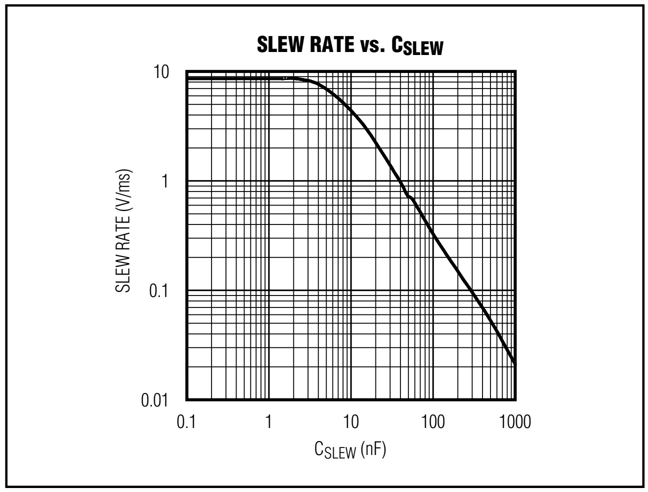


Figure 18. MAX5938 Slew Rate vs. C_{SLEW}

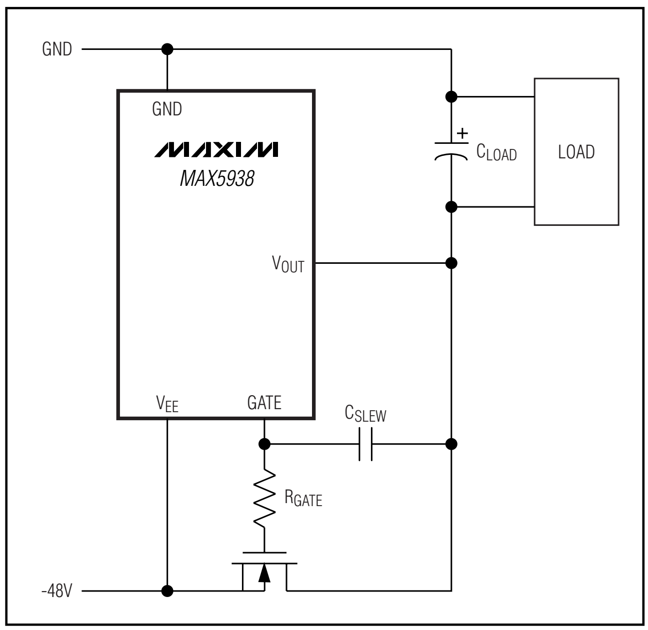


Figure 19. Adjusting the MAX5938 Slew Rate

From the data sheet of the power MOSFET find the reverse transfer capacitance (gate-to-drain capacitance) above 10V. If the reverse transfer capacitance of the external power MOSFET is 5% or more of C_{SLEW}, then it should be subtracted from C_{SLEW} in the equation above.

Figure 19 gives an example of the external circuit for controlling slew rate. Depending on the parasitics associated with the selected power MOSFET, the addition of C_{SLEW} may lead to oscillation while the MOSFET and GATE control are in the linear range. If this is an issue, an external resistor, R_{GATE}, in series with gate of the MOSFET is recommended to prevent possible oscillation. It should be as small as possible, e.g., 5Ω to 10Ω, to avoid impacting the MOSFET turn-off performance of the MAX5938.

Layout Guidelines

To benefit from the temperature compensation designed into the MAX5938, the part should be placed as close as possible to the power MOSFET that it is controlling. The V_{EE} pin of the MAX5938 should be placed close to the source pin of the power MOSFET and they should share a wide trace. A common top layer plane would service both the thermal and electrical requirements. The load-probe current must be taken into account. If this current is high, the layout traces and current-limiting resistor must be sized appropriately. Stray inductance must be minimized in the traces of the overall layout of the hot-swap controller, the power MOSFET and the load capacitor. Starting from the board contacts, all high-current traces should be short, wide, and direct. The potentially high pulse current pins of the MAX5938 are GATE (when pulling GATE low), load probe, and V_{EE}. Because of the nature of the hot-swap requirement no decoupling capacitor is recommended for the MAX5938. Because there is no decoupling capacitor, stray inductance may result in excessive ringing at the GND pin during power-up or during very rapid V_{IN} steps. This should be examined in every application design since ringing at the GND pin may exceed the absolute maximum supply rating for the part.

Input Transient Protection

During hot plug-in/unplug and fast V_{IN} steps, stray inductance in the power path may cause voltage ringing above the normal input DC value, which may exceed the absolute maximum supply rating. An input transient such as that caused by lightning can also put a severe transient peak voltage on the input rail. The following techniques are recommended to reduce the effect of transients:

1) Minimize stray inductance in the power path using wide traces and minimize loop area including the power traces and the return ground path.
2) Add a high-frequency (ceramic) bypass capacitor on the backplane as close as possible to the plug-in connector (Figure 20).
3) Add a 1kΩ resistor in series with the MAX5938's GND pin and a 0.1µF capacitor from GND to V_{EE} to limit transient current going into this pin.

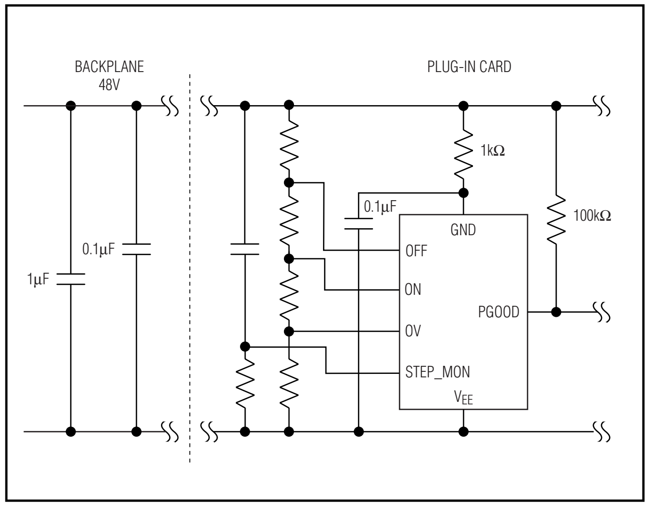


Figure 20. Protecting the MAX5938 Input from High-Voltage Transients

Appendix A

GATE Cycles

The power-up GATE cycle, step GATE cycle, and the OV GATE cycle are quite similar but have distinct differences. Understanding these differences may clarify application issues.

GATE Cycle During Power-Up

The power-up GATE cycle occurs during the initial power-up of the MAX5938 and the associated power MOSFET and load. The power-up GATE cycle can result in full enhancement or in a fault (all voltages are relative to V_{EE}).

Power-Up-to-Full-Enhancement Fault:

1) At the beginning of the power-up sequence to the start of the power-up GATE cycle, the GATE is held at V_{EE}. Following a successful completion of the load-probe test, GATE is held at V_{EE} for an additional 350µs and then is allowed to float for 650µs. At this point, the GATE begins to ramp with 52µA charging the gate of the power MOSFET. [GATE turn-on]
2) When GATE reaches the gate threshold voltage of the power MOSFET, V_{OUT} begins to ramp down toward V_{EE}. [V_{OUT} ramp]
3) When V_{OUT} ramps below 74% V_{CB}, the GATE is rapidly pulled to full enhancement and the power-up GATE cycle is complete. 1.26ms after GATE is pulled to full enhancement, PGOOD asserts. [Full enhancement]

Power-Up-to-Fault-Management Fault:

1) Same as step 1 above. [GATE turn-on]
2) Same as step 2 above. [V_{OUT} ramp]
3) GATE ramps to 90% of full enhancement while V_{OUT} remains above 74% V_{CB}, at which point the GATE is rapidly pulled to V_{EE} and fault management is initiated. [Fault management]

GATE Cycle During V_{IN} Step

A step GATE cycle occurs only after a successful power-up GATE cycle to full enhancement occurs and as a result of a positive V_{IN} step (all voltages are relative to V_{EE}).

Step-to-Full-Enhancement Fault:

1) A V_{IN} step occurs resulting in STEP_MON rising above $STEP_{TH}$ before V_{OUT} rises above V_{SC}. [Step detection]
2) After a step is detected, V_{OUT} rises above V_{SC} in response to the step. When V_{OUT} rises above V_{SC}, GATE is immediately pulled to V_{EE}, rapidly turning off the power MOSFET. GATE is held at V_{EE} for 350µs to damp any ringing. Once GATE is pulled to V_{EE}, the gate cycle has begun and STEP_MON can safely drop below $STEP_{TH}$ and successfully complete a step GATE cycle to full enhancement without initiating fault management. [GATE pulldown]
3) Following the 350µs of GATE pulldown, GATE is allowed to float for 650µs. At this point, the GATE begins to ramp with 52µA charging the gate of the power MOSFET. [GATE turn-on]
4) When GATE reaches the gate threshold voltage of the power MOSFET, V_{OUT} begins to ramp down toward the new lower V_{EE}. In the interval where GATE is below the MOSFET threshold, the MOSFET is off and V_{OUT} will droop depending on the RC time constant of the load. [V_{OUT} ramp]
5) When V_{OUT} ramps below 74% V_{CB}, the GATE pulls rapidly to full enhancement and the step GATE cycle is complete. If STEP_MON remains above $STEP_{TH}$ when GATE has ramped to 90% of full enhancement and V_{OUT} remains above 74% of V_{CB}, GATE remains at 90% and is not pulled to full enhancement. In this condition, if V_{OUT} drops below 74% of V_{CB} before STEP_MON drops below $STEP_{TH}$, GATE is rapidly pulled to full enhancement and the step GATE cycle is complete. PGOOD remains asserted throughout the step GATE cycle. [Full enhancement]

Step-to-Fault-Management Fault:

1) Same as step 1 above. [Step detection]
2) Same as step 2 above. [GATE pulldown]
3) Same as step 3 above. [GATE turn-on]
4) Same as step 4 above. [V_{OUT} ramp]
5) If STEP_MON is below $STEP_{TH}$ when GATE ramps to 90% of full enhancement and V_{OUT} remains above 74% V_{CB}, GATE is rapidly pulled to V_{EE}. Fault management is initiated and PGOOD is deasserted. If STEP_MON is above $STEP_{TH}$ when GATE ramps to 90% of full enhancement and V_{OUT} remains above 74% of V_{CB}, GATE remains at 90%. It is not pulled to full enhancement nor is it pulled to V_{EE}. In this condition, if V_{OUT} drops below 74% of V_{CB} before STEP_MON drops below $STEP_{TH}$, GATE is rapidly pulled to full enhancement and a fault is avoided. Conversely, if STEP_MON drops below $STEP_{TH}$ first, the GATE is rapidly pulled to V_{EE}, fault management is initiated, and PGOOD is deasserted. [Fault management]

It should be emphasized that while STEP_MON remains above $STEP_{TH}$ the current fault management is blocked. During this time it is possible for there to be multiple events involving V_{OUT} rising above V_{SC} then falling below 74% V_{CB}. In each of these events, when V_{OUT} rises above V_{SC}, a full GATE cycle is initiated where GATE is first pulled low then allowed to ramp up. Then finally, when V_{OUT} conditions are met, it will be fully enhanced.

GATE Cycle During Momentary Overvoltage

An OV GATE cycle occurs only after a successful power-up GATE cycle to full enhancement and as a result of a momentary excursion of OV above the OV threshold voltage. An OV GATE cycle does not result in an OV fault unless OV remains above the threshold for more than 1.5ms (all voltages are relative to V_{EE}).

OV GATE Cycle to Full enhancement:

1) When OV rises above the OV threshold voltage, GATE is immediately pulled to V_{EE}, rapidly turning off the power MOSFET. GATE is held at V_{EE} indefinitely while OV is above the OV threshold voltage. It is held for an additional 350µs to damp any ringing. [GATE pulldown]
2) Following the GATE pulldown, GATE is allowed to float for 650µs. At this point, the GATE begins to ramp with 52µA charging the gate of the power MOSFET. [GATE turn-on]

3) When GATE reaches the gate threshold voltage of the power MOSFET, V_{OUT} begins to ramp back down toward V_{EE}. In the interval where GATE is below the MOSFET threshold, the MOSFET is off and V_{OUT} will droop depending on the RC time constant of the load. [V_{OUT} ramp]
4) When V_{OUT} ramps below 74% V_{CB}, the GATE is rapidly pulled to full enhancement and the OV GATE cycle is complete. [Full enhancement]

OV GATE Cycle to Fault management:

1) Same as step 1 above. [GATE pulldown]
2) Same as step 2 above. [GATE turn-on]
3) Same as step 3 above. [V_{OUT} ramp]
4) If GATE ramps to 90% of full enhancement and V_{OUT} remains above 74% V_{CB}, GATE is rapidly pulled to V_{EE}, fault management is initiated, and PGOOD is deasserted. [Fault management]

GATE Output

GATE is a complex output structure and its condition at any moment is dependent on various timing sequences in response to multiple inputs. A diode to V_{EE} prevents negative excursions. For positive excursions, the states are:

1) Power-off with 2V clamp.
2) 8Ω pulldown to V_{EE}.
   a. Continuous during startup delay and during fault conditions.
   b. Pulsed following detected step or OV condition.
3) Floating with 16V clamp [prior to GATE ramp].
4) 52µA current source with 16V clamp [GATE ramp].
5) Pullup to internal 10V supply with 16V clamp [full enhancement].

Appendix B

Step Monitor Component Selection Analysis

As mentioned previously in the *Setting the Circuit-Breaker and Short-Circuit Thresholds* section, the AC response from V_{IN} to V_{OUT} is dependent on the parasitics of the load. This is especially true for the load capacitor in conjunction with the power MOSFET's $R_{DS(ON)}$. The load capacitor (with parasitic ESR and LSR) and the power MOSFET's $R_{DS(ON)}$ can be modeled as a heavily damped second-order system. As such, this system functions as a bandpass filter from V_{IN} to V_{OUT} limiting the ability of V_{OUT} to follow the V_{IN} ramp. STEP_MON lags the V_{IN} ramp with a first-order RC response, while V_{OUT} lags with an overdamped second-order response.

Given a positive V_{IN} ramp with a ramp rate of dV/dt, the approximate response of V_{OUT} to V_{IN} is:

$$V_{OUT}(t) = (dV/dt) \times \tau_C \times (1-e^{(-t / \tau_{L,eqv})}) + R_{DS(ON)} \times I_{LOAD} \quad \text{(Equation 1)}$$

where $\tau_C = C_{LOAD} \times R_{DS(ON)}$.

Equation 1 is a simplification for the overdampened second-order response of the load to a ramp input, $\tau_C = C_{LOAD} \times R_{DS(ON)}$ and corresponds to the ability of the load capacitor to transfer dV/dt current to the fully enhanced power MOSFET's $R_{DS(ON)}$. The equivalent time constant of the load ($\tau_{L,eqv}$) accounts for the parasitic series inductance and resistance of the capacitor and board interconnect. To characterize the load dynamic response to V_{IN} ramps, determine $\tau_{L,eqv}$ empirically with a few tests.

Similarly, the response of STEP_MON to a V_{IN} ramp is:

$$V_{STEP\_MON}(t) = (dV/dt) \times \tau_{STEP} \times (1-e^{(-t / \tau_{STEP})}) + 10\mu A \times R_{STEP\_MON} \quad \text{(Equation 2)}$$

where $\tau_{STEP} = R_{STEP\_MON} \times C_{STEP\_MON}$.

For proper step detection, V_{STEP_MON} must exceed $STEP_{TH}$ prior to V_{OUT} reaching V_{SC} or within 1.4ms of V_{OUT} reaching V_{CB} (or overall V_{IN} ramp rates anticipated in the application). It is impossible to give a fixed set of design guidelines that rigidly apply over the wide array of applications using the MAX5938. There are, however, limiting conditions and recommendations that should be observed.

One limiting condition that must be observed is to ensure that the STEP_MON time constant, τ_{STEP}, is not so low that at the lowest ramp rate, the anticipated $STEP_{TH}$ cannot be obtained. The product (dV/dt) x $\tau_{STEP} = \tau_{STEP\_MON,MAX}$, is the maximum differential voltage at STEP_MON if the V_{IN} ramp were to continue indefinitely. A related condition is setting the STEP_MON voltage below $STEP_{TH}$ with adequate margin, ΔV_{STEP_MON}, to accommodate the tolerance of both I_{STEP_OS} (±8%) and R_{STEP_MON}. In determining τ_{STEP_MON}, use the 9.2µA limit to ensure sufficient margin with worst-case I_{STEP_OS}.

The margin of V_{OUT} (with respect to V_{SC} and V_{CB}) is set when R_{CB_ADJ} is selected as described in the *Setting the Circuit-Breaker and Short-Circuit Thresholds* section. This margin may be lower at one of the temperature extremes and if so, that value should be used in the following discussion. These margins will be called

ΔV_{CB} and ΔV_{SC} and they represent the minimum V_{OUT} excursion required to trip the respective fault. R_{STEP_MON} will typically be set to 100kΩ ±1%. This gives a ΔV_{STEP_MON} of 0.25V, a worst-case low of 0.13V, and a worst-case high of 0.37V. In finding τ_{STEP} in the equation below, use ΔV_{STEP_MON} = 0.37V to ensure sufficient margin with worst-case I_{STEP_OS}.

To set τ_{STEP} to block all V_{CB} and V_{SC} faults for any ramp rate, find the ratio of ΔV_{STEP_MON} to ΔV_{CB} and choose τ_{STEP} so:

$$\tau_{STEP} = 1.2 \times \tau_C \times \Delta V_{STEP\_MON} / \Delta V_{CB}$$

and since R_{STEP_MON} = 100kΩ:

$$C_{STEP\_MON} = \tau_{STEP} / R_{STEP\_MON} = \tau_{STEP} / 100k\Omega$$

After the first-pass component selection, if sufficient timing margin exists, it is possible (but not necessary) to lower R_{STEP} below 100kΩ to reduce the sensitivity of STEP_MON to V_{IN} noise.

Verification of the Step Monitor Timing

It is prudent to verify conclusively that all circuit-breaker and short-circuit faults will be blocked for all ramp rates. To do this, some form of graphical analysis is recommended but first, find the value of $\tau_{L,eqv}$ of the load by a series of ramp tests as indicated earlier. These tests include evaluating the load with a series of V_{IN} ramps of increasing ramp rates and monitoring the rate of rise of V_{OUT} during the ramp. Each V_{IN} ramp should have a constant slope. The V_{OUT} response data must be taken only during the positive ramp. Data taken after V_{IN} has leveled off at the new higher value must not be used.

Figure 21 shows the load in parallel with the load capacitor, C_{LOAD}, and the parallel connection in series with the power MOSFET, which is fully enhanced with V_{GS} = 10V. The objective is to determine $\tau_{L,eqv}$ from the V_{OUT} response.

Figure 22 shows the general response of V_{OUT} to a V_{IN} ramp over time t. Equation 1 gives the response of V_{OUT} to a ramp of dV/dt. The product (dV/dt) x τ_C = ΔV_{OUT}(max) or the maximum V_{OUT} voltage differential if the V_{IN} ramp were to continue indefinitely. The parameter of interest is ΔV_{OUT} due to the ramp dV/dt, thus it is necessary to subtract the DC shift in V_{OUT} due to the load resistance. For some loads, which are relatively independent of supply voltage, this may be insignificant.

$$V_{OUT}(t) = V_{OUT}(t) - R_{DS(ON)} \times I_{LOAD}$$

where I_{LOAD} is a function of the V_{OUT} level that should be determined separately with DC tests.

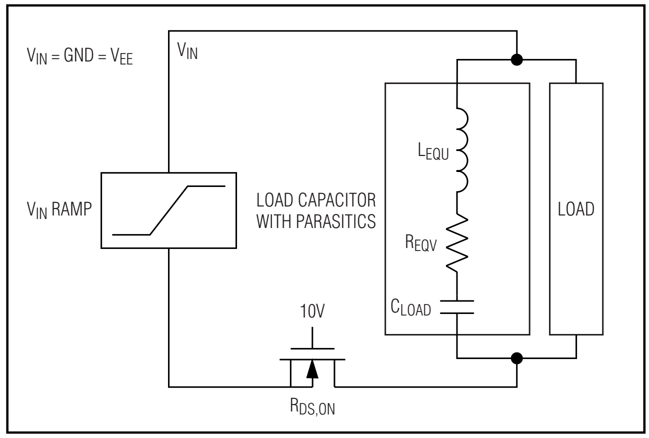


Figure 21. V_{IN} Ramp Test Of Load

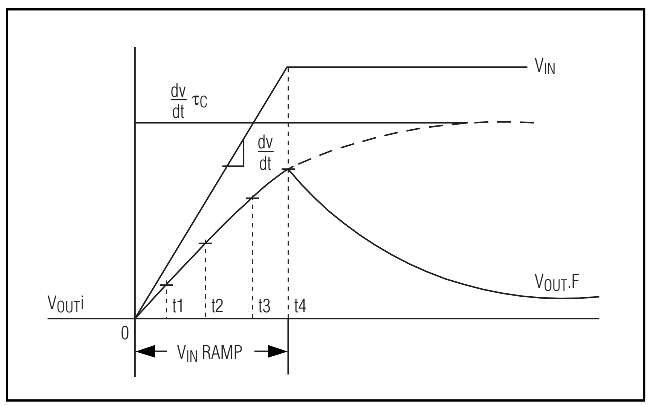


Figure 22. General Response of V_{OUT} to a V_{IN} Ramp

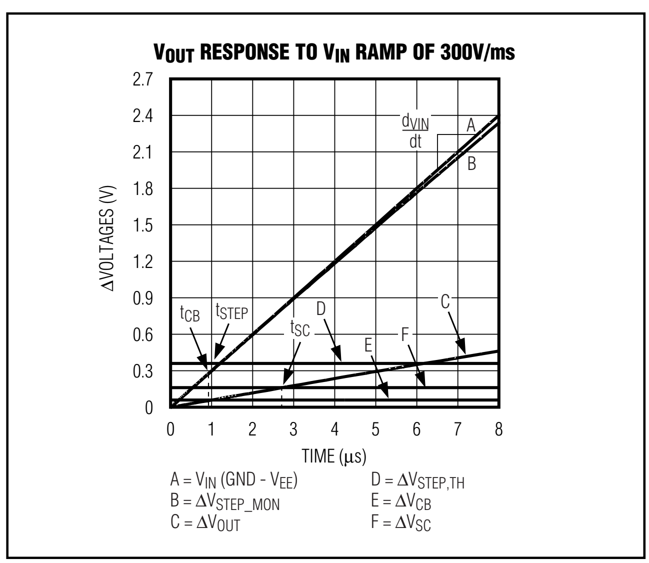


Figure 23. V_{OUT} Response to V_{IN} Ramp of 300V/ms

At any time (t) the ΔV_{OUT} fraction of $\Delta V_{OUT}(max)$ is:

$$\Delta V_{OUT}(t) / [(dV/dt) \times \tau_C] = (1 - e^{(-t / \tau_{L,eqv})})$$

If $V_{OUT}(t)$ is measured at time t, then the equivalent time constant of the load is found from:

$$\tau_{L,eqv} = -t / \ln(1 - \Delta V_{OUT} / [(dV/dt) \times \tau_C])$$

As mentioned earlier, several measurements of ΔV_{OUT} at times t1, t2, t3, and t4 should be made during the ramp. Each of these may result in slightly different values of $\tau_{L,eqv}$ and all values should then be averaged. In making the measurements, the V_{IN} ramp duration should be such that ΔV_{OUT} reaches 2 or 3 times the selected ΔV_{SC}. The ramp tests should include three ramp rates: $\Delta V_{SC} / \tau_C$, $2 \times \Delta V_{SC} / \tau_C$, and $4 \times \Delta V_{SC} / \tau_C$. The values of $\tau_{L,eqv}$ may vary over the range of slew rates due to measurement error, nonlinear dynamics in the load, and due to the fact that Equation 1 is a simplification from a higher order dynamic system. The resulting range of $\tau_{L,eqv}$ values should be used to validate the performance of the final design.

Having τ_C, $\tau_{L,eqv}$, R_{STEP}, and C_{STEP} in a graphical analysis using Equation 1 and Equation 2 can verify the step monitor function by displaying the relative timing of t_{CB}, t_{STEP}, and t_{SC}, which are the times when V_{CB}, V_{STEP_MON}, and V_{SC} voltage thresholds are exceeded. A simple Excel spreadsheet for this purpose can be supplied by Maxim upon request. Figures 23, 24, and 25 graphically verify a particular solution over 3 decades of V_{IN} ramp rates. In addition, Figure 25 verifies that this solution will block all circuit-breaker and short-circuit faults for even the lowest V_{IN} ramp that will cause V_{OUT} to exceed V_{CB}.

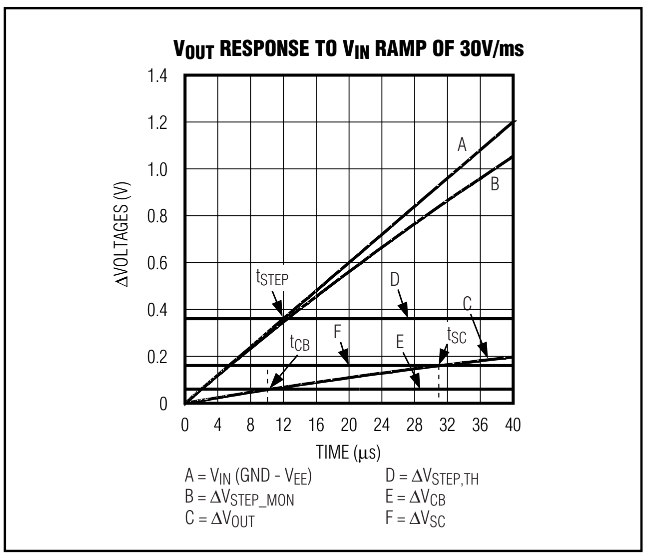


Figure 24. V_{OUT} Response to V_{IN} Ramp of 30V/ms

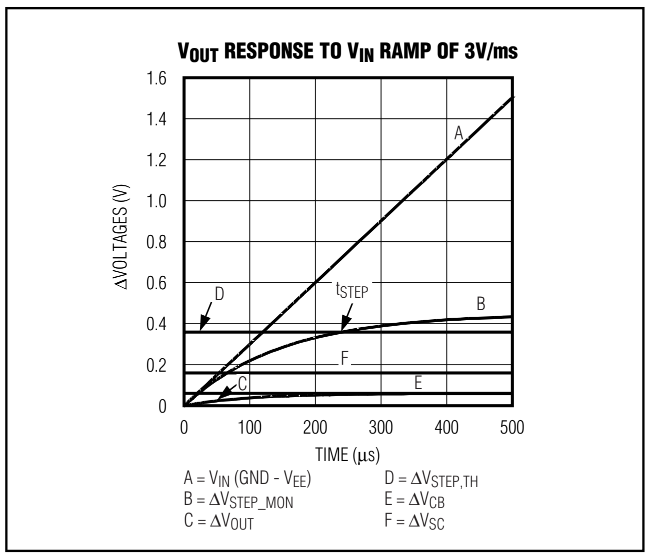
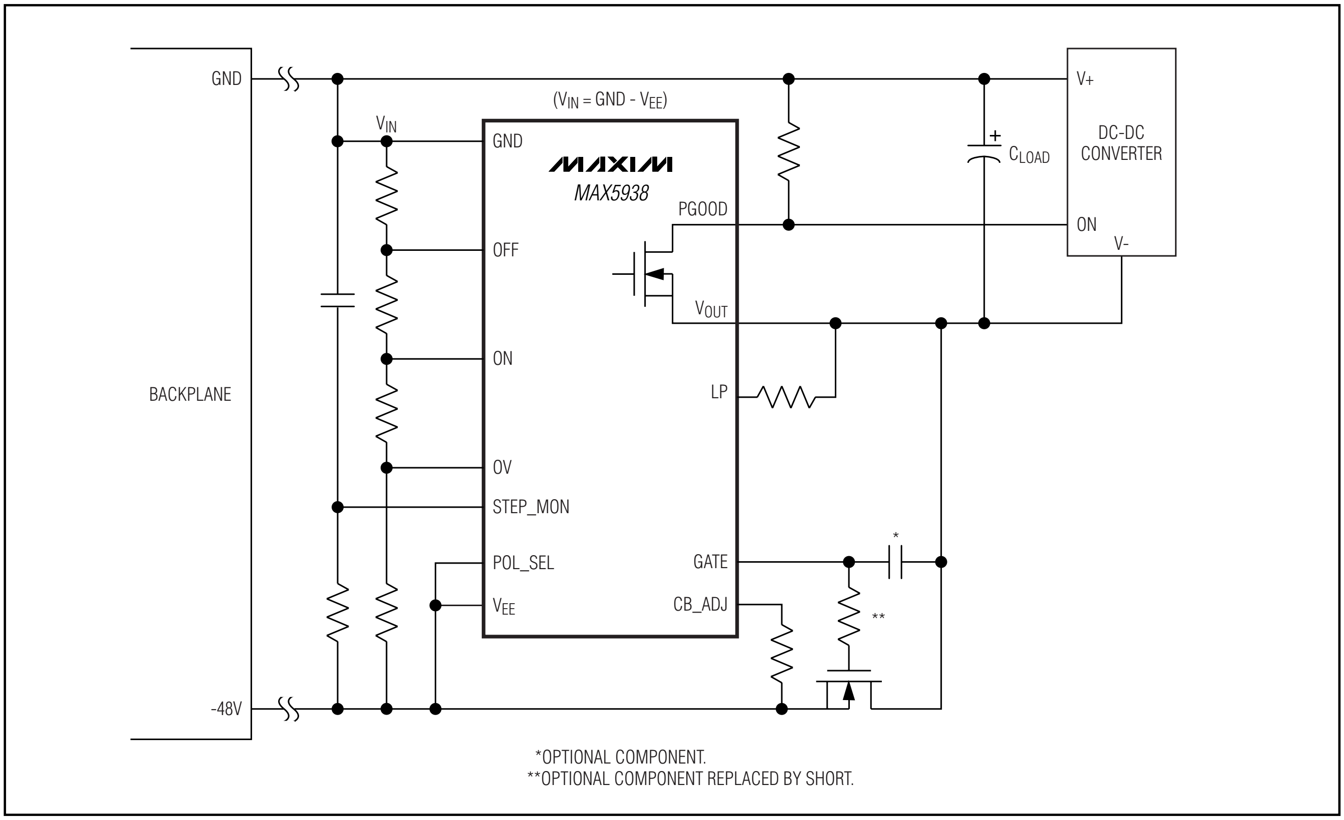


Figure 25. V_{OUT} Response to V_{IN} Ramp of 3V/ms

Typical Operating Circuit



Timing Table

NAME	SYMBOL	TYPICAL TIME (s)
Power-Up Delay	t_{ONDLY}	220m
Load-Probe Test Timeout	t_{LP}	220m
Load-Probe Retry Time	t_{LP_OFF}	3.5
PGOOD Assertion Delay Time	t_{PGOOD}	1.26m
Autoretry Delay	t_{RETRY}	3.5
Circuit-Breaker Glitch Rejection	t_{CB_DLY}	1.4m
ON Glitch Rejection	t_{REJ}	1.5m
OV Transient Rejection	t_{OVREJ}	1.5m
GATE Pulldown Pulse Following a V_{IN} Step	—	350µ
GATE Low after a V_{IN} Step, Prior to Ramp	—	1m

Chip Information

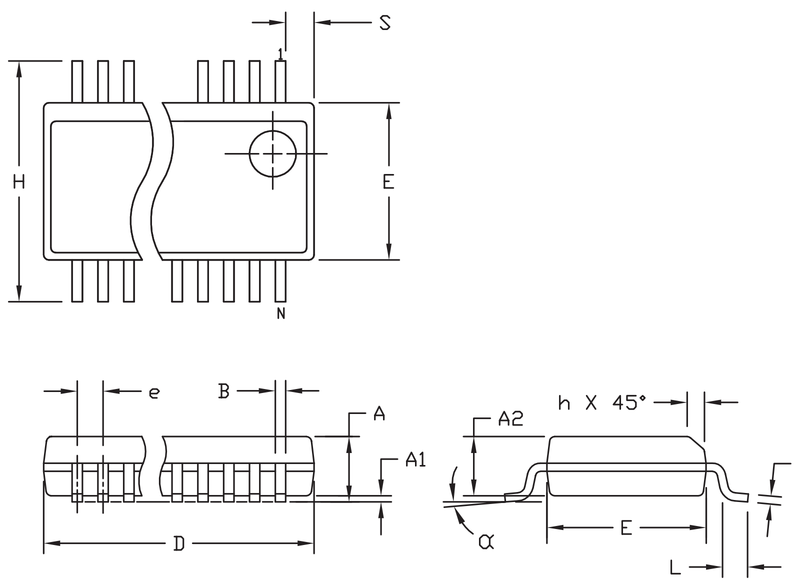
TRANSISTOR COUNT: 2320

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°

VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1