19-3063; Rev 0; 1/04

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

MAX5530/MAX5531

General Description

The MAX5530/MAX5531 are single, 12-bit, ultra-low-power, voltage-output, digital-to-analog converters (DACs) offering Rail-to-Rail® buffered voltage outputs. The DACs operate from a 1.8V to 5.5V supply and consume less than 6µA, making them desirable for low-power and low-voltage applications. A shutdown mode reduces overall current, including the reference input current, to just 0.18µA. The MAX5530/MAX5531 use a 3-wire serial interface that is compatible with SPI™, QSPI™, and MICROWIRE™.

At power-up, the MAX5530/MAX5531 outputs are driven to zero scale, providing additional safety for applications that drive valves or for other transducers that must be off during power-up. The zero-scale outputs enable glitch-free power-up.

The MAX5530 accepts an external reference input. The MAX5531 contains an internal reference and provides an external reference output. Both devices have force-sense-configured output buffers.

The MAX5530/MAX5531 are available in a 4mm x 4mm x 0.8mm, 12-pin, thin QFN package and are guaranteed over the extended -40°C to +85°C temperature range.

For 10-bit compatible devices, refer to the MAX5520/MAX5521 data sheet. For 8-bit compatible devices, refer to the MAX5510/MAX5511 data sheet.

Applications

Portable Battery-Powered Devices

Instrumentation

Automatic Trimming and Calibration in Factory or Field

Programmable Voltage and Current Sources

Industrial Process Control and Remote Industrial Devices

Remote Data Conversion and Monitoring

Chemical Sensor Cell Bias for Gas Monitors

Programmable Liquid Crystal Display (LCD) Bias

Selector Guide

PART	REFERENCE	TOP MARK
MAX5530ETC	External	AACS
MAX5531ETC	Internal	AACT

Rail-to-Rail is a registered trademark of Nippon Motorola, Inc.
SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp

Features

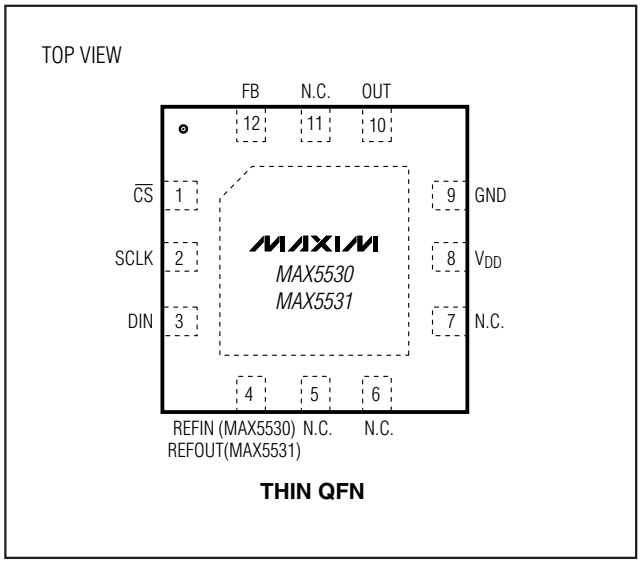
- **Ultra-Low 6µA Supply Current**
- **Shutdown Mode Reduces Supply Current to 0.18µA (max)**
- **Single +1.8V to +5.5V Supply**
- **Small 4mm x 4mm x 0.8mm Thin QFN Package**
- **Flexible Force-Sense-Configured Rail-to-Rail Output Buffers**
- **Internal Reference Sources 8mA of Current (MAX5531)**
- **Fast 16MHz 3-Wire SPI-/QSPI-/MICROWIRE-Compatible Serial Interface**
- **TTL- and CMOS-Compatible Digital Inputs with Hysteresis**
- **Glitch-Free Outputs During Power-Up**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5530ETC	-40°C to +85°C	12 Thin QFN-EP*
MAX5531ETC	-40°C to +85°C	12 Thin QFN-EP*

**EP = Exposed paddle (internally connected to GND).*

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
OUT to GND .....-0.3V to (V_{DD} + 0.3V)
FB to GND .....-0.3V to (V_{DD} + 0.3V)
SCLK, DIN, $\overline{CS}$ to GND .....-0.3V to (V_{DD} + 0.3V)
REFIN, REFOUT to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Thin QFN (derate 16.9mW/°C above +70°C 1349mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +1.8V to +5.5V, OUT unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY (MAX5530 EXTERNAL REFERENCE)						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	V_{DD} = 5V, V_{REF} = 4.096V		±4	±8	LSB
		V_{DD} = 1.8V, V_{REF} = 1.024V		±4	±8	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic, V_{DD} = 5V, V_{REF} = 4.096V		±0.2	±1	LSB
		Guaranteed monotonic, V_{DD} = 1.8V, V_{REF} = 1.024V		±0.2	±1	
Offset Error (Note 2)	V_{OS}	V_{DD} = 5V, V_{REF} = 4.096V		±1	±20	mV
		V_{DD} = 1.8V, V_{REF} = 1.024V		±1	±20	
Offset-Error Temperature Drift				±2		µV/°C
Gain Error (Note 3)	GE	V_{DD} = 5V, V_{REF} = 4.096V		±2	±4	LSB
		V_{DD} = 1.8V, V_{REF} = 1.024V		±2	±4	
Gain-Error Temperature Coefficient				±4		ppm/°C
Power-Supply Rejection Ratio	PSRR	1.8V ≤ V_{DD} ≤ 5.5V		85		dB
STATIC ACCURACY (MAX5531 INTERNAL REFERENCE)						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	V_{DD} = 5V, V_{REF} = 3.9V		±4	±8	LSB
		V_{DD} = 1.8V, V_{REF} = 1.2V		±4	±8	
Differential Nonlinearity (Note 1)	DNL	Guaranteed monotonic, V_{DD} = 5V, V_{REF} = 3.9V		±0.2	±1	LSB
		Guaranteed monotonic, V_{DD} = 1.8V, V_{REF} = 1.2V		±0.2	±1	
Offset Error (Note 2)	V_{OS}	V_{DD} = 5V, V_{REF} = 3.9V		±1	±20	mV
		V_{DD} = 1.8V, V_{REF} = 1.2V		±1	±20	
Offset-Error Temperature Drift				±2		µV/°C
Gain Error (Note 3)	GE	V_{DD} = 5V, V_{REF} = 3.9V		±2	±4	LSB
		V_{DD} = 1.8V, V_{REF} = 1.2V		±2	±4	
Gain-Error Temperature Coefficient				±4		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V to +5.5V, OUT unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	1.8V ≤ V_{DD} ≤ 5.5V		85		dB
REFERENCE INPUT (MAX5530)						
Reference-Input Voltage Range	V_{REFIN}		0		V_{DD}	V
Reference-Input Impedance	R_{REFIN}	Normal operation	4.1			MΩ
		In shutdown		2.5		GΩ
REFERENCE OUTPUT (MAX5531)						
Initial Accuracy	V_{REFOUT}	No external load, V_{DD} = 1.8V	1.197	1.214	1.231	V
		No external load, V_{DD} = 2.5V	1.913	1.940	1.967	
		No external load, V_{DD} = 3V	2.391	2.425	2.459	
		No external load, V_{DD} = 5V	3.828	3.885	3.941	
Output-Voltage Temperature Coefficient	V_{TEMPCO}	T_A = -40°C to +85°C (Note 4)		12	30	ppm/°C
Line Regulation		V_{REFOUT} < V_{DD} - 200mV (Note 5)		2	200	µV/V
Load Regulation		0 ≤ I_{REFOUT} ≤ 1mA, sourcing, V_{DD} = 1.8V, V_{REF} = 1.2V		0.3	2	µV/µA
		0 ≤ I_{REFOUT} ≤ 8mA, sourcing, V_{DD} = 5V, V_{REF} = 3.9V		0.3	2	
		-150µA ≤ I_{REFOUT} ≤ 0, sinking		0.2		
Output Noise Voltage		0.1Hz to 10Hz, V_{REFOUT} = 3.9V		150		$µV_{P-P}$
		10Hz to 10kHz, V_{REFOUT} = 3.9V		600		
		0.1Hz to 10Hz, V_{REFOUT} = 1.2V		50		
		10Hz to 10kHz, V_{REFOUT} = 1.2V		450		
Short-Circuit Current (Note 6)		V_{DD} = 5V		30		mA
		V_{DD} = 1.8V		14		
Capacitive Load Stability Range		(Note 7)		0 to 10		nF
Thermal Hysteresis		(Note 8)		200		ppm
Reference Power-Up Time (from Shutdown)		REFOUT unloaded, V_{DD} = 5V		5.4		ms
		REFOUT unloaded, V_{DD} = 1.8V		4.4		
Long-Term Stability				200		ppm/ 1khrs
DAC OUTPUT (OUT)						
Capacitive Driving Capability	C_L			1000		pF
Short-Circuit Current (Note 6)		V_{DD} = 5V, V_{OUT} set to full scale, OUT shorted to GND, source current			65	mA
		V_{DD} = 5V, V_{OUT} set to 0V, OUT shorted to V_{DD}, sink current			65	
		V_{DD} = 1.8V, V_{OUT} set to full scale, OUT shorted to GND, source current			14	
		V_{DD} = 1.8V, V_{OUT} set to 0V, OUT shorted to V_{DD}, sink current			14	

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.8V to +5.5V, OUT unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Power-Up Time		Coming out of shutdown (MAX5530)	V_{DD} = 5V		3		ms
			V_{DD} = 1.8V		3.8		
		Coming out of standby (MAX5531)	V_{DD} = 1.8V to 5.5V		0.4		
Output Power-Up Glitch		C_L = 100pF			10		mV
FB_ Input Current					10		pA
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$)							
Input High Voltage	V_{IH}	4.5V ≤ V_{DD} ≤ 5.5V		2.4			V
		2.7V < V_{DD} ≤ 3.6V		2.0			
		1.8V ≤ V_{DD} ≤ 2.7V		0.7 x V_{DD}			
Input Low Voltage	V_{IL}	4.5V ≤ V_{DD} ≤ 5.5V				0.8	V
		2.7V < V_{DD} ≤ 3.6V				0.6	
		1.8V ≤ V_{DD} ≤ 2.7V				0.3 x V_{DD}	
Input Leakage Current	I_{IN}	(Note 9)			±0.05	±0.5	µA
Input Capacitance	C_{IN}				10		pF
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	Positive and negative (Note 10)			10		V/ms
Voltage-Output Settling Time		0.1 to 0.9 of full scale to within 0.5 LSB (Note 10)			660		µs
Output Noise Voltage		0.1Hz to 10Hz	V_{DD} = 5V		80		$µV_{P-P}$
			V_{DD} = 1.8V		55		
		10Hz to 10kHz	V_{DD} = 5V		620		
			V_{DD} = 1.8V		476		
POWER REQUIREMENTS							
Supply Voltage Range	V_{DD}			1.8		5.5	V
Supply Current (Note 9)	I_{DD}	MAX5530	V_{DD} = 5V		2.6	4	µA
			V_{DD} = 3V		2.6	4	
			V_{DD} = 1.8V		3.6	5	
		MAX5531	V_{DD} = 5V		5.3	7.0	
			V_{DD} = 3V		4.8	7.0	
			V_{DD} = 1.8V		5.4	7.0	
Standby Supply Current	I_{DDSD}	(Note 9)	V_{DD} = 5V		3.3	4.5	µA
			V_{DD} = 3V		2.8	4.0	
			V_{DD} = 1.8V		2.4	3.5	
Shutdown Supply Current	I_{DDPD}	(Note 9)			0.05	0.25	µA

TIMING CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (V_{DD} = 4.5V TO 5.5V)						
Serial Clock Frequency	f_{SCLK}		0		16.7	MHz
DIN to SCLK Rise Setup Time	t_{DS}		15			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		24			ns
SCLK Pulse-Width Low	t_{CL}		24			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		100			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		20			ns
SCLK Fall to $\overline{CS}$ Fall Setup	t_{CSO}		0			ns
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}		20			ns

TIMING CHARACTERISTICS

(V_{DD} = +1.8V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (V_{DD} = 1.8V TO 5.5V)						
Serial Clock Frequency	f_{SCLK}		0		10	MHz
DIN to SCLK Rise Setup Time	t_{DS}		24			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		150			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		30			ns
SCLK Fall to $\overline{CS}$ Fall Setup	t_{CSO}		0			ns
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}		30			ns

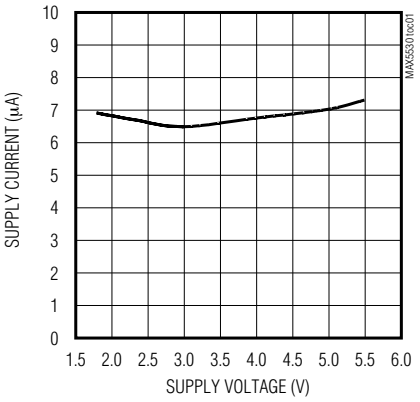
Note 1: Linearity is tested within codes 96 to 4080.
Note 2: Offset is tested at code 96.
Note 3: Gain is tested at code 4095. FB is connected to OUT.
Note 4: Guaranteed by design. Not production tested.
Note 5: V_{DD} must be a minimum of 1.8V.
Note 6: Outputs can be shorted to V_{DD} or GND indefinitely, provided that the package power dissipation is not exceeded.
Note 7: Optimal noise performance is at 2nF load capacitance.
Note 8: Thermal hysteresis is defined as the change in the initial +25°C output voltage after cycling the device from T_{MAX} to T_{MIN}.
Note 9: All digital inputs at V_{DD} or GND.
Note 10: Load = 10kΩ in parallel with 100pF, V_{DD} = 5V, V_{REF} = 4.096V (MAX5530) or V_{REF} = 3.9V (MAX5531).

Ultra-Low-Power, 12-Bit, Voltage-Output DACs

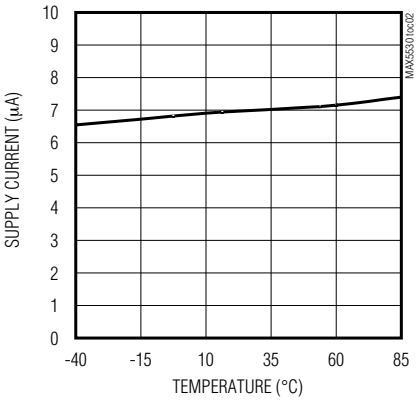
Typical Operating Characteristics

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

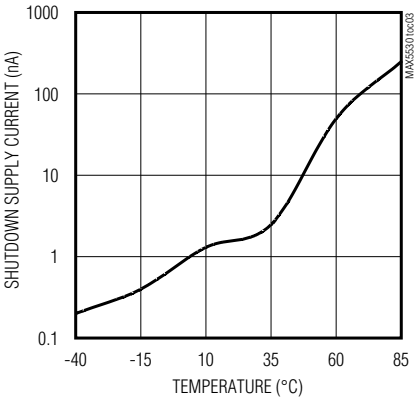
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5531)



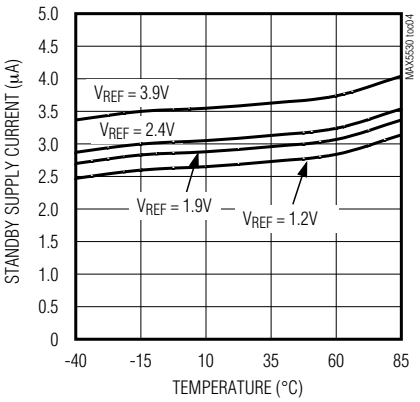
SUPPLY CURRENT vs. TEMPERATURE (MAX5531)



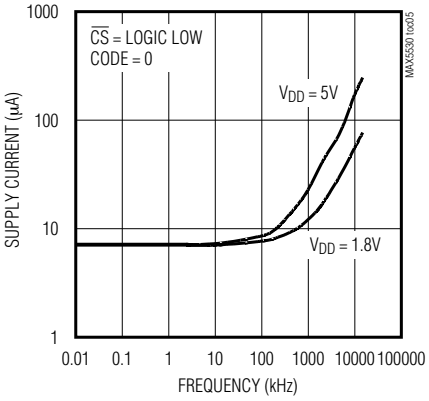
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5531)



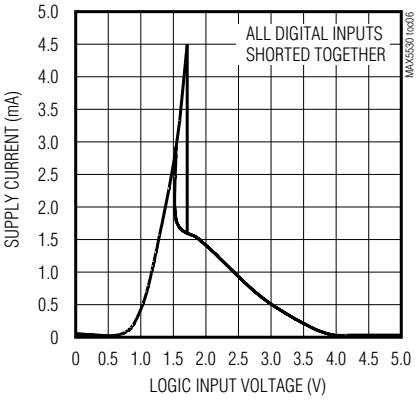
STANDBY SUPPLY CURRENT vs. TEMPERATURE (MAX5531)



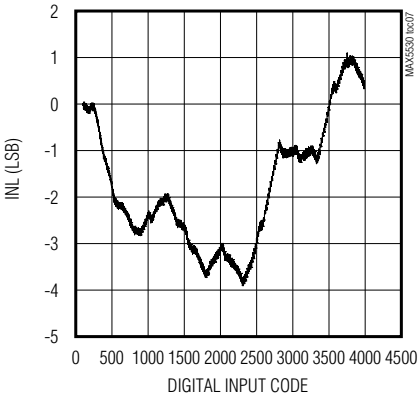
SUPPLY CURRENT vs. CLOCK FREQUENCY



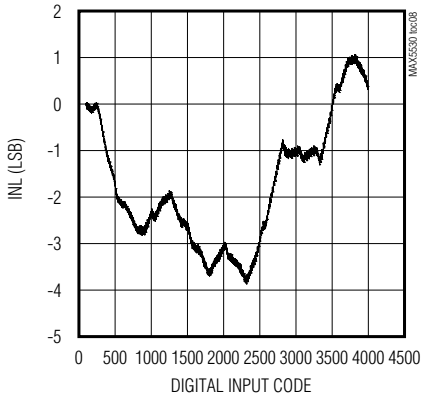
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



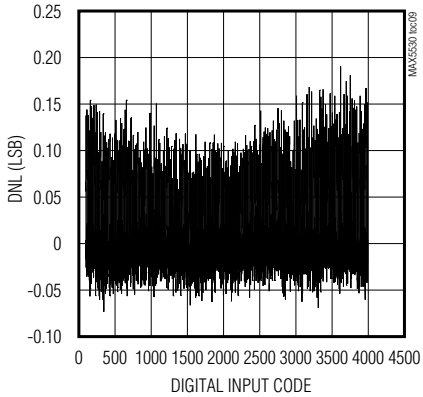
INL vs. INPUT CODE (V_{DD} = V_{REF} = 1.8V)



INL vs. INPUT CODE (V_{DD} = V_{REF} = 5V)



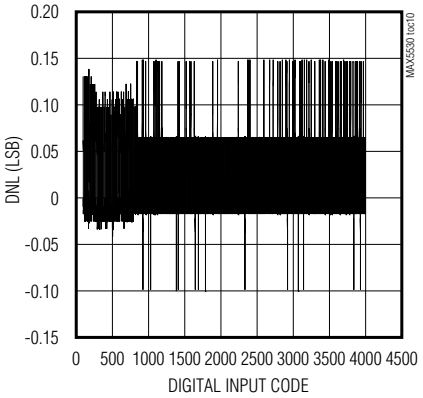
DNL vs. INPUT CODE (V_{DD} = V_{REF} = 1.8V)



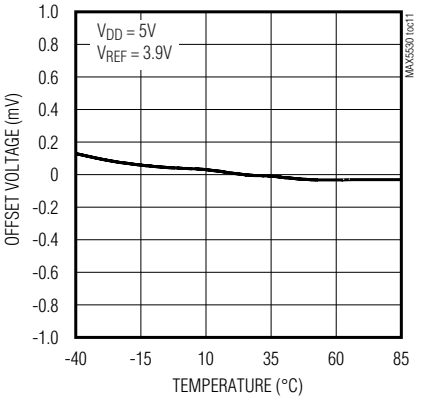
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

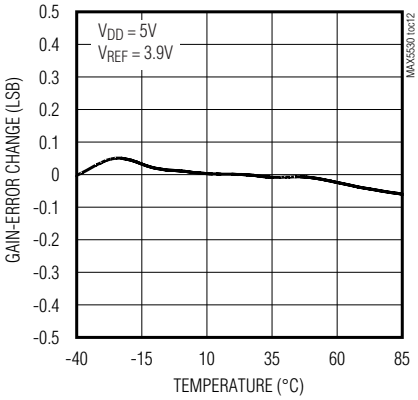
DNL vs. INPUT CODE (V_{DD} = V_{REF} = 5V)



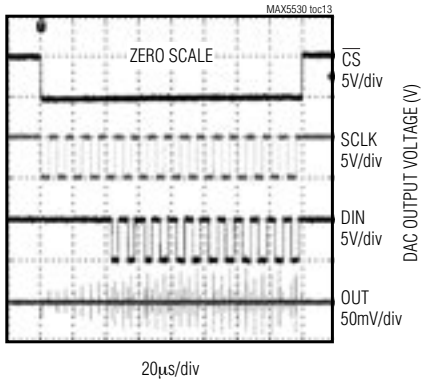
OFFSET VOLTAGE vs. TEMPERATURE



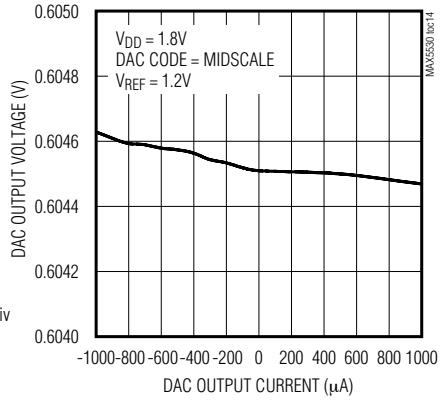
GAIN-ERROR CHANGE vs. TEMPERATURE



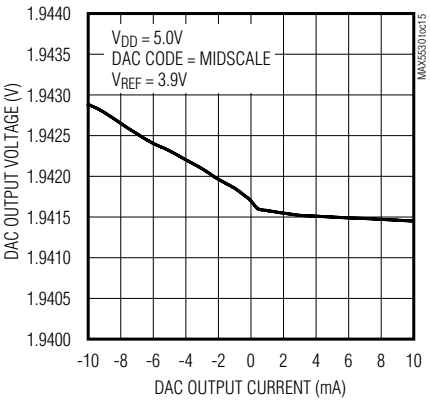
DIGITAL FEEDTHROUGH RESPONSE



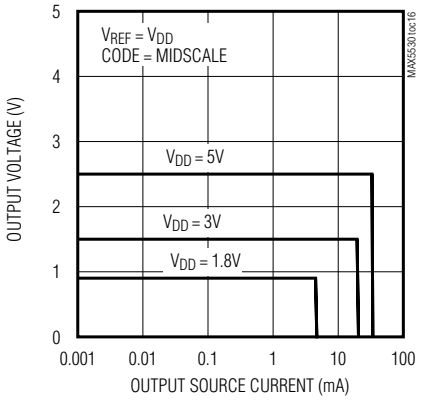
DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT



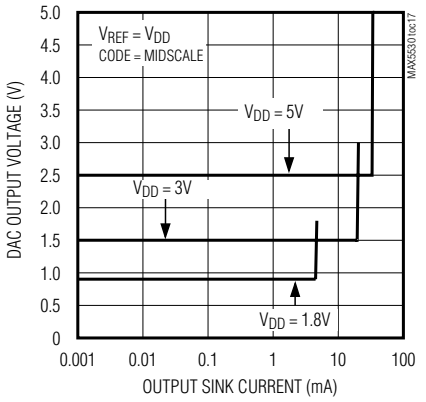
DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT



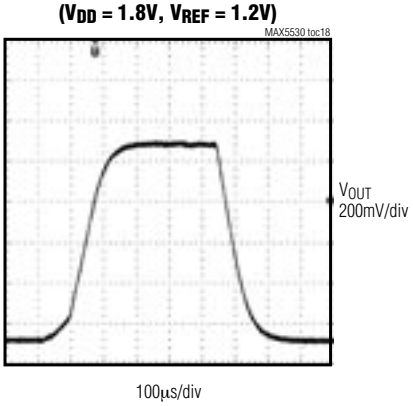
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



OUTPUT LARGE-SIGNAL STEP RESPONSE (V_{DD} = 1.8V, V_{REF} = 1.2V)

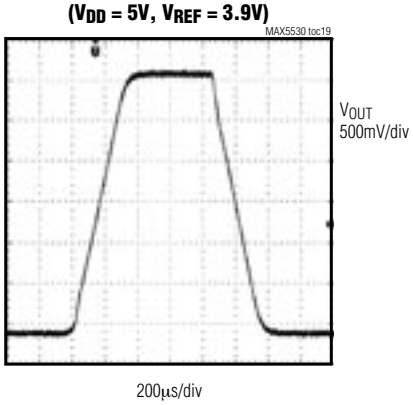


Ultra-Low-Power, 12-Bit, Voltage-Output DACs

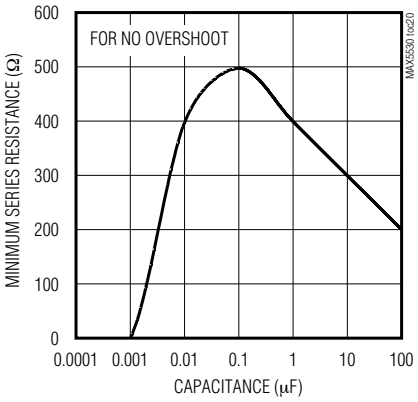
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

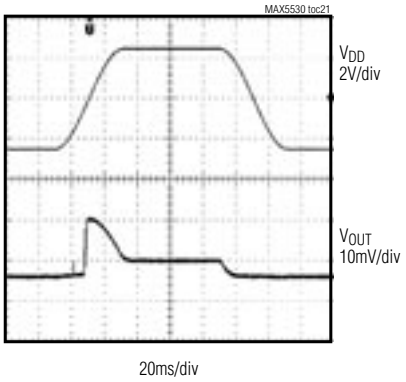
OUTPUT LARGE-SIGNAL STEP RESPONSE (V_{DD} = 5V, V_{REF} = 3.9V)



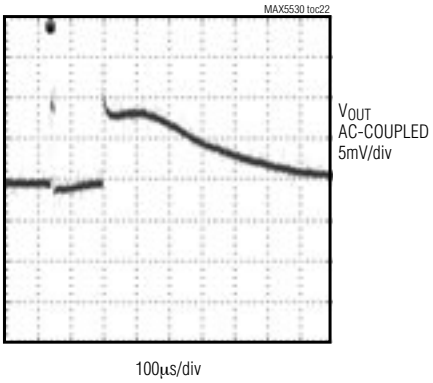
OUTPUT MINIMUM SERIES RESISTANCE vs. LOAD CAPACITANCE



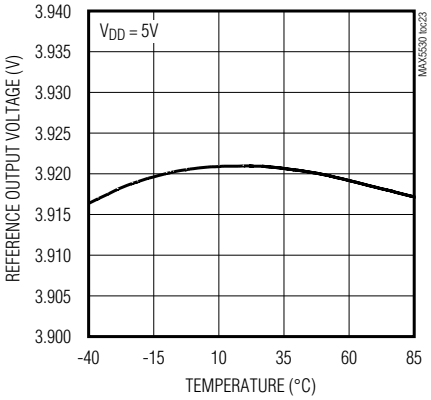
POWER-UP OUTPUT VOLTAGE GLITCH



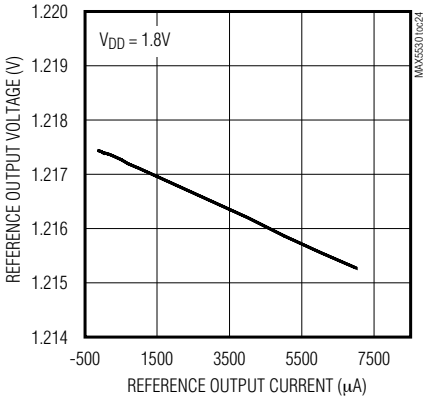
MAJOR CARRY OUTPUT VOLTAGE GLITCH (CODE 7FFh TO 800h) (V_{DD} = 5V, V_{REF} = 3.9V)



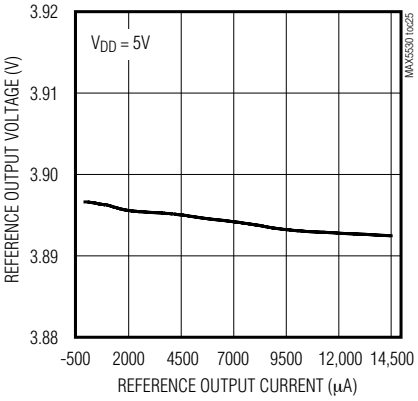
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



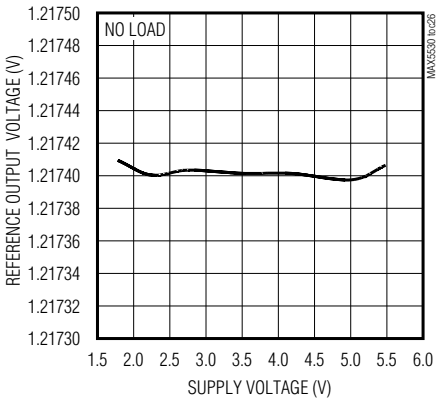
REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT



REFERENCE OUTPUT VOLTAGE vs. REFERENCE OUTPUT CURRENT



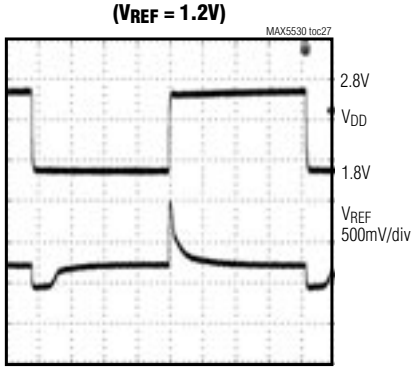
REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



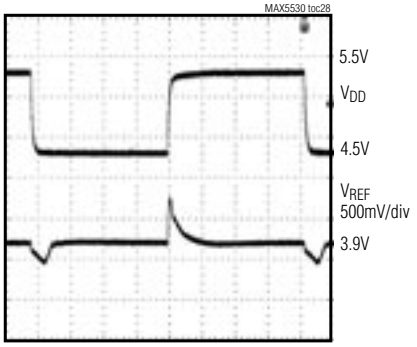
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

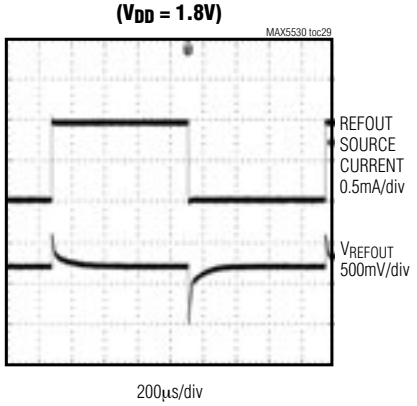
REFERENCE LINE-TRANSIENT RESPONSE (V_{REF} = 1.2V)



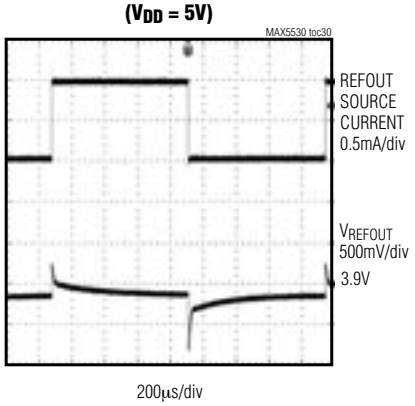
REFERENCE LINE-TRANSIENT RESPONSE (V_{REF} = 3.9V)



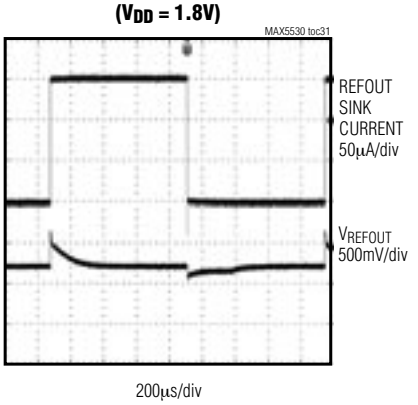
REFERENCE LOAD TRANSIENT (V_{DD} = 1.8V)



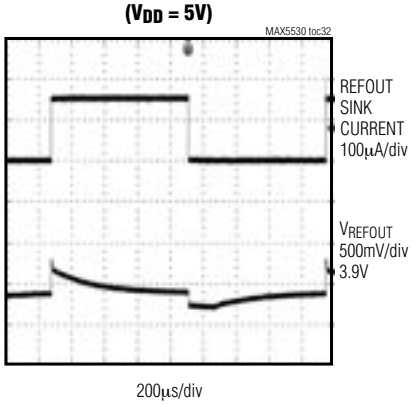
REFERENCE LOAD TRANSIENT (V_{DD} = 5V)



REFERENCE LOAD TRANSIENT (V_{DD} = 1.8V)



REFERENCE LOAD TRANSIENT (V_{DD} = 5V)

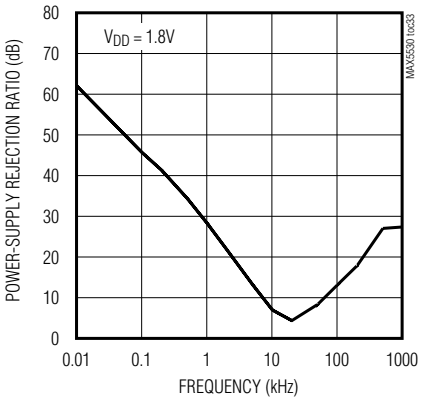


Ultra-Low-Power, 12-Bit, Voltage-Output DACs

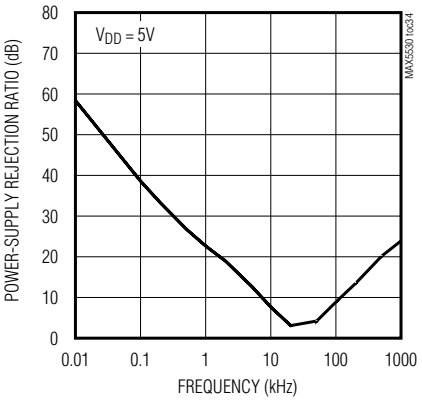
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{REF} = 4.096V (MAX5530), V_{REF} = 3.9V (MAX5531), T_A = +25°C, unless otherwise noted.)

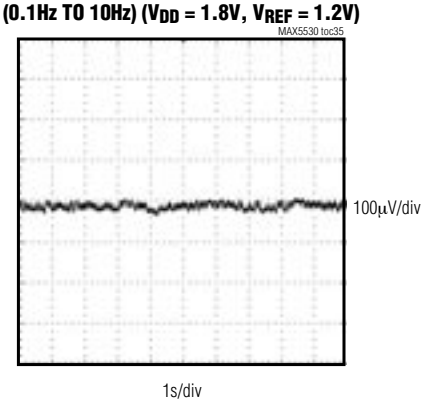
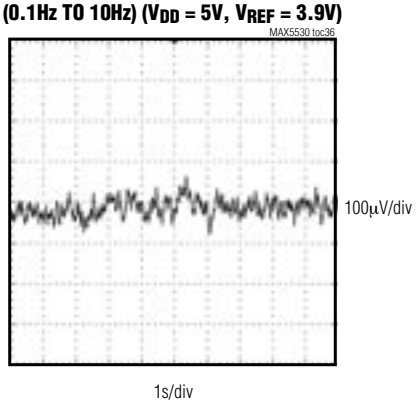
REFERENCE PSRR vs. FREQUENCY



REFERENCE PSRR vs. FREQUENCY



REFERENCE OUTPUT NOISE (0.1Hz TO 10Hz) (V_{DD} = 1.8V, V_{REF} = 1.2V)



REFERENCE OUTPUT NOISE (0.1Hz TO 10Hz) (V_{DD} = 5V, V_{REF} = 3.9V)