



10/100/1000 Base-T Ethernet LAN Switch

General Description

The MAX4890/MAX4891/MAX4892 high-speed analog switches meet the needs of 10/100/1000 Base-T applications. These devices switch the signals from two interface transformers and connect the signals to a single 10/100/1000 Base-T Ethernet PHY, simplifying docking station design and reducing manufacturing costs. The MAX4890/MAX4891/MAX4892 can also route signals from a common interface transformer to two different boards in board-redundancy applications.

The MAX4890/MAX4891/MAX4892 switches provide an extremely low capacitance and on-resistance to meet Ethernet insertion and return-loss specifications. The MAX4891/MAX4892 feature one and three built-in LED switches, respectively.

The MAX4890/MAX4891/MAX4892 are available in space-saving 32- and 36-lead TQFN packages, significantly reducing the required PC board area. These devices operate over the -40°C to +85°C temperature range.

Applications

Notebooks and Docking Stations
Servers and Routers with Ethernet Interfaces
Board-Level Redundancy Protection
SONET/SDH Signal Routing
T3/E3 Redundancy Protection
Video Switching

Features

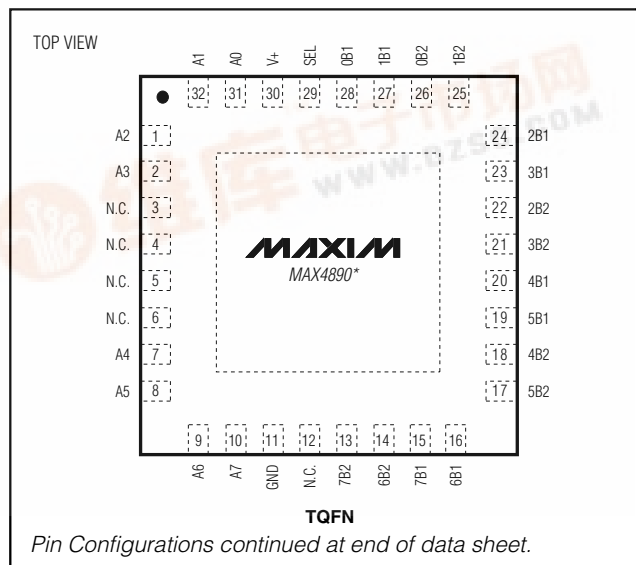
- ◆ Single +3.0V to +3.6V Power-Supply Voltage
- ◆ Low On-Resistance (R_{ON}): 4Ω (typ), 6.5Ω (max)
- ◆ Ultra-Low On-Capacitance (C_{ON}): 6.5pF (typ)
- ◆ Low < 200ps Bit-to-Bit Skew
- ◆ -3dB Bandwidth: 1GHz
- ◆ Optimized Pin-Out for Easy Transformer and PHY Interface
- ◆ Built-In LED Switches for Switching Indicators to Docking Station
- ◆ Low 450μA (max) Quiescent Current
- ◆ Bidirectional 8 to 16 Multiplexer/Demultiplexer
- ◆ Space-Saving Packages
 - 32-Pin, 5mm x 5mm, TQFN Package
 - 36-Pin, 6mm x 6mm, TQFN Package

Ordering Information

PART	PIN-PACKAGE	LED SWITCHES	PKG CODE
MAX4890ETJ	32 TQFN	—	T-3255-4
MAX4891ETJ	32 TQFN	1	T-3255-4
MAX4892ETX	36 TQFN	3	T-3666-3

All devices are available in the -40°C to +85°C operation temperature range.

Pin Configurations



Typical Operating Circuit appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

V+ -0.3V to +4V
 SEL (Note 1) -0.3V to (V+ +0.3V)
 A₋, B₋, LED₋, LED₋ -0.3V to (V+ +0.3V)
 Continuous Current (A₋ to B₋) ±120mA
 Continuous Current (LED₋ to LED₋) ±30mA
 Peak Current (A₋ to B₋)
 (pulsed at 1ms, 10% duty cycle) ±240mA

Continuous Power Dissipation (T_A = +70°C)
 32-Pin TQFN (derate 34.5mW/°C above +70°C) 2.76W
 36-Pin TQFN (derate 26.3mW/°C above +70°C) 2.11W
 Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Note 1: Signals on SEL, exceeding V+ or GND, are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCH							
On-Resistance	R _{ON}	V ₊ = 3V, I _{A-} = -40mA, 1.5V ≤ V _{A-} ≤ V ₊	T _A = +25°C		4	5.5	Ω
			T _{MIN} to T _{MAX}			6.5	
On-Resistance LED Switches	R _{ONLED}	V ₊ = 3V, I _{LED-} = -40mA, 1.5V ≤ V _{A-} ≤ V ₊ , MAX4891/MAX4892				40	Ω
On-Resistance Match Between Channels	ΔR _{ON}	V ₊ = 3V, I _{A-} = -40mA, 1.5V ≤ V _{A-} ≤ V ₊ (Note 3)	T _A = +25°C		0.5	1.5	Ω
			T _{MIN} to T _{MAX}			2	
On-Resistance Flatness	R _{FLAT(ON)}	V ₊ = 3V, I _{A-} = -40mA, V _{A-} = 1.5V, 2.7V			0.01		Ω
Off-Leakage Current	I _{LA-(OFF)}	V ₊ = 3.6V, V _{A-} = 0.3V, 3.3V V _{B1} or V _{B2} = 3.3V, 0.3V		-1		+1	μA
On-Leakage Current	I _{LA-(ON)}	V ₊ = 3.6V, V _{A-} = 0.3V, 3.3V V _{B1} or V _{B2} = 0.3V, 3.3V or floating		-1		+1	
ESD PROTECTION							
ESD Protection		Human Body Model			±2		kV
SWITCH AC PERFORMANCE							
Insertion Loss	I _{LOS}	Insertion loss with typical transformer, R _L = 100Ω, 1MHz < f < 100MHz, Figure 1 (Note 3)			0.6		dB
Return Loss	R _{LOS1}	Return loss with typical transformer, R _L = 100Ω, return	1MHz < f < 40MHz		-19		dB
	R _{LOS2}	loss, f in MHz, Figure 2 (Note 3)	40MHz < f < 100MHz		-13 +20log (f/80)		

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = +3V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk	VCT1	Any switch to any switch R _L = 100Ω, Figure 3	1MHz < f < 30MHz	-45		dB	
	VCT2		30MHz < f < 60MHz				
	VCT3		60MHz < f < 100MHz				
Differential Crosstalk	VDCT1	R _L = 100Ω, Figure 4	1MHz < f < 30MHz	-60		dB	
	VDCT2		30MHz < f < 60MHz				
	VDCT3		60MHz < f < 100MHz				
SWITCH DYNAMICS							
On-Channel -3dB Bandwidth	BW	R _L = 100Ω, Differential pair		1000		MHz	
Off-Capacitance	C _{OFF}	f = 1MHz, _B_ inputs		3.5		pF	
On-Capacitance	C _{ON}	f = 1MHz, _B_ inputs		6.5		pF	
Off-Capacitance, LED Switches	C _{OFFLED}	f = 1MHz, _LED inputs		20		pF	
On-Capacitance, LED Switches	C _{ONLED}	f = 1MHz, _LED inputs		22		pF	
Turn-On Time	t _{ON}	V _{A_} = 1V, Figure 5		25	50	ns	
Turn-Off Time	t _{OFF}	V _{A_} = 1V, Figure 5		20	40	ns	
Propagation Delay	t _{PLH} , t _{PHL}	C _L = 10pF, Figure 6		0.15		ns	
Output Skew Between Ports	t _{SK(o)}	Skew between A4 and A5 and any other port, Figure 7		0.01		ns	
Output Skew Same Port	t _{SK(p)}	Skew between opposite transitions in same port		0.07		ns	
SWITCH LOGIC							
Input-Voltage Low	V _{IL}			0.8		V	
Input-Voltage High	V _{IH}			2.0			
Input-Logic Hysteresis	V _{HYST}			100		mV	
Input Leakage Current	I _{SEL}	V+ = 3.6V, V _{SEL} = 0 or V+		-5	+5	uA	
Operating Supply-Voltage Range	V+			3	3.6	V	
Quiescent Supply Current	I+	V+ = 3.6V, V _{SEL} = 0 or V+		280	450	μA	

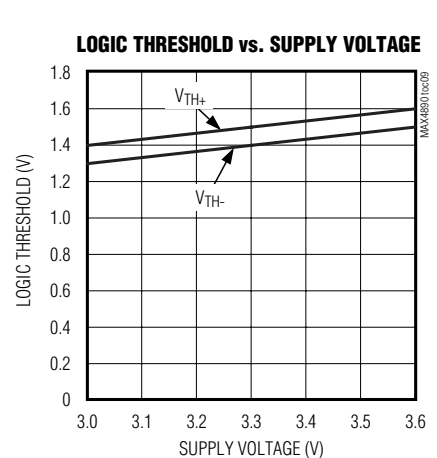
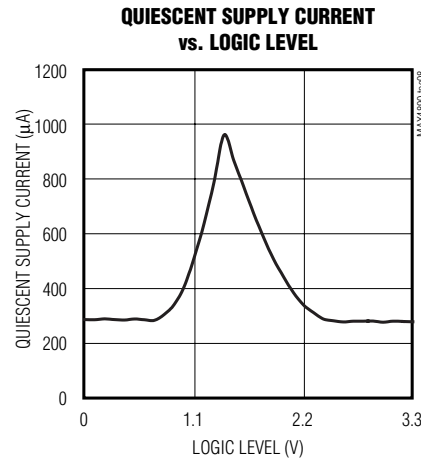
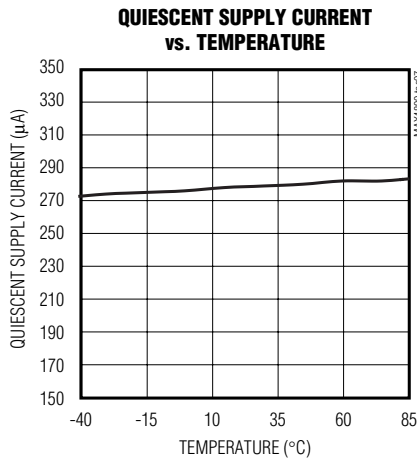
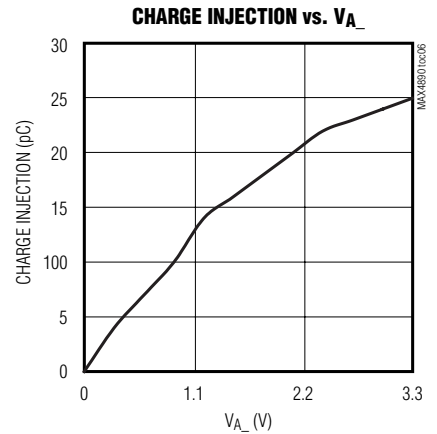
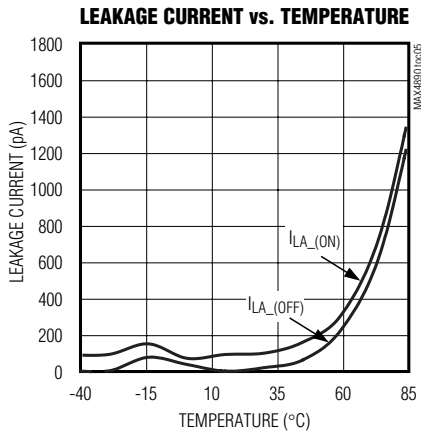
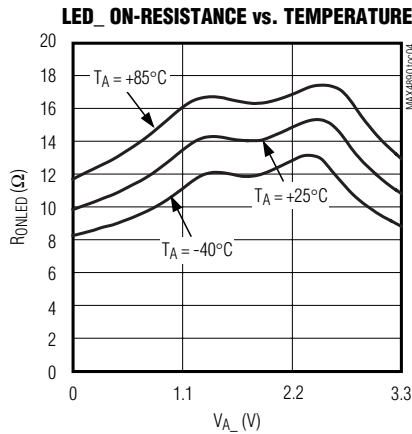
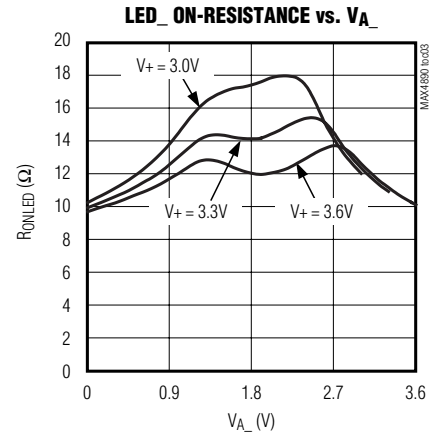
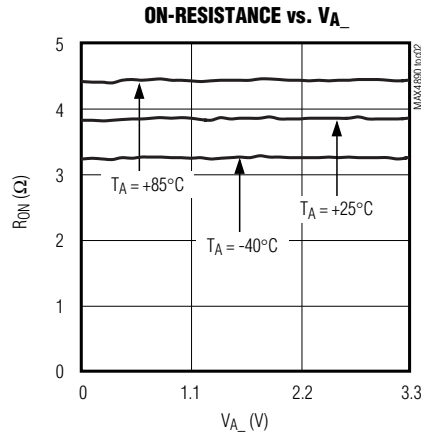
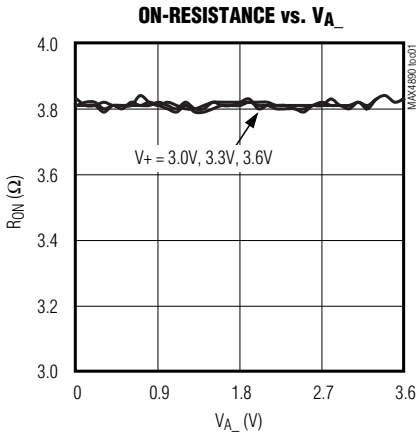
Note 2: Specifications at -40°C are guaranteed by design.

Note 3: Guaranteed by design.

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Typical Operating Characteristics

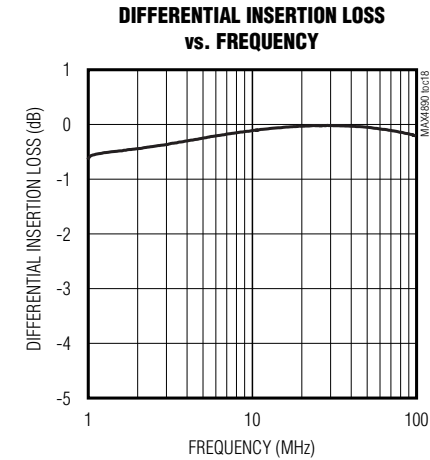
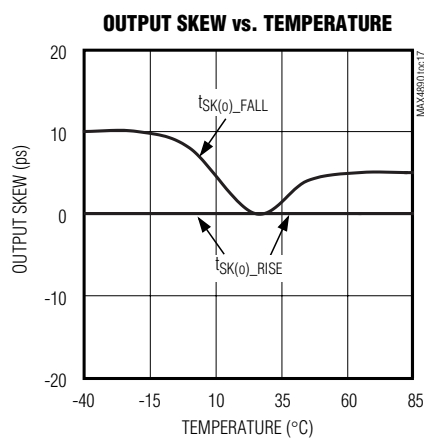
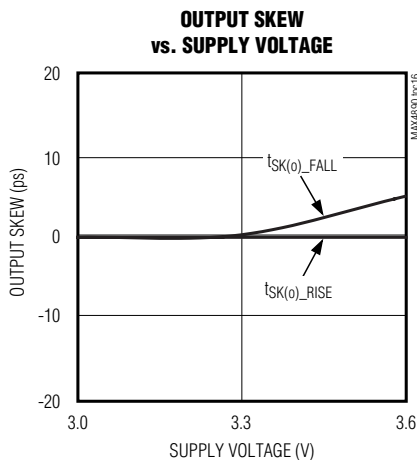
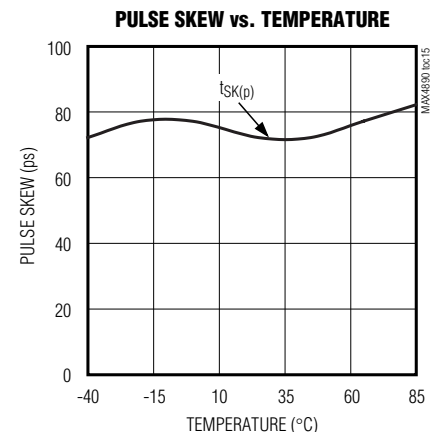
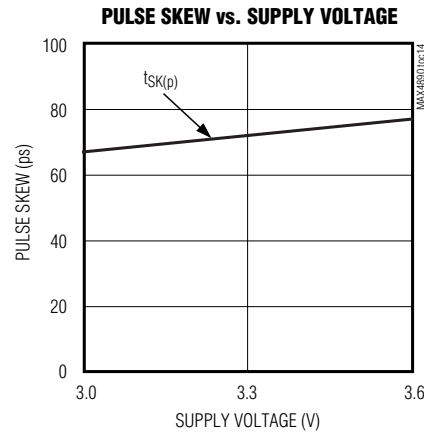
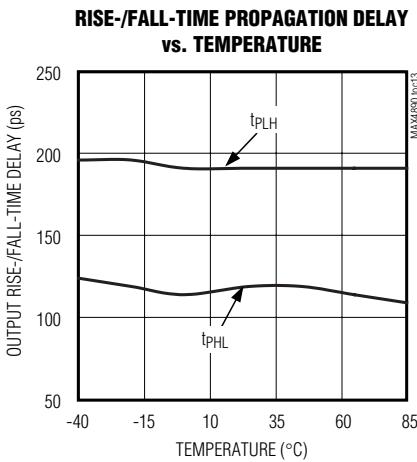
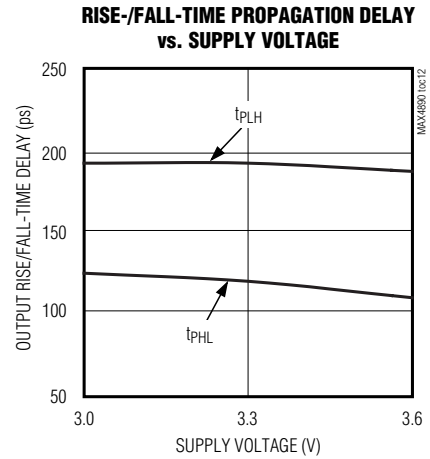
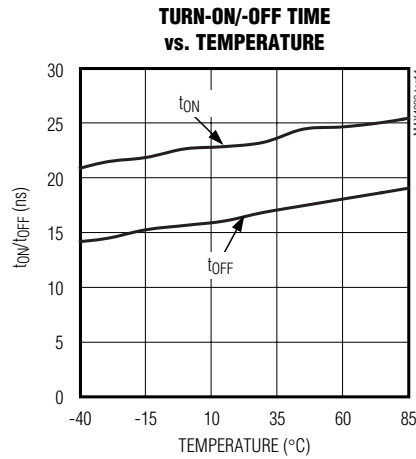
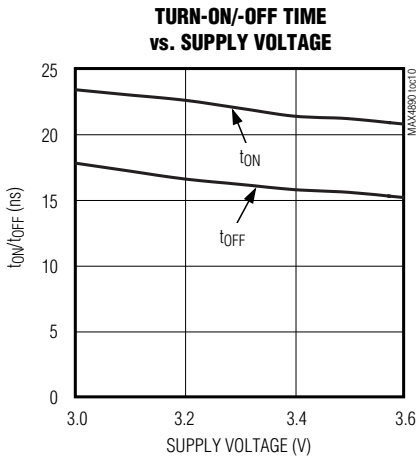
($V_+ = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

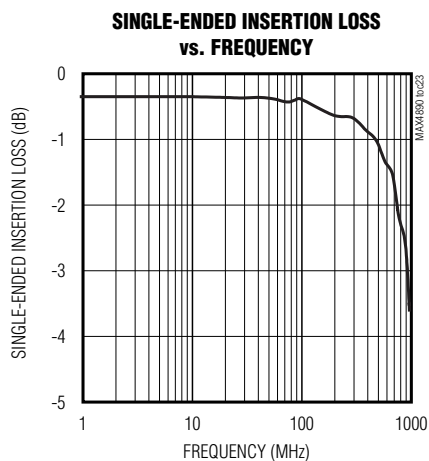
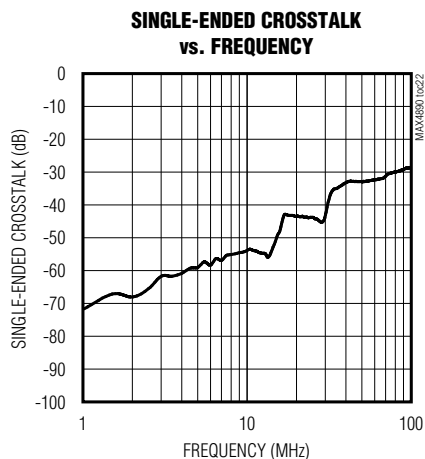
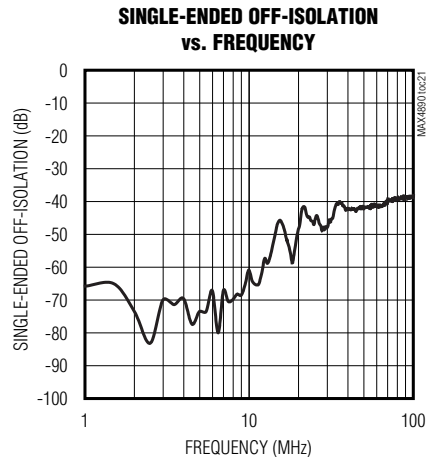
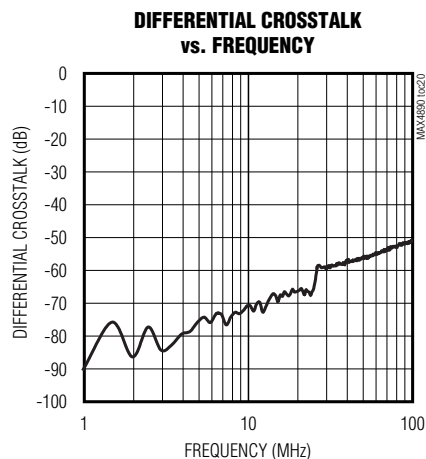
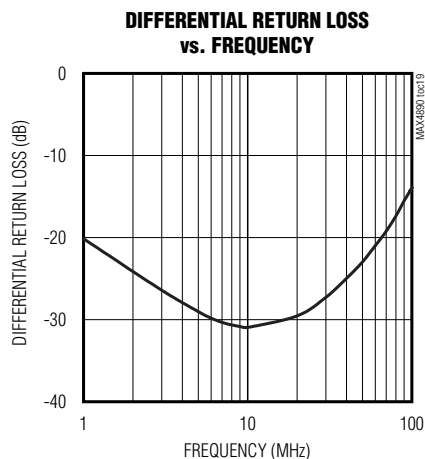
($V_+ = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_+ = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



10/100/1000 Base-T Ethernet LAN Switch

Pin Description

PIN			NAME	FUNCTION
MAX4890	MAX4891	MAX4892		
31, 32, 1, 2, 7–10	31, 32, 1, 2, 7–10	36, 1, 2, 3, 7–10	A0–A7	Differential PHY Interface Pair. Connects to the Ethernet PHY.
—	3	4	LED0	LED0 Input
—	4	5	0LED1	0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.
—	5	6	0LED2	0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.
3–6, 12	6, 12	—	N.C.	No Connection. Not internally connected.
11	11	11	GND	Ground
—	—	12	LED1	LED1 Input
—	—	13	1LED1	1LED1 Output. Connects LED1 to 1LED1 when SEL = 0.
—	—	14	1LED2	1LED2 Output. Connects LED1 to 1LED2 when SEL = 1.
13, 14, 17, 18, 21, 22, 25, 26	13, 14, 17, 18, 21, 22, 25, 26	15, 16, 19, 20, 23, 24, 28, 29	7B2–0B2	B2 Differential Transformer Pair
15, 16, 19, 20, 23, 24, 27, 28	15, 16, 19, 20, 23, 24, 27, 28	17, 18, 21, 22, 25, 26, 30, 31	7B1–0B1	B1 Differential Transformer Pair
29	29	27	SEL	Select Input. Selects switch connection. See the Truth Table (Table 1).
—	—	32	2LED2	2LED2 Output. Connects LED2 to 2LED2 when SEL = 1.
—	—	33	2LED1	2LED1 Output. Connects LED2 to 2LED1 when SEL = 0.
—	—	34	LED2	LED2 Input
30	30	35	V+	Positive Supply-Voltage Input
EP	EP	EP	EP	Exposed Paddle. Not internally connected. Leave unconnected or connect to ground.

MAX4890/MAX4891/MAX4892

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Test Circuits

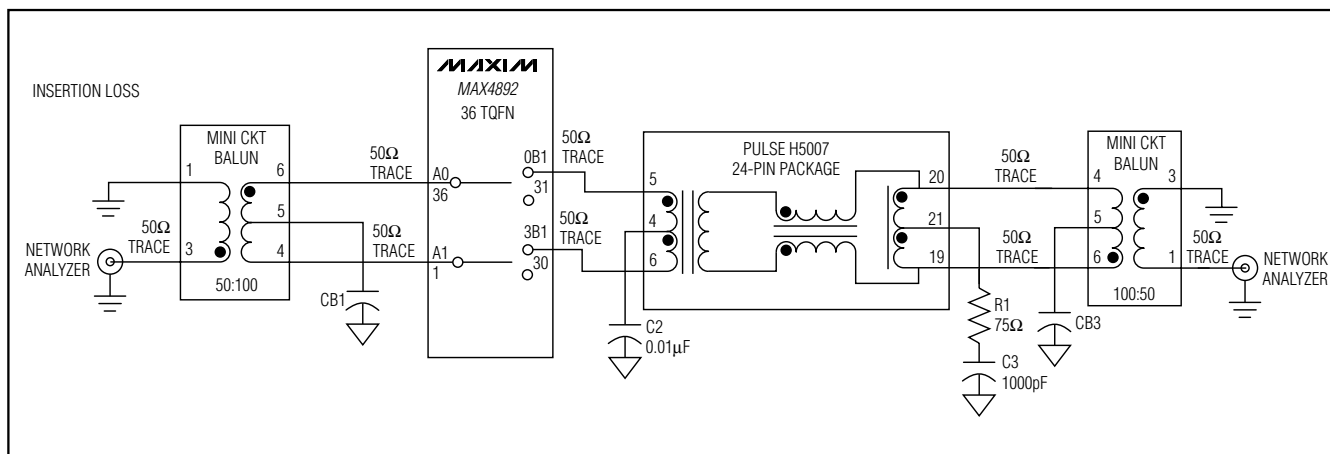


Figure 1. Differential Insertion Loss

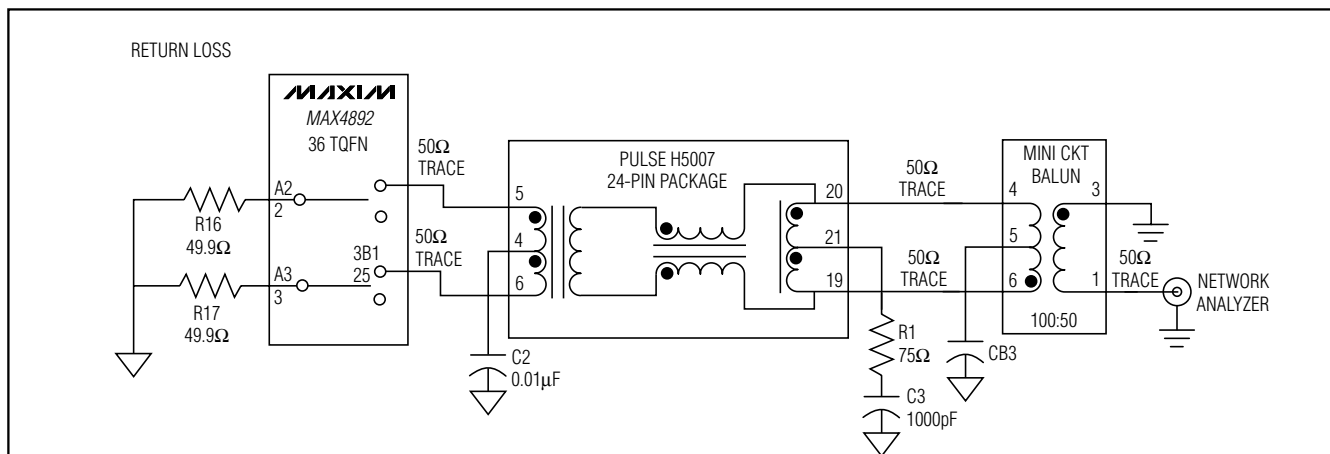


Figure 2. Differential Return Loss

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Test Circuits (continued)

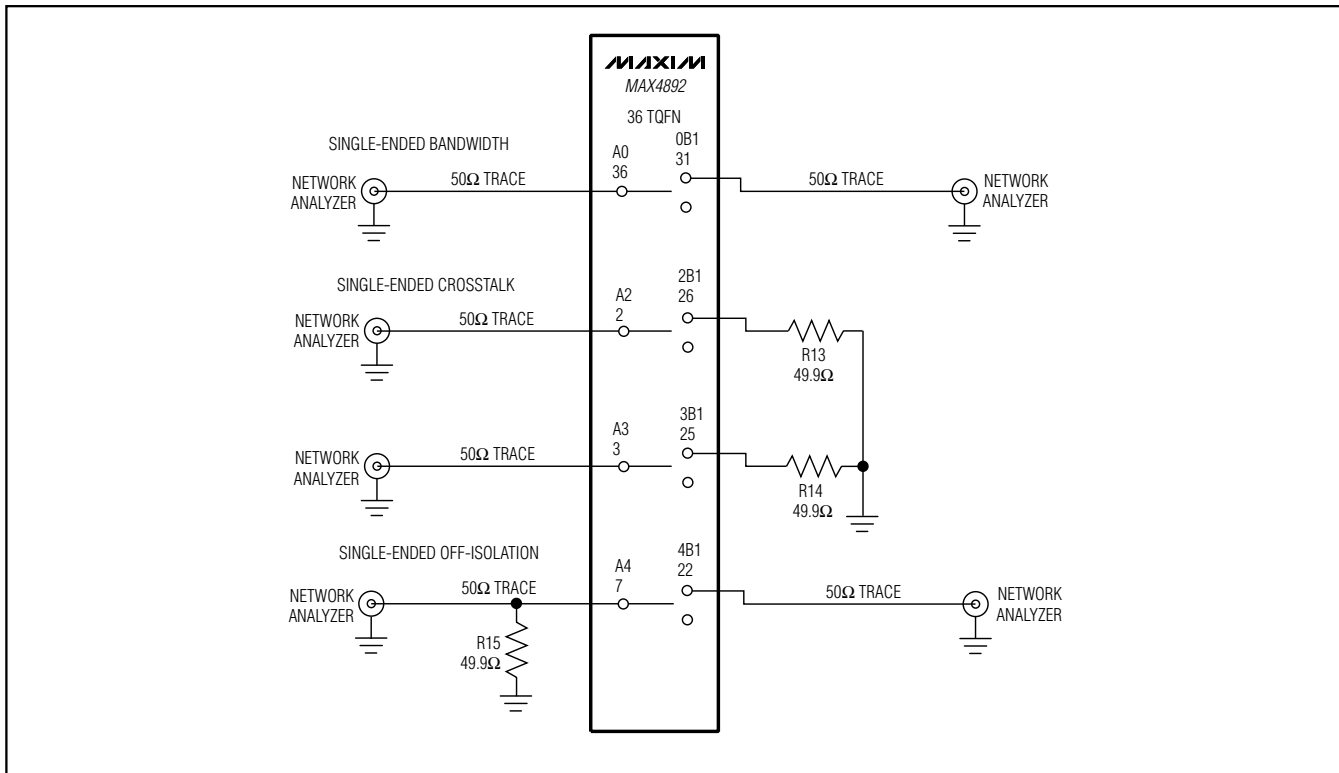


Figure 3. Single-Ended Bandwidth, Crosstalk and Off-Isolation

Detailed Description

The MAX4890/MAX4891/MAX4892 are high-speed analog switches targeted for 10/100/1000 Base-T applications. In a typical application, the MAX4890/MAX4891/MAX4892 switch the signals from two separate interface transformers and connect the signals to a single 10/100/1000 Base-T Ethernet PHY (see the *Typical Operating Circuit*). This configuration simplifies docking station design by avoiding signal reflections associated with unterminated transmission lines in a T configuration. The MAX4891 and MAX4892 also include LED switches that allow the LED output signals to be routed to a docking station along with the Ethernet signals. See the *Functional Diagrams*.

The MAX4890/MAX4891/MAX4892 switches provide an extremely low capacitance and on-resistance to meet Ethernet insertion and return-loss specifications. The MAX4891/MAX4892 feature one and three built-in LED switches, respectively.

The MAX4890/MAX4891/MAX4892 incorporate a unique architecture design utilizing only n-channel switches

within the main Ethernet switch, reducing I/O capacitance and channel resistance. An internal two-stage charge pump with a nominal output of 7.5V provides the high voltage needed to drive the gates of the n-channel switches, while maintaining a consistently low R_{ON} throughout the input signal range. An internal bandgap reference set to 1.23V and an internal oscillator running at 2.5MHz provide proper charge-pump operation. Unlike other charge-pump circuits, the MAX4890/MAX4891/MAX4892 include internal flyback capacitors, reducing design time, board space, and cost.

Digital Control Inputs

The MAX4890/MAX4891/MAX4892 provide a single digital control SEL. SEL controls the switches as well as the LED switches as shown in Table 1.

Table 1. Truth Table

SEL	CONNECTION
0	A_ to _B1, LED_ to _LED1
1	A_ to _B2, LED_ to _LED2

10/100/1000 Base-T Ethernet LAN Switch

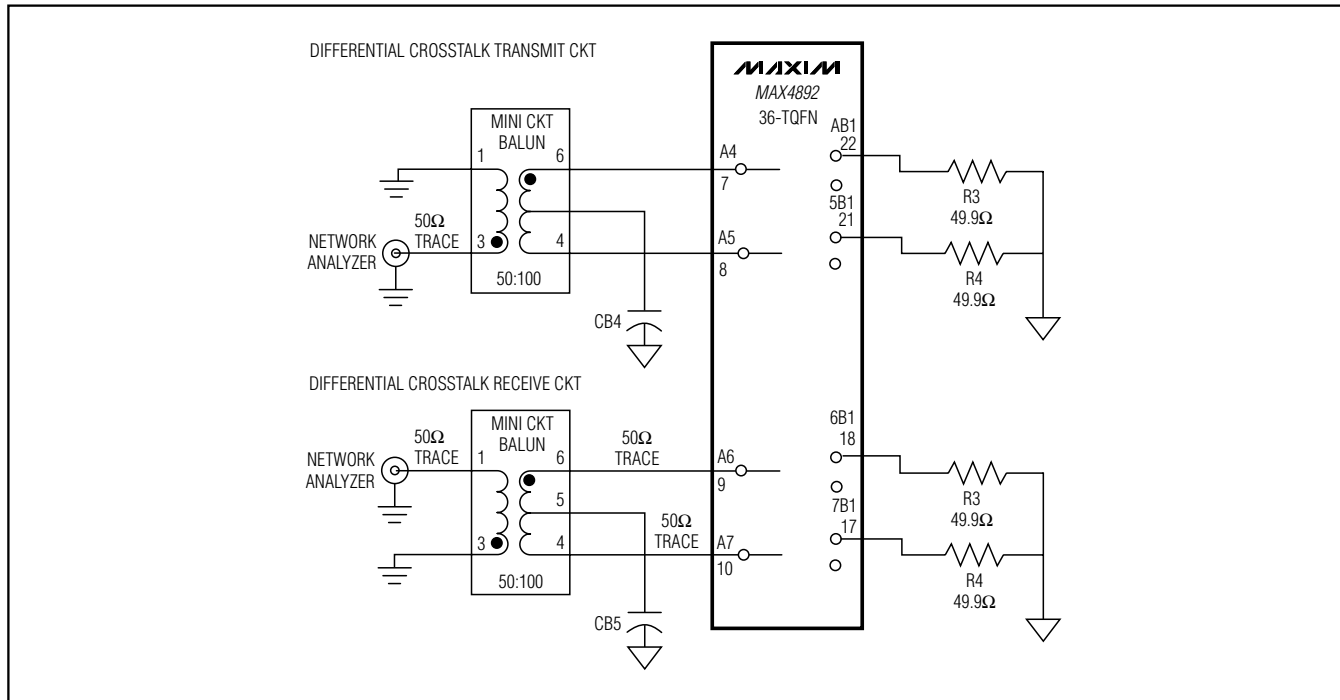


Figure 4. Differential Crosstalk

Analog Signal Levels

The on-resistance of the MAX4890/MAX4891/MAX4892 is very low and stable as the analog input signals are swept from ground to V_+ (see the *Typical Operating Characteristics*). The switches are bidirectional, allowing A_ and _B_ to be configured as either inputs or outputs.

ESD Protection

The MAX4890/MAX4891/MAX4892 are characterized using the Human Body Model for $\pm 2\text{kV}$ of ESD protection. Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform the Human Body Model generates when discharged into a low-impedance load. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5k Ω resistor.

Applications Information

Typical Operating Circuit

The *Typical Operating Circuit* depicts the MAX4890/MAX4891/MAX4892 in a 10/100/1000 Base-T docking station application.

Line-Card Redundancy (Ethernet T3/E3)

Figure 10 shows the MAX4890/MAX4891/MAX4892 in a line-card redundancy configuration.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_+ before applying analog signals, especially if the analog signal is not current limited.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled-impedance printed circuit board traces as short as possible. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

10/100/1000 Base-T Ethernet LAN Switch

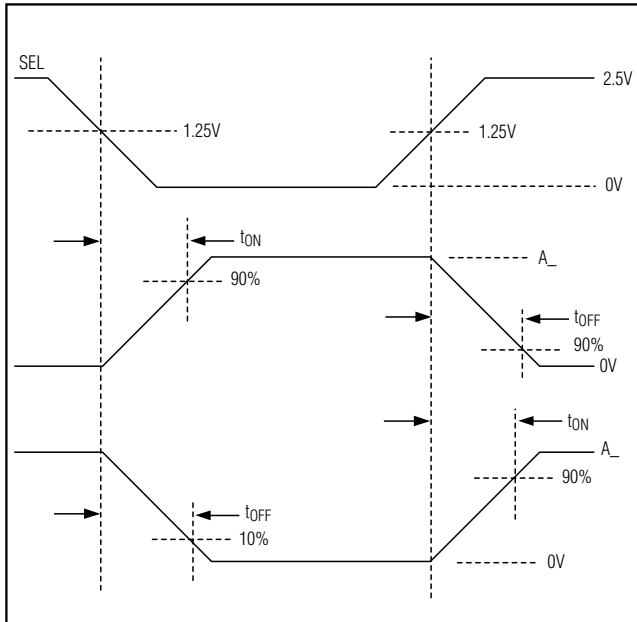


Figure 5. ENABLE and DISABLE Times

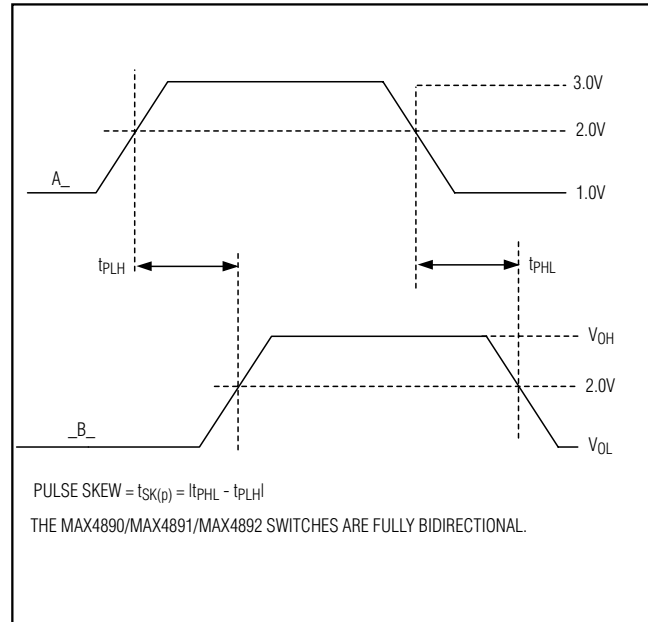


Figure 6. Propagation Delay Times

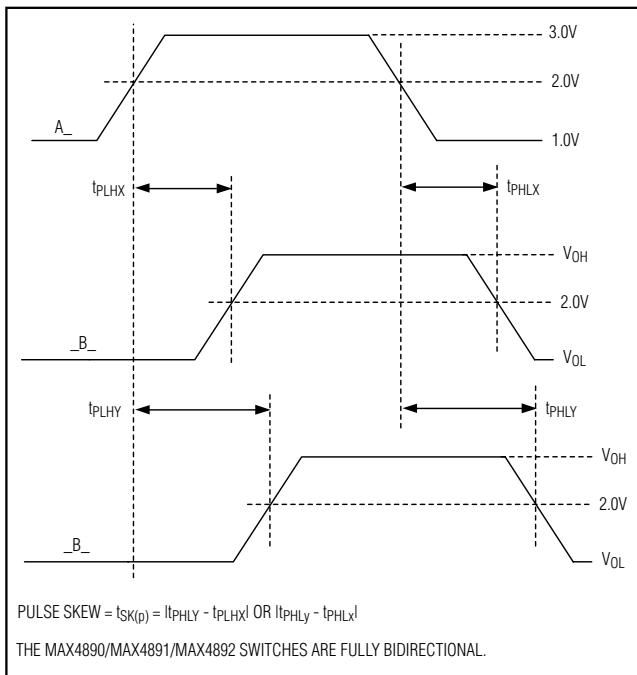


Figure 7. Output Skew

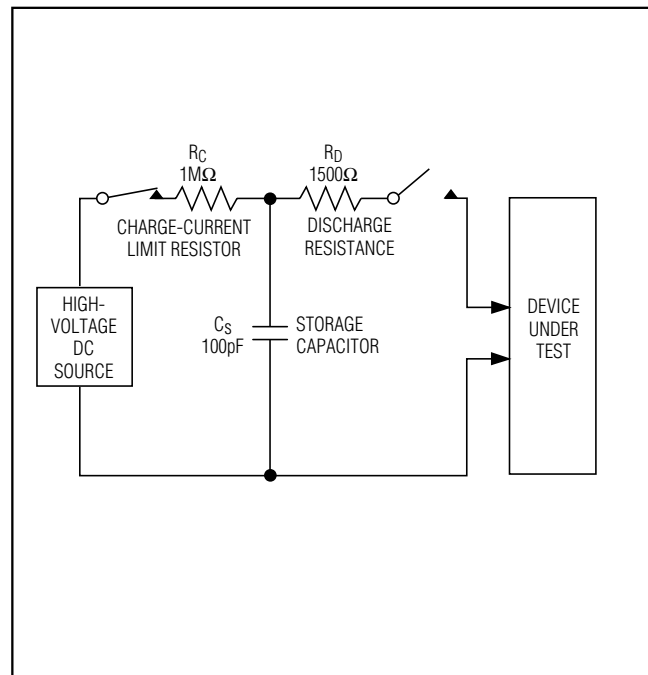


Figure 8. Human Body ESD Test Model

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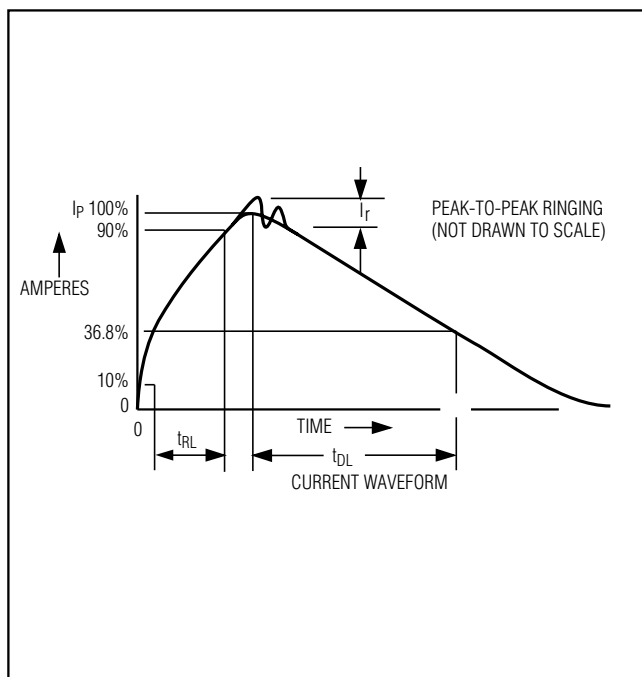


Figure 9. Human Body Model Current Waveform

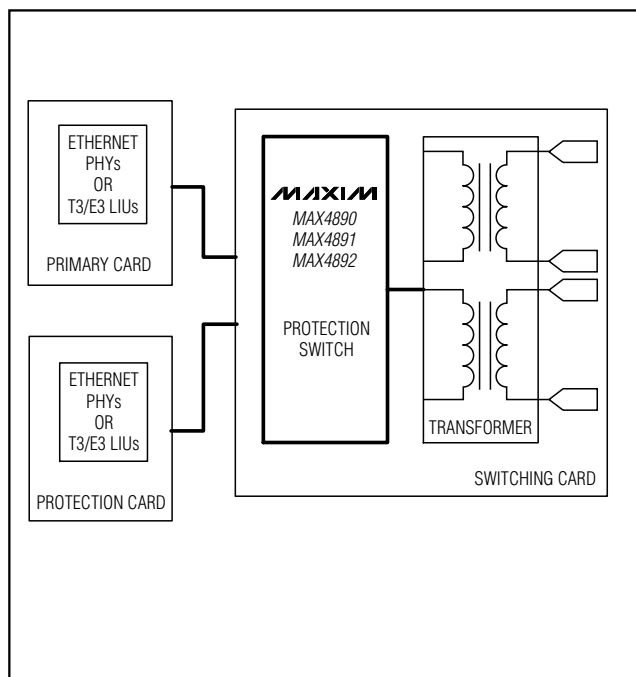
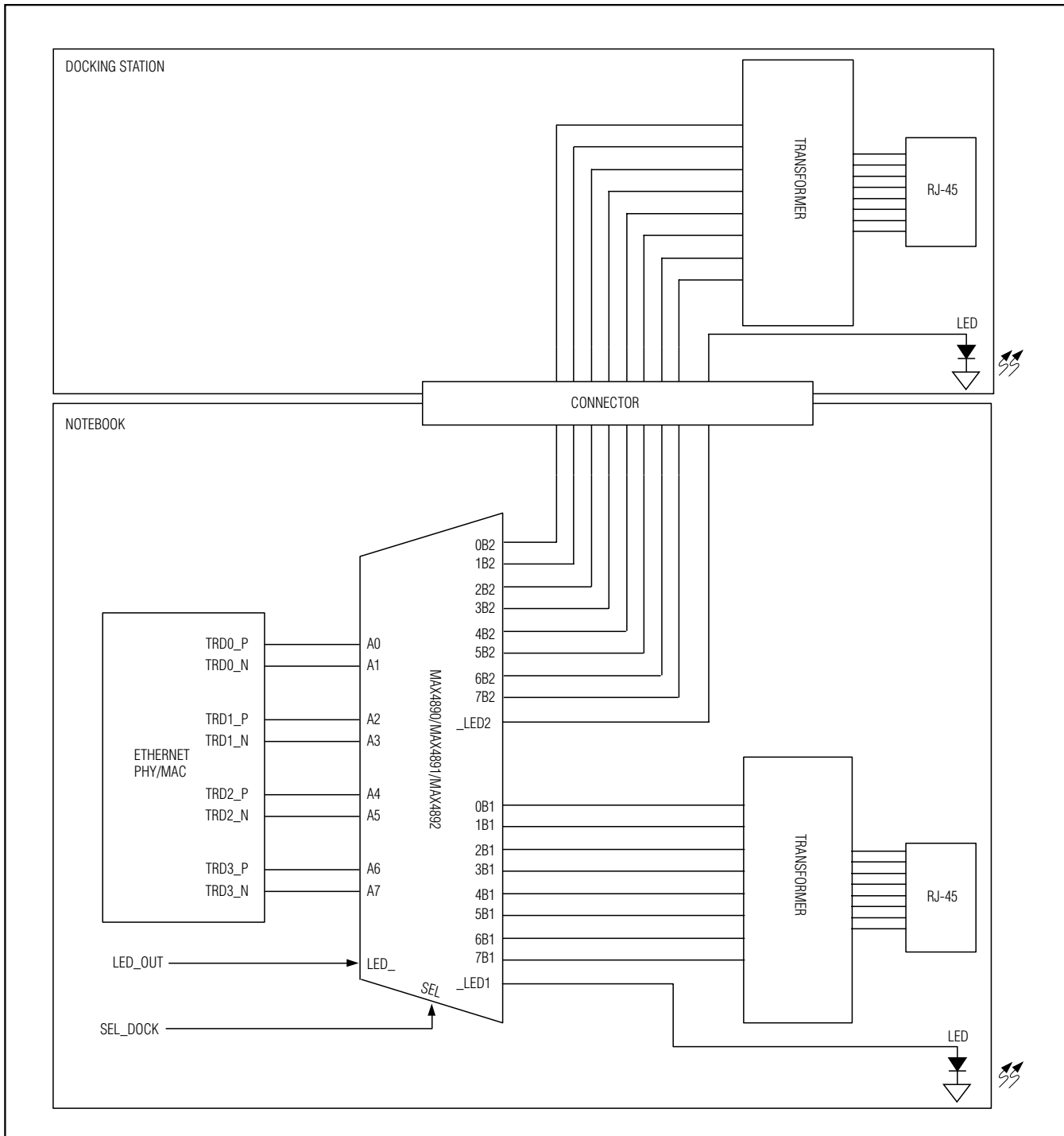


Figure 10. Typical Application for Line-Card Redundancy

10/100/1000 Base-T Ethernet LAN Switch

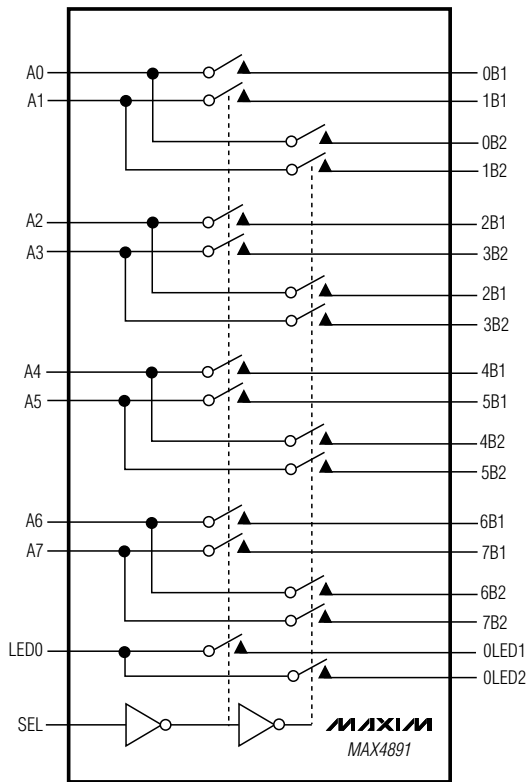
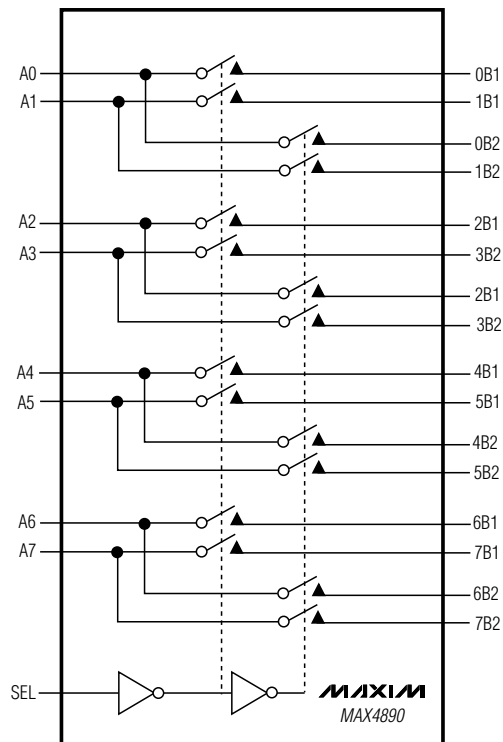
Typical Operating Circuit

MAX4890/MAX4891/MAX4892



10/100/1000 Base-T Ethernet LAN Switch

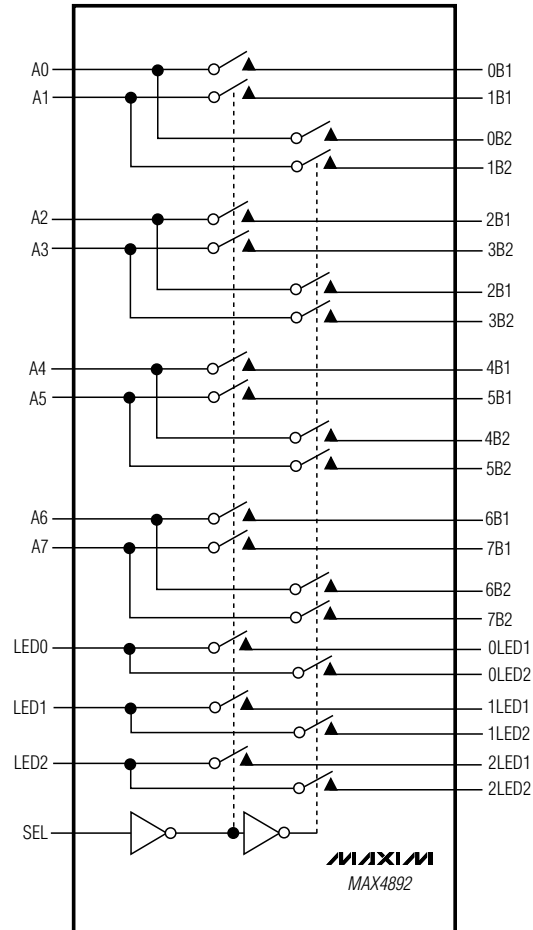
Functional Diagrams



10/100/1000 Base-T Ethernet LAN Switch

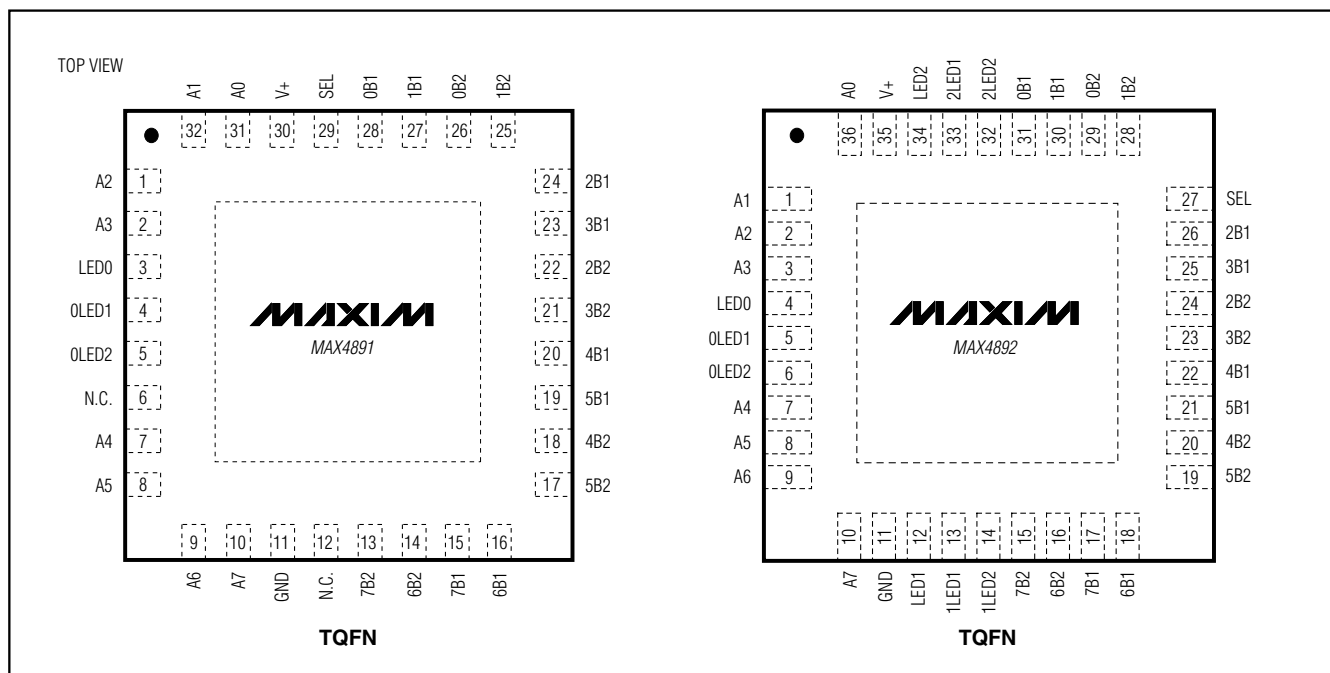
Functional Diagrams (continued)

MAX4890/MAX4891/MAX4892



10/100/1000 Base-T Ethernet LAN Switch

Pin Configurations (continued)



Chip Information

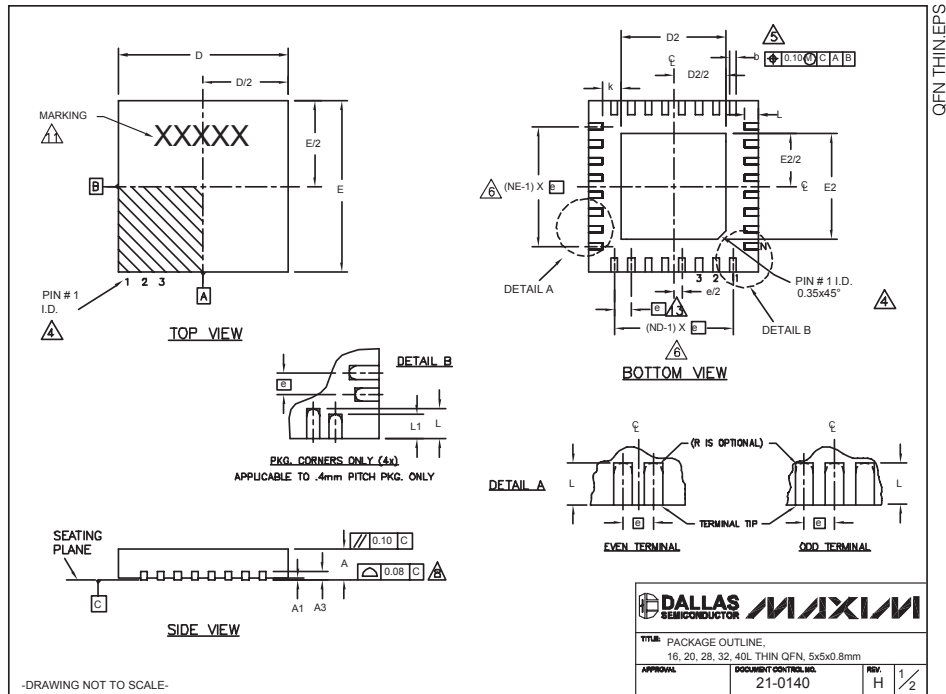
TRANSISTOR COUNT: 948

PROCESS: BiCMOS

10/100/1000 Base-T Ethernet LAN Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



COMMON DIMENSIONS															
PKG. SYMBOL	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35	0.25	0.30	0.35	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3. N IS THE TOTAL NUMBER OF TERMINALS.

△

THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

△

DIMENSION B APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.

△

ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

△

DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

△

COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

△

DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.

△

WARPAGE SHALL NOT EXCEED 0.10 mm.

△

MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

△

NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

△

LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", 40.50.

-DRAWING NOT TO SCALE-

EXPOSED PAD VARIATIONS								
PKG CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

DALLAS

SEMICONDUCTOR

MAXIM

TITLE: PACKAGE OUTLINE;
16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL DOCUMENT CONTROL NO. 21-0140 REV. H 2/2

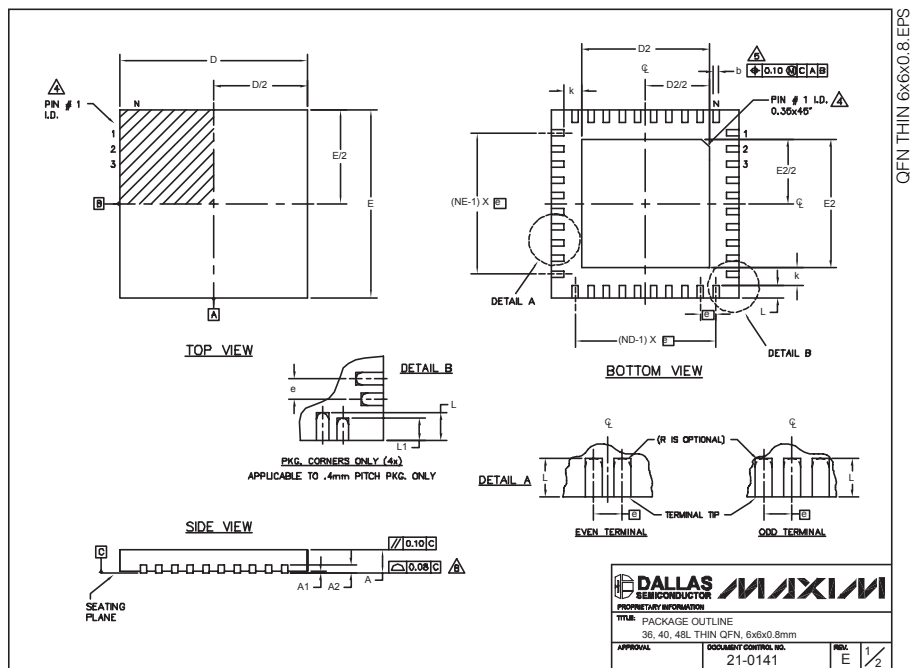
NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
- WARPAGE SHALL NOT EXCEED 0.10 mm.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

10/100/1000 Base-T Ethernet LAN Switch

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
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- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
- WARPAGE SHALL NOT EXCEED 0.10 mm.

PKG. CODES	EXPOSED PAD VARIATIONS						DOWN BONDS ALLOWED
	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.80	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.80	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.80	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE			
36, 40, 48L THIN QFN, 6x6x0.8mm			
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	E	2/2

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