19-3037; Rev 2; 2/05

High-Bandwidth, Quad DPDT Switches

General Description

The MAX4760/MAX4761 (DPDT) analog switches operate from a single +1.8V to +5.5V supply. These switches feature a low 25pF capacitance for high-speed data switching applications.

The MAX4760 is a quad double-pole/double-throw (DPDT) switch and the MAX4761 is an octal single-pole/double-throw (SPDT) switch. They have eight 3.5Ω on-resistance, low-capacitance switches to route audio and data signals. The MAX4760 has 4 logic inputs to control the switches in pairs. The MAX4761 has one logic control input and an enable input ($\overline{EN}$) to disable the switches.

The MAX4760/MAX4761 are available in a small 36-pin (6mm x 6mm) thin QFN and 36-bump (3mm x 3mm) chip-scale package (UCSP™).

Applications

USB Signal Switching
Audio-Signal Routing
Cellular Phones
PDAs/Hand-Held Devices
Notebook Computers

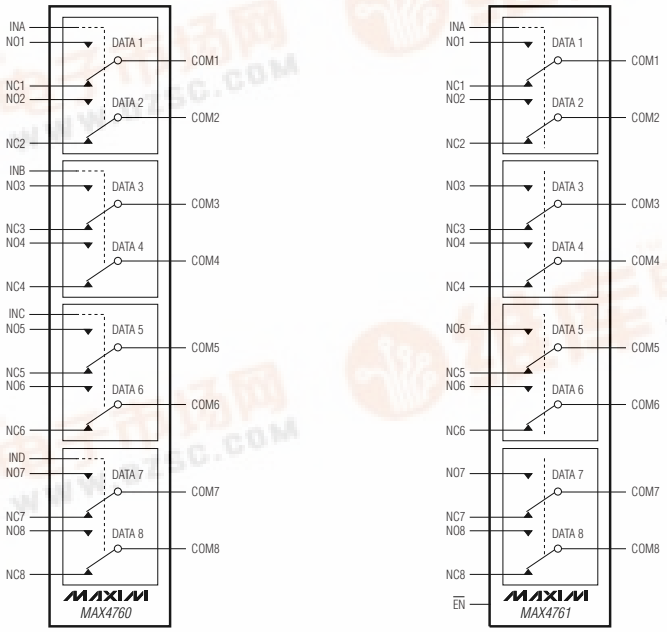
Features

- **USB 1.1 and USB 2.0 (Full Speed) Signal-Switching Compliant**
- **Data and Audio Signal Routing**
- **Low-Capacitance (25pF) Data Switches**
- **Less than 0.2ns Skew**
- **-3dB Bandwidth: 325MHz**
- **0.2Ω Channel-to-Channel Matching**
- **0.8Ω On-Resistance Flatness**
- **Rail-to-Rail Signal Handling**
- **0.03% THD**
- **+1.8V to +5.5V Supply Range**
- **Tiny 36-Bump UCSP (3mm x 3mm)**
- **36-Pin Thin QFN (6mm x 6mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4760EBX-T	-40°C to +85°C	36 UCSP-36
MAX4760ETX	-40°C to +85°C	36 Thin QFN (6mm x 6mm)
MAX4761EBX-T	-40°C to +85°C	36 UCSP-36
MAX4761ETX	-40°C to +85°C	36 Thin QFN (6mm x 6mm)

Functional Diagrams



Pin Configurations/Functional Diagrams/Truth Table continued at end of data sheet.

High-Bandwidth, Quad DPDT Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+, IN_, $\overline{EN}$.....-0.3V to +6V
COM_, NO_, NC_ (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current
NO_, NC_, COM_ .....±100mA
Peak Current
(pulsed at 1ms, 10% duty cycle).....±200mA
(pulsed at 1ms, 50% duty cycle)..... ±300mA
Continuous Power Dissipation (T_A = +70°C)
36-Bump UCSP (derate 15.3mW/°C above +70°C).... 1221mW
36-Pin Thin QFN (derate 26.3mW/°C above +70°C)... 2105mW
ESD per Method 3015.7.....±2kV
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Bump Temperature (soldering)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$,		T_{MIN} to T_{MAX}	0		V+	V
On-Resistance (Note 4)	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NC\_}$ or $V_{NO\_}$ = 0V or V+	+25°C		2.0	3.5	Ω
			T_{MIN} to T_{MAX}			4	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.2	0.4	Ω
			T_{MIN} to T_{MAX}			0.55	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$=10mA, $V_{NC\_}$ or $V_{NO\_}$ = 0V or V+	+25°C		0.8	1.5	Ω
			T_{MIN} to T_{MAX}			1.8	
NO_, NC_ Off-Leakage Current	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V	+25°C	-5		+5	nA
			T_{MIN} to T_{MAX}	-25		+25	
COM_ Off-Leakage Current		V+ = 3.6V (MAX4761); $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V	+25°C	-5	0.01	+5	nA
			T_{MIN} to T_{MAX}	-25		+25	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V or floating	+25°C	-5		+5	nA
			T_{MIN} to T_{MAX}	-25		+25	
DYNAMIC							
Turn-On Time	t_{ON}	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 2	+25°C		45	140	ns
			T_{MIN} to T_{MAX}			150	
Turn-Off Time	t_{OFF}	V+ = 2.7V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, Figure 2	+25°C		25	50	ns
			T_{MIN} to T_{MAX}			60	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Break-Before-Make (Note 7)	t_{BBM}	V+ = 2.7V, $V_{NO\_}$ or $V_{NC\_}$ = 1.5V; R_L = 50Ω, C_L = 35pF, Figure 3	+25°C		15		ns
			T_{MIN} to T_{MAX}	2			
Skew (Note 7)	t_{SKEW}	R_S = 39Ω, C_L = 50pF, Figure 4	+25°C		0.2	0.5	ns
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0, C_L = 1.0nF, Figure 5	+25°C		15		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C_L = 5pF, R_L = 50Ω	+25°C		320		MHz
Off-Isolation (Note 8)	V_{ISO}	C_L = 5pF, R_L = 50Ω, $V_{COM\_}$ = $1V_{P-P}$, f = 100kHz, Figure 6	+25°C		100		dB
Crosstalk (Note 9)	V_{CT}	C_L = 5pF, R_L = 50Ω, $V_{COM\_}$ = $1V_{P-P}$, f = 100kHz, Figure 6	+25°C		95		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $1V_{P-P}$, R_L = 600Ω	+25°C		0.03		%
NO_, NC_ Off-Capacitance	$C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$	$V_{NO\_}$, $V_{NC\_}$ = GND, f = 1MHz, Figure 7	+25°C		25		pF
COM_ On-Capacitance	$C_{COM(ON)}$	$V_{NO\_}$, $V_{NC\_}$ = GND, f = 1MHz, Figure 7	+25°C		54		pF
COM_ Off-Capacitance	$C_{COM(OFF)}$	$V_{COM\_}$ = GND, f = 1MHz (MAX4761), Figure 7	+25°C		25		pF
DIGITAL I/O (IN_, $\overline{EN}$)							
Input-Logic High	V_{IH}	V+ = 2.7V to 3.6V	T_{MIN} to T_{MAX}	1.4			V
		V+ = 3.6V to 5.25V	T_{MIN} to T_{MAX}	2.0			
Input-Logic Low	V_{IL}	V+ = 2.7V to 3.6V	T_{MIN} to T_{MAX}			0.5	V
		V+ = 3.6V to 5.25V	T_{MIN} to T_{MAX}			0.6	
Input Leakage Current	I_{IN}	V_{IN} = 0 or V+	T_{MIN} to T_{MAX}			1	µA
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Positive Supply Current	I+	V+ = 4.3V, $V_{IN\_}$ = 0V or V+	+25°C		0.01		µA
			T_{MIN} to T_{MAX}			1.0	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: UCSP packages are 100% tested at +25°C and limits across the full temperature range are guaranteed by correlation and design. Thin QFN packages are 100% tested at +85°C and limits across the full temperature range are guaranteed by correlation and design.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design, not production tested.

Note 8: Off-isolation = $20\log_{10}$ [$V_{COM\_}$ / ($V_{NO\_}$ or $V_{NC\_}$)], $V_{COM\_}$ = output, $V_{NO\_}$ or $V_{NC\_}$ = input to off switch.

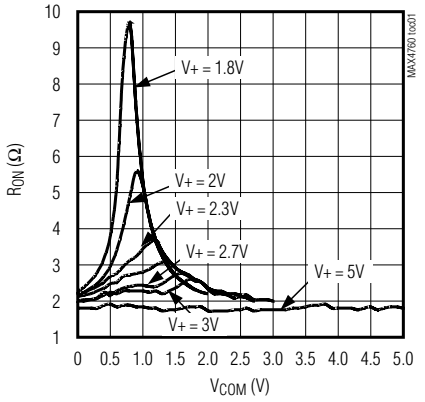
Note 9: Between any two switches.

High-Bandwidth, Quad DPDT Switches

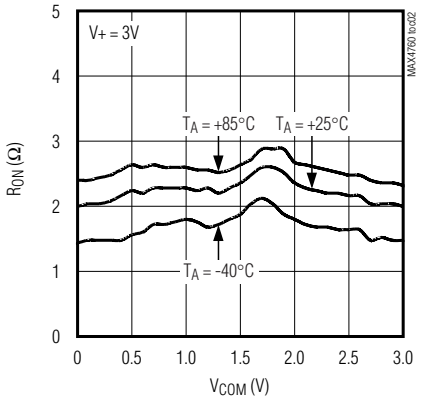
Typical Operating Characteristics

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

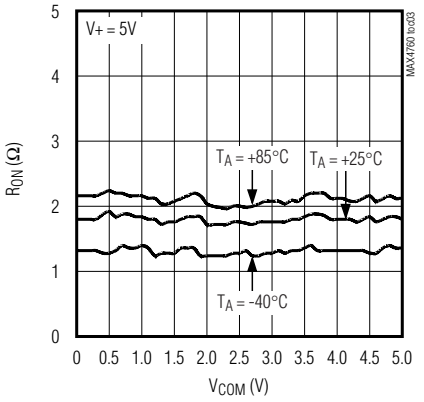
ON-RESISTANCE vs. V_{COM}



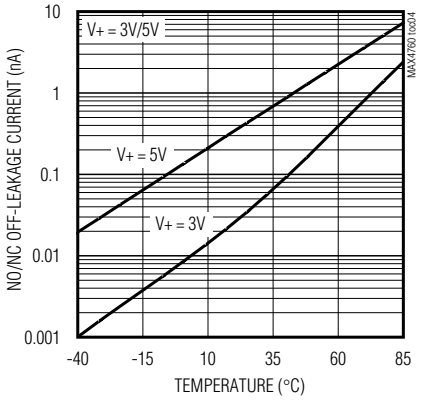
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



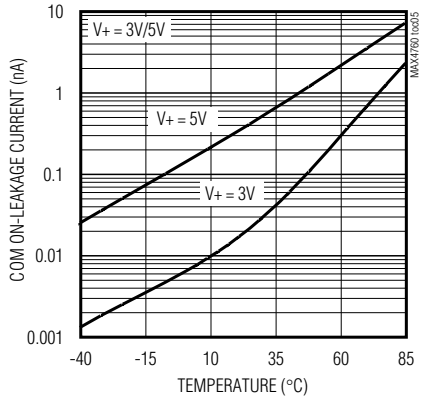
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



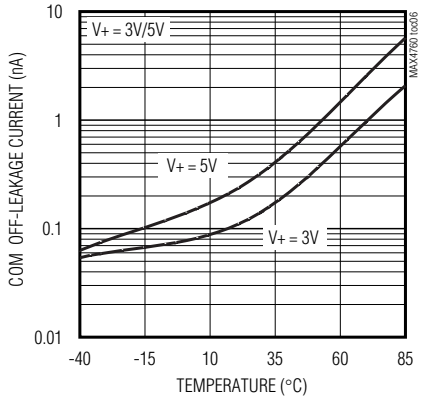
NO/NC OFF-LEAKAGE CURRENT vs. TEMPERATURE



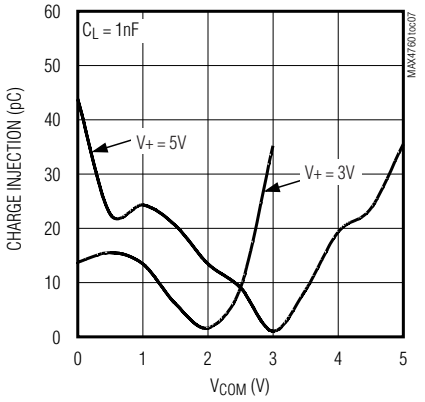
COM ON-LEAKAGE CURRENT vs. TEMPERATURE



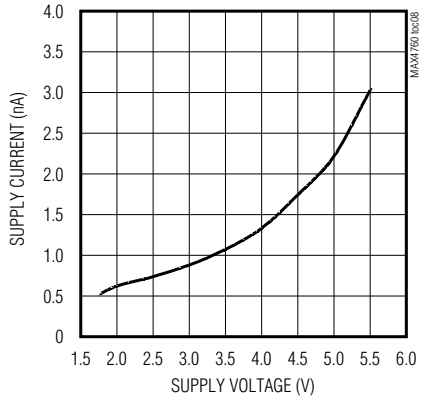
COM OFF-LEAKAGE CURRENT vs. TEMPERATURE



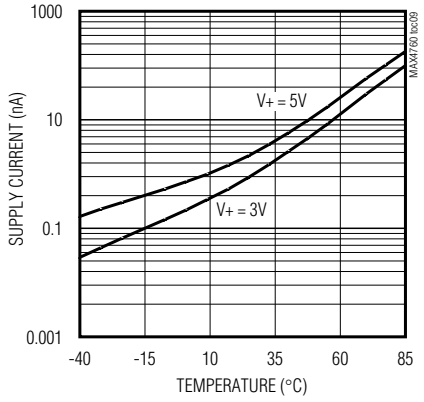
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. SUPPLY VOLTAGE



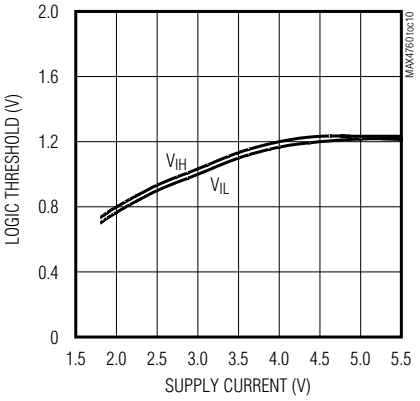
SUPPLY CURRENT vs. TEMPERATURE



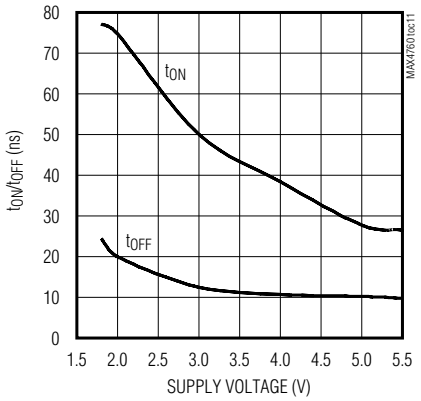
Typical Operating Characteristics (continued)

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

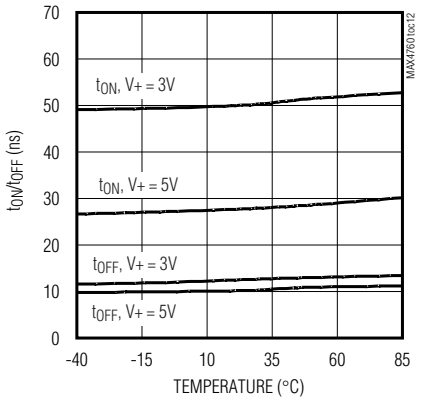
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



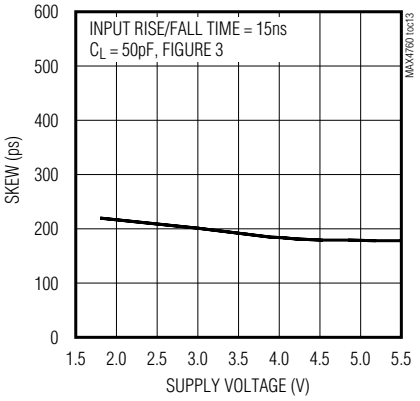
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



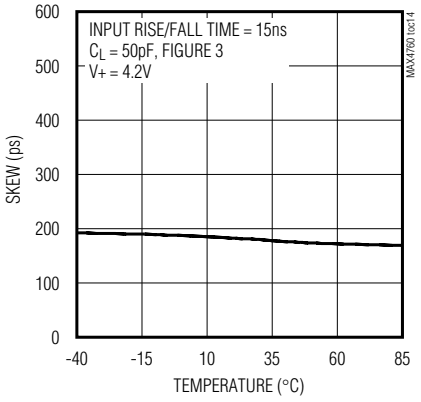
TURN-ON/OFF TIMES vs. TEMPERATURE



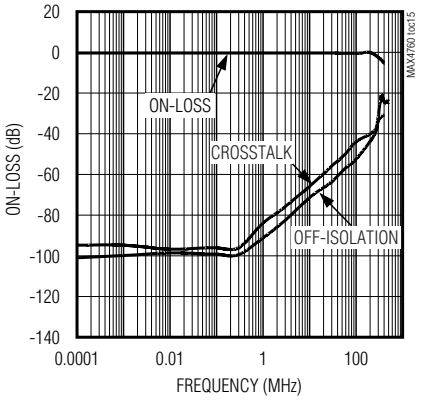
SKEW vs. SUPPLY VOLTAGE



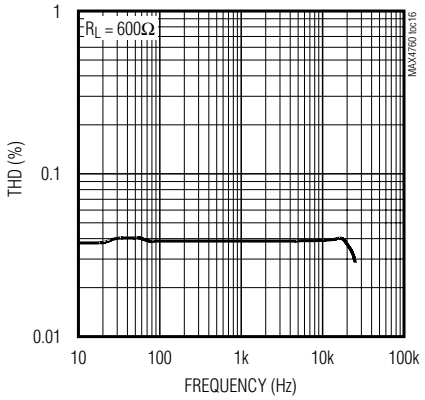
SKEW vs. TEMPERATURE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



High-Bandwidth, Quad DPDT Switches

Pin Description

PIN				NAME	FUNCTION
MAX4760		MAX4761			
THIN QFN	UCSP	THIN QFN	UCSP		
1	A1	1	A1	NC1	Analog Switch 1, Normally Closed Terminal 1
2	B2	2	B2	COM2	Analog Switch 2, Common Terminal 2
3	A2	3	A2	NC2	Analog Switch 2, Normally Closed Terminal 2
4	A3	4	A3	INA	Logic Control Digital Input for the MAX4760 Switch 1 and Switch 2. Digital control input for all MAX4761 switches.
5	C3, D4	5	C3, D4	V+	Positive Supply Voltage
6	A4	—	—	INB	Logic Control Digital Input for Switches 3 and 4
7	A5	7	A5	NC3	Analog Switch 3, Normally Closed Terminal 3
8	B5	8	B5	COM3	Analog Switch 3, Common Terminal 2
9	A6	9	A6	NC4	Analog Switch 4, Normally Closed Terminal 4
10	B6	10	B6	COM4	Analog Switch 4, Common Terminal 4
11, 14, 17, 29, 32, 35	—	6, 11, 14, 17, 24, 29, 32, 35	A4, F3	N.C.	No Connection. Not internally connected.
12	C5	12	C5	NO3	Analog Switch 3, Normally Open Terminal 3
13	C6	13	C6	NO4	Analog Switch 4, Normally Open Terminal 4
15	D6	15	D6	NO8	Analog Switch 8, Normally Open Terminal 8
16	D5	16	D5	NO7	Analog Switch 7, Normally Open Terminal 7
18	E6	18	E6	COM8	Analog Switch 8, Common Terminal 8
19	F6	19	F6	NC8	Analog Switch 8, Normally Closed Terminal 8
20	E5	20	E5	COM7	Analog Switch 7, Common Terminal 7
21	F5	21	F5	NC7	Analog Switch 7, Normally Closed Terminal 7
22	F4	—	—	IND	Logic Control Digital Input for Switches 7 and 8
23	C4, D3	23	C4, D3	GND	Ground
24	F3	—	—	INC	Logic Control Digital Input for Switches 5 and 6
25	F2	25	F2	NC6	Analog Switch 6, Normally Closed Terminal 2
26	E2	26	E2	COM6	Analog Switch 6, Common Terminal 6
27	F1	27	F1	NC5	Analog Switch 5, Normally Closed Terminal 5
28	E1	28	E1	COM5	Analog Switch 5, Common Terminal 5
30	D2	30	D2	NO6	Analog Switch 6, Normally Open Terminal 6
31	D1	31	D1	NO5	Analog Switch 5, Normally Open Terminal 5
33	C1	33	C1	NO1	Analog Switch 1, Normally Open Terminal 1
34	C2	34	C2	NO2	Analog Switch 2, Normally Open Terminal 1
36	B1	36	B1	COM1	Analog Switch 1, Common Terminal 1
—	—	22	F4	$\overline{EN}$	Output Enable, Active Low
EP	—	EP	—	EP	Exposed Pad, Connect to GND.

Detailed Description

The MAX4760 quad double-pole/double-throw (DPDT) and the MAX4761 octal single-pole/double-throw (SPDT) analog switches operate from a single +1.8V to +5.5V supply. These devices are fully specified for +3V applications.

The MAX4760/MAX4761 have a guaranteed 3.5Ω (max) on-resistance to switch data or audio signals. The low 25pF capacitance and 0.2ns change in skew makes them ideal for data switching applications. The MAX4760 has 4 logic inputs to control two switches in pairs and the MAX4761 has one logic control input and an enable input ($\overline{EN}$) to disable the switches.

Applications Information

Digital Control Inputs

The MAX4760/MAX4761 logic inputs accept up to +5.5V regardless of the supply voltage. For example, with a +3.3V supply, IN_ can be driven low to GND and high to +5.5V, which allows mixed logic levels in a system. Driving the control logic inputs rail-to-rail also minimizes power consumption. For a +3V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high).

For the MAX4761, drive $\overline{EN}$ low to enable. When $\overline{EN}$ is high, COM_ is high impedance.

Analog Signal Levels

Analog signal inputs over the full voltage range (0V to V+) are passed through the switch with minimal change in on-resistance (see the *Typical Operating Characteristics*). The switches are bidirectional so NO_, NC_, and COM_ can be either inputs or outputs.

Power-Supply Bypassing

Power-supply bypassing improves noise margin and prevents switching noise from propagating from the V+ supply to other components. A 0.1µF capacitor connected from V+ to GND is adequate for most applications.

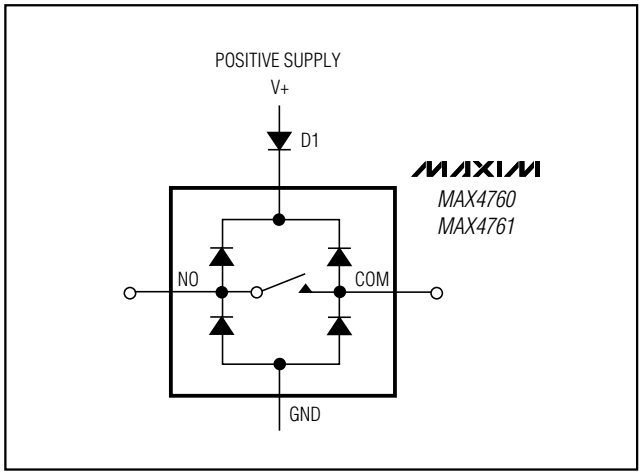


Figure 1. Overvoltage Protection Using an External Blocking Diode

Power-Supply Sequencing

CMOS devices require proper power-supply sequencing. Always apply V+ before the analog signals, especially if the input signal is not current limited. If sequencing is not possible, and the input signal is not current limited to less than 20mA, add a small-signal diode (Figure 1). Adding the diode reduces the analog range to a diode drop (0.7V) below V+ and increases the on-resistance slightly. The maximum supply voltage must not exceed +6V at any time.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to the Maxim website at www.maxim-ic.com/ucsp for the Application Note, “UCSP—A Wafer-Level Chip-Scale Package.”

High-Bandwidth, Quad DPDT Switches

Timing Circuits/Timing Diagrams

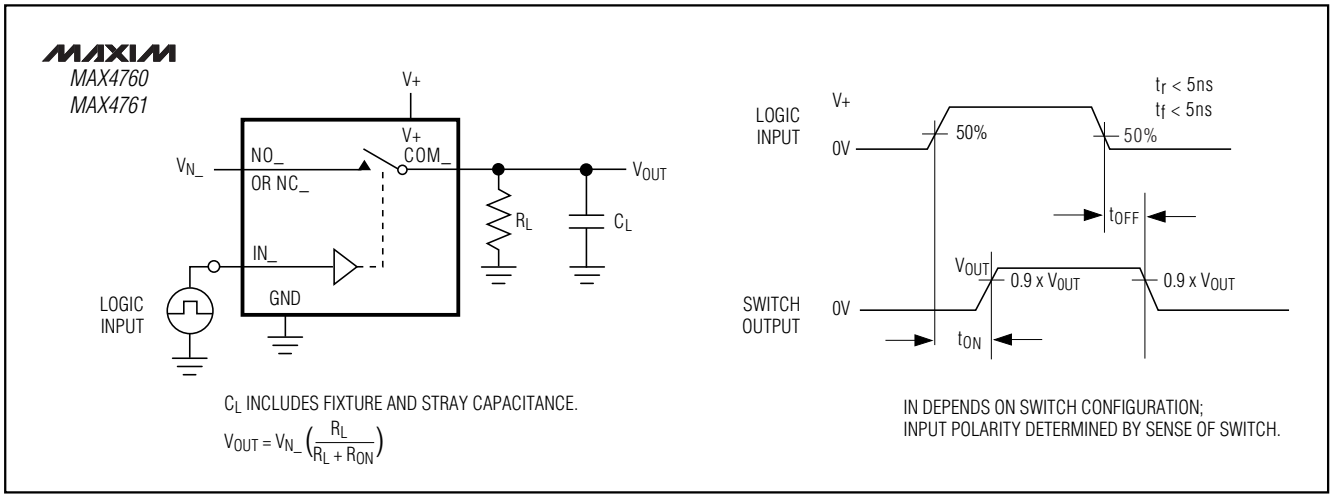


Figure 2. Switching Time

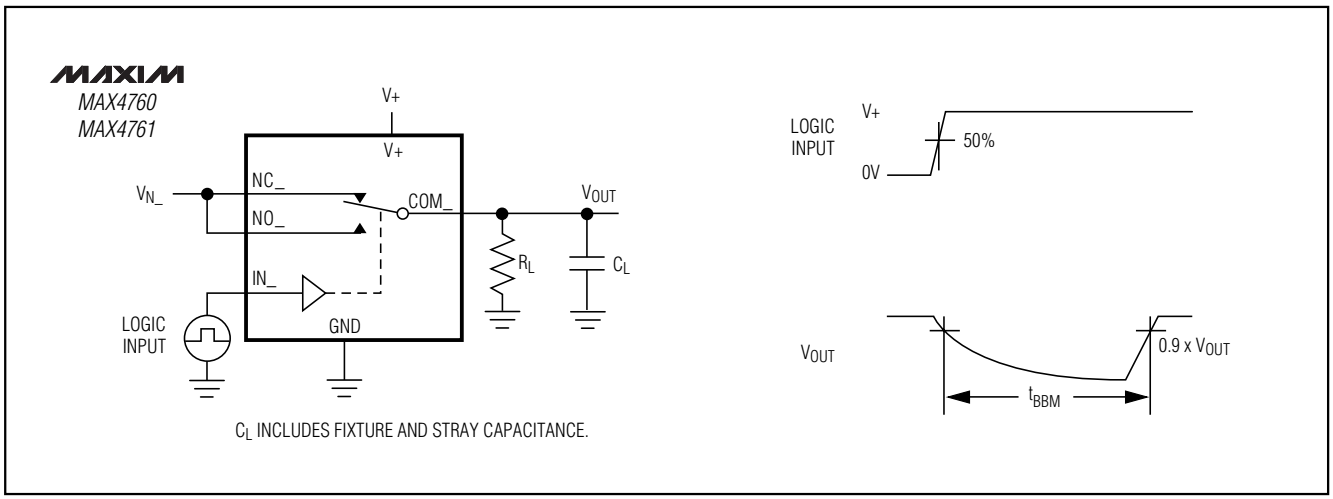
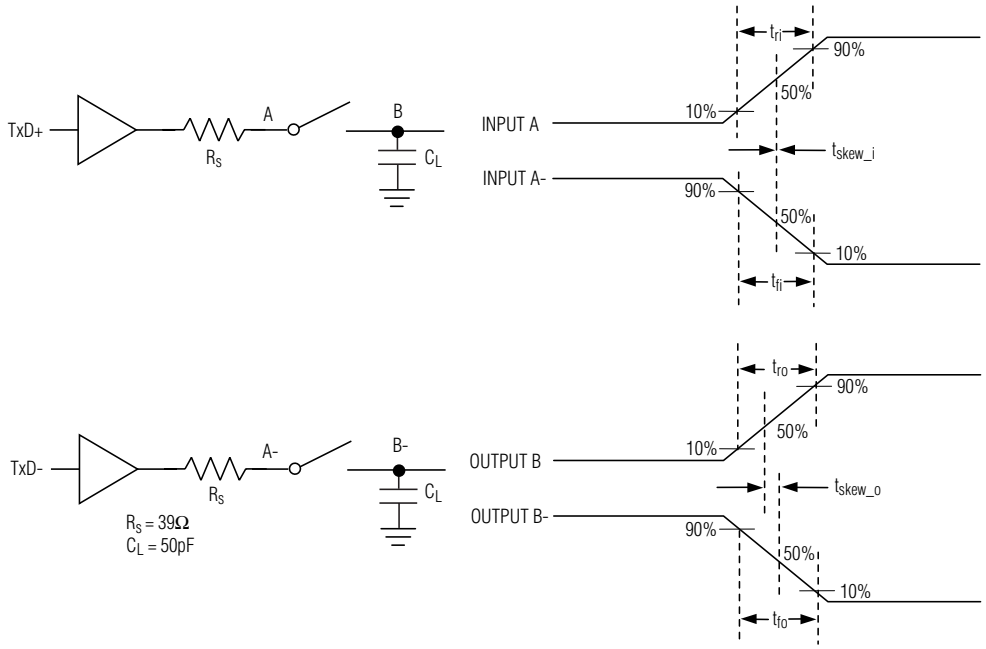


Figure 3. Break-Before-Make Interval

Timing Circuits/Timing Diagrams (continued)



$|t_{ro} - t_{ri}|$ DELAY DUE TO SWITCH FOR RISING INPUT AND RISING OUTPUT SIGNALS.

$|t_{fo} - t_{fi}|$ DELAY DUE TO SWITCH FOR FALLING INPUT AND FALLING OUTPUT SIGNALS.

$|t_{skew\_o}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR OUTPUT SIGNALS.

$|t_{skew\_i}|$ CHANGE IN SKEW THROUGH THE SWITCH FOR INPUT SIGNALS.

Figure 4. Input/Output Skew Timing Diagram

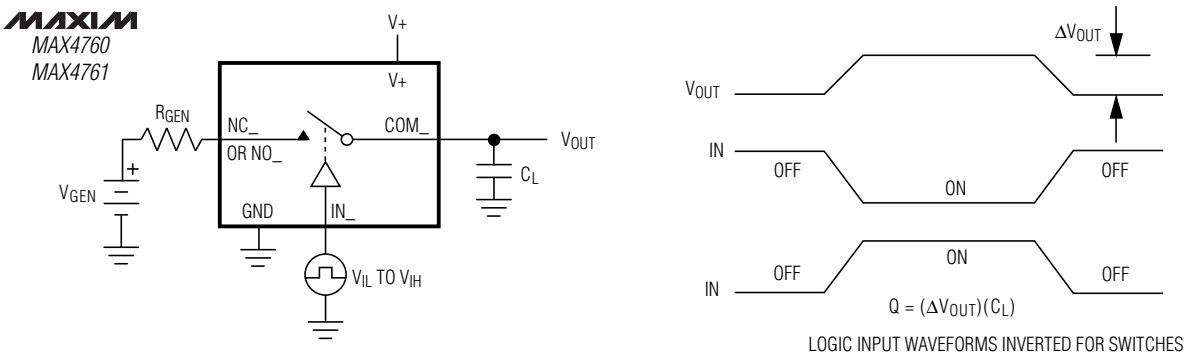


Figure 5. Charge Injection

High-Bandwidth, Quad DPDT Switches

Timing Circuits/Timing Diagrams (continued)

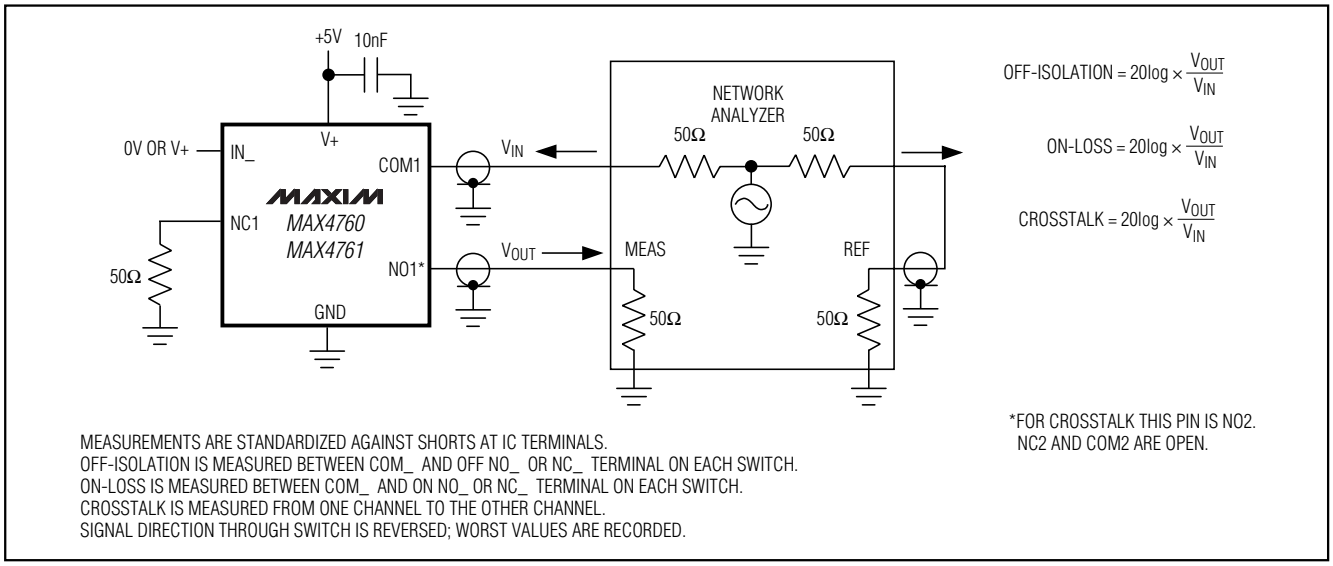


Figure 6. On-Loss, Off-Isolation, and Crosstalk

Typical Operating Circuit

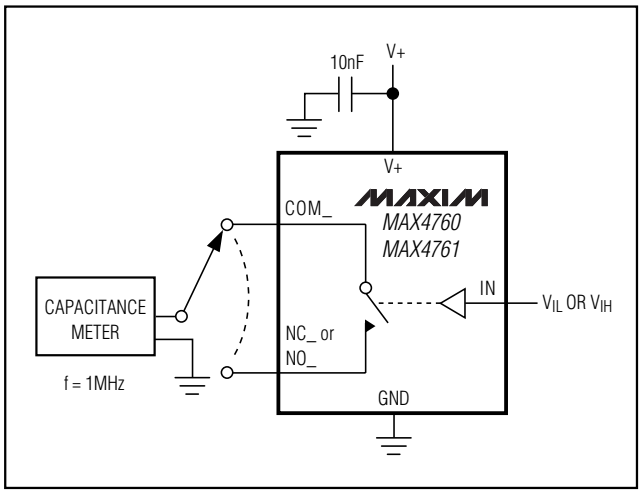
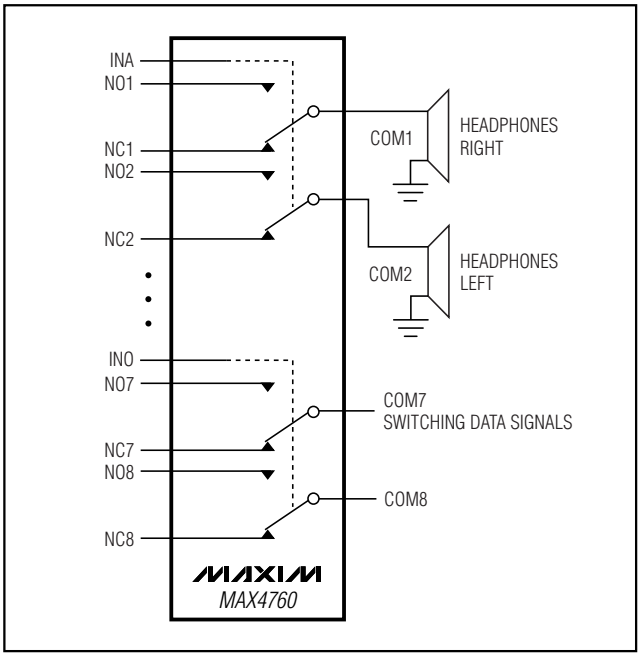


Figure 7. Channel On-/Off-Capacitance



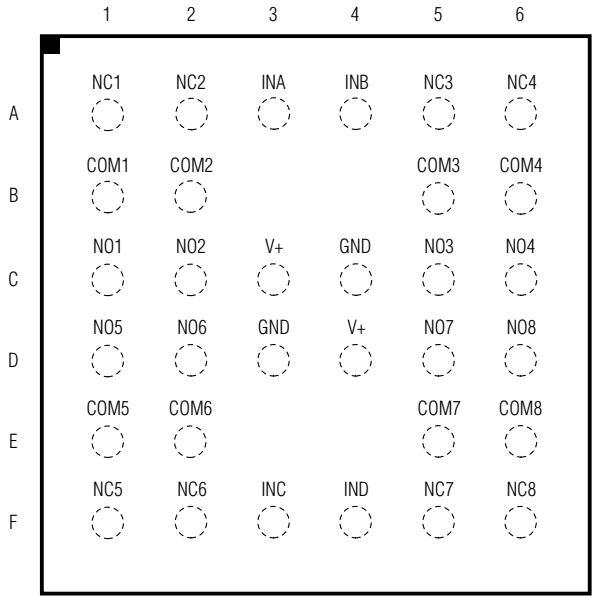
Pin Configurations/Truth Tables

TOP VIEW

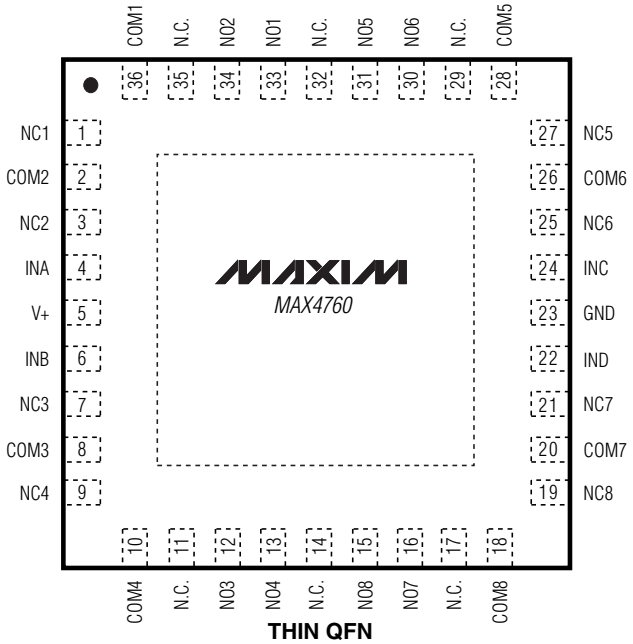
MAXIM

MAX4760

(BUMP SIDE DOWN)



UCSP



THIN QFN

NOTE: EXPOSED PADDLE CONNECTED TO GND OR FLOATING.

MAX4760

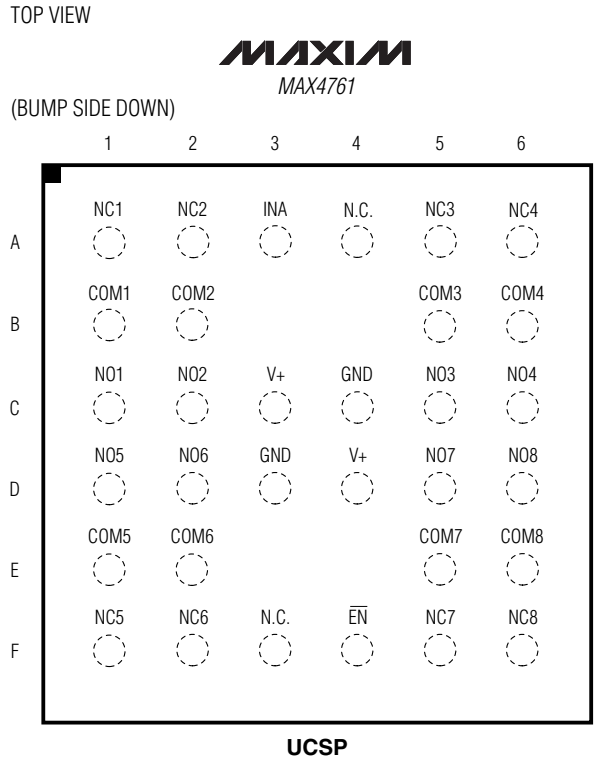
INA	NO1/NO2	NC1/NC2
LOW	OFF	ON
HIGH	ON	OFF
INB	**NO3/NO4**	**NC3/NC4**
LOW	OFF	ON
HIGH	ON	OFF
INC	**NO5/NO6**	**NC5/NC6**
LOW	OFF	ON
HIGH	ON	OFF
IND	**NO7/NO8**	**NC7/NC8**
LOW	OFF	ON
HIGH	ON	OFF

MAX4761

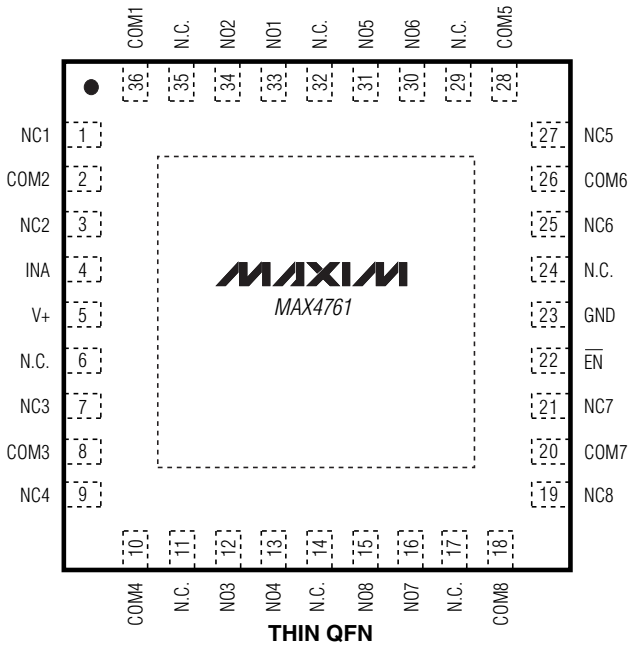
$\overline{EN}$	INA	NO_	NC_
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF
HIGH	X	OFF	OFF

High-Bandwidth, Quad DPDT Switches

Pin Configurations/Truth Tables (continued)



UCSP



THIN QFN

NOTE: EXPOSED PADDLE CONNECTED TO GND.

Chip Information

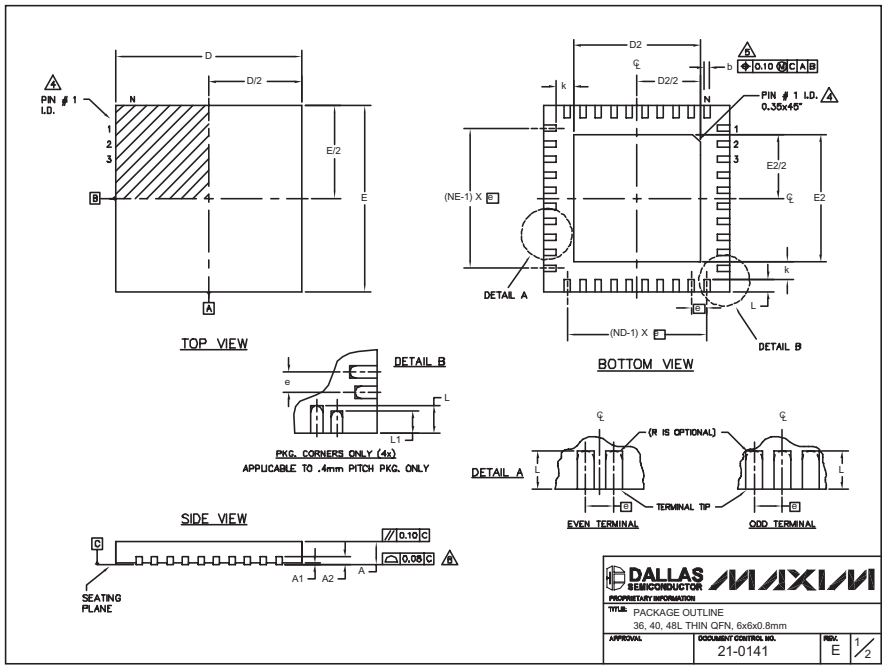
TRANSISTOR COUNT: 1432

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN 6x6x0.8.EPS



DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	E	1/2

COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2		0.20 REF.			0.20 REF.			0.20 REF.	
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e		0.50 BSC.			0.50 BSC.			0.40 BSC.	
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N		36			40			48	
ND		9			10			12	
NE		9			10			12	
JEDEC		WJJD-1			WJJD-2			–	

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	E	2/2

High-Bandwidth, Quad DPDT Switches

Package Information (continued)

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