CY29948

2.5V or 3.3V, 200-MHz, 1:12 Clock Distribution Buffer

Features

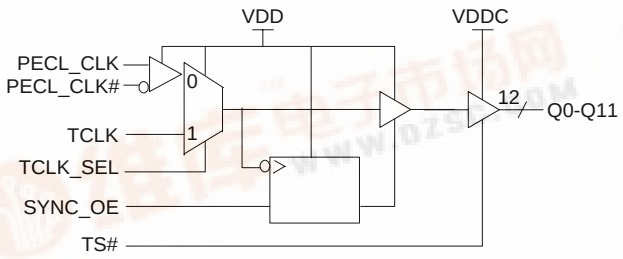
- **2.5V or 3.3V operation**
- **200-MHz clock support**
- **LVPECL or LVCMOS/LVTTL clock input**
- **LVCMOS-/LVTTL-compatible inputs**
- **12 clock outputs: drive up to 24 clock lines**
- **Synchronous Output Enable**
- **Output three-state control**
- **250 ps max. output-to-output skew**
- **Pin compatible with MPC948, MPC948L, MPC9448**
- **Available in Commercial and Industrial temp. range**
- **32-pin TQFP package**

Description

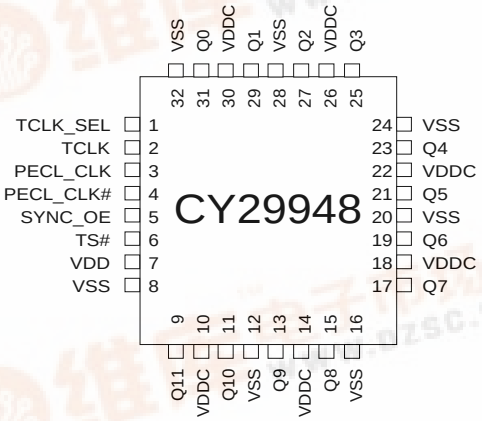
The CY29948 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The 12 outputs are LVCMOS or LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:24. The outputs can also be three-stated via the three-state input TS#. Low output-to-output skews make the CY29948 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

The CY29948 also provides a synchronous output enable input for enabling or disabling the output clocks. Since this input is internally synchronized to the input clock, potential output glitching or runt pulse generation is eliminated.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
3	PECL_CLK		I, PU	**PECL Input Clock**
4	PECL_CLK#		I, PD	**PECL Input Clock**
2	TCLK		I, PU	**External Reference/Test Clock Input**
9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31	Q(11:0)	VDDC	O	**Clock Outputs**
1	TCLK_SEL		I, PU	**Clock Select Input**. When LOW, PECL clock is selected and when HIGH TCLK is selected.
5	SYNC_OE		I, PU	**Output Enable Input**. When asserted HIGH, the outputs are enabled and when set LOW the outputs are disabled in a LOW state.
6	TS#		I, PU	**Three-state Control Input**. When asserted LOW, the output buffers are three-stated. When set HIGH, the output buffers are enabled.
10, 14, 18, 22, 26, 30	VDDC			**2.5V or 3.3V Power Supply for Output Clock Buffers**
7	VDD			**2.5V or 3.3V Power Supply**
8, 12, 16, 20, 24, 28, 32	VSS			**Common Ground**

Note:
1. PD = Internal Pull-Down, PU = Internal Pull- UP

Output Enable/Disable

The CY29948 features a control input to enable or disable the outputs. This data is latched on the falling edge of the input clock. When SYNC_OE is asserted LOW, the outputs are disabled in a LOW state. When SYNC_OE is set HIGH, the outputs are enabled as shown in *Figure 1*.

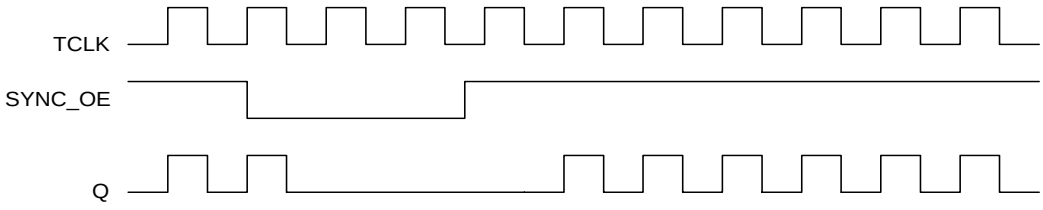


Figure 1. SYNC_OE Timing Diagram

Maximum Ratings [2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: ..... –65°C to + 150°C
Operating Temperature: ..... –40°C to +85°C
Maximum ESD protection ..... 2 kV
Maximum Power Supply: 5.5V
Maximum Input Current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters: $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, Over the specified temperature range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	V_{DD} = 3.3V, PECL_CLK single ended	1.49		1.825	V
		V_{DD} = 2.5V, PECL_CLK single ended	1.10		1.45	
		All other inputs	V_{SS}		0.8	
V_{IH}	Input High Voltage	V_{DD} = 3.3V, PECL_CLK single ended	2.135		2.42	V
		V_{DD} = 2.5V, PECL_CLK single ended	1.75		2.0	
		All other inputs	2.0		V_{DD}	
I_{IL}	Input Low Current[3]				–100	µA
I_{IH}	Input High Current[3]				100	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		300		1000	mV
V_{CMR}	Common Mode Range[4] PECL_CLK	V_{DD} = 3.3V	V_{DD} – 2.0		V_{DD} – 0.6	V
		V_{DD} = 2.5V	V_{DD} – 1.2		V_{DD} – 0.6	
V_{OL}	Output Low Voltage[5]	I_{OL} = 20 mA			0.4	V
V_{OH}	Output High Voltage[5]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5			V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8			
I_{DDQ}	Quiescent Supply Current			5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF		180		mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF		270		
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF		125		
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF		190		
Zout	Output Impedance	V_{DD} = 3.3V	12	15	18	Ω
		V_{DD} = 2.5V	14	18	22	
C_{in}	Input Capacitance			4		pF

Notes:
2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
5. Driving series or parallel terminated 50Ω (or 50Ω to V_{DD}/2) transmission lines.

AC Parameters[6]**:** $V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, Over the specified operating range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[7]	V_{DD} = 3.3V			200	MHz
		V_{DD} = 2.5V			170	
Tpd	PECL_CLK to Q Delay[7]	V_{DD} = 3.3V	4.0		8.0	ns
	TCLK to Q Delay[7]		4.4		8.9	
	PECL_CLK to Q Delay[7]	V_{DD} = 2.5V	6.0		10.0	
	TCLK to Q Delay[7]		6.4		10.9	
FoutDC	Output Duty Cycle[7, 8, 9]	Measured at $V_{DD}/2$	45		55	%
tpZL, tpZH	Output Enable Time (all outputs)		2		10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2		10	ns
Tskew	Output-to-Output Skew[7, 9]			150	250	ps
Tskew(pp)	Part-to-Part Skew[11]	PECL_CLK to Q			1.5	ns
		TCLK to Q			2.0	
Ts	Set-up Time[7, 10]	SYNC_OE to PECL_CLK	1.0			ns
		SYNC_OE to TCLK	0.0			
Th	Hold Time[7, 10]	PECL_CLK to SYNC_OE	0.0			ns
		TCLK to SYNC_OE	1.0			
Tr/Tf	Output Clocks Rise/Fall Time[9]	0.8V to 2.0V, V_{DD} = 3.3V	0.20		1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.20		1.3	

Notes:
6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. See *Figures 2 and 3*.
10. Setup and hold times are relative to the falling edge of the input clock
11. Part-to-Part skew at a given temperature and voltage.

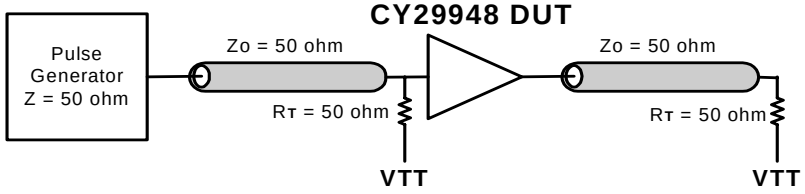


Figure 2. LVCMOS_CLK CY29948 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

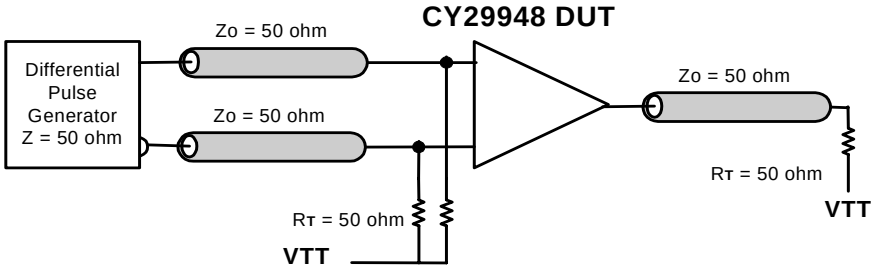


Figure 3. PECL_CLK CY29948 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

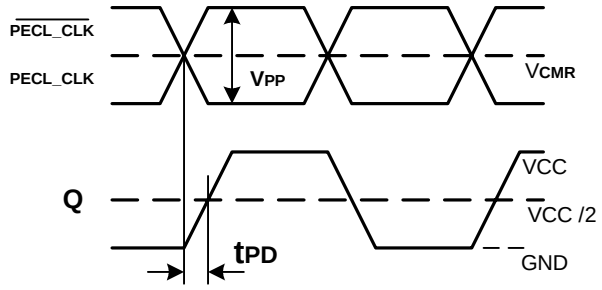


Figure 4. Propagation Delay (TPD) Test Reference

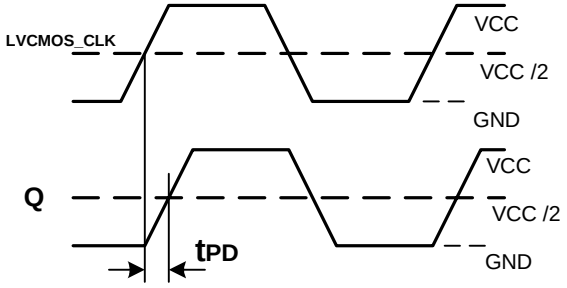


Figure 5. LVCMOS Propagation Delay (TPD) Test Reference

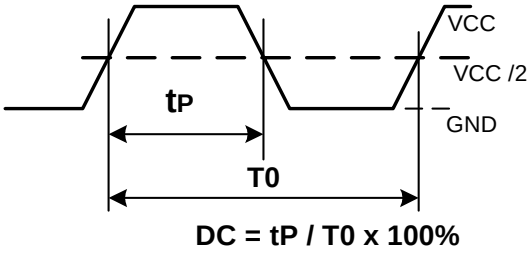


Figure 6. Output Duty Cycle (FoutDC)

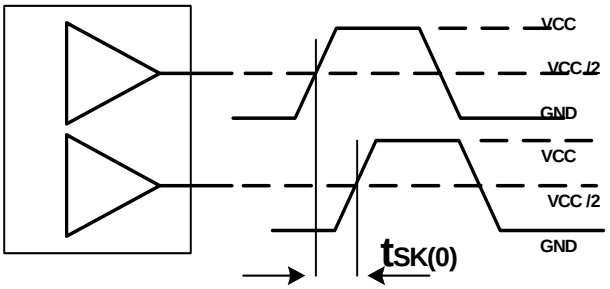


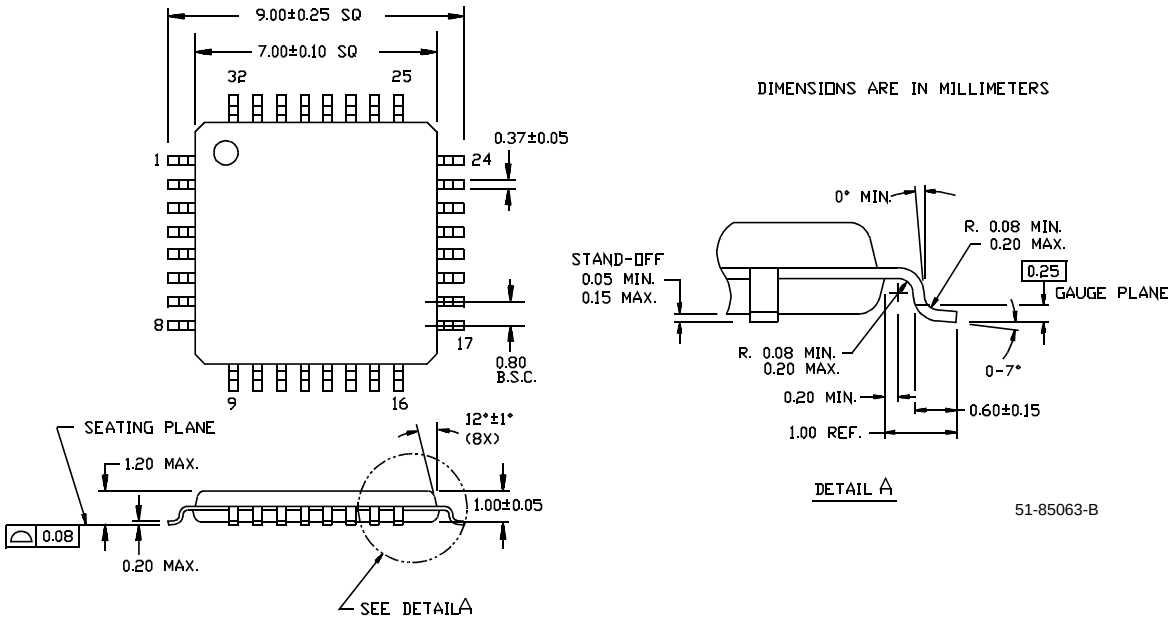
Figure 7. Output-to-Output Skew tsk(0)

Ordering Information

Part Number	Package Type	Production Flow
CY29948AI	32 Pin TQFP	Industrial, -40°C to +85°C
CY29948AIT	32 Pin TQFP - Tape and Reel	Industrial, -40°C to +85°C
CY29948AC	32 Pin TQFP	Commercial, 0°C to +70°C
CY29948ACT	32 Pin TQFP - Tape and Reel	Commercial, 0°C to +70°C

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32



Revision History

Document Title: CY29948 2.5V or 3.3V, 200-MHz, 1:12 Clock Distribution Buffer Document Number: 38-07288				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111099	02/13/02	BRK	New datasheet
*A	116782	08/14/02	HWT	Added Commercial Temperature Range
*B	122880	12/22/02	RBI	Added power up requirements to Maximum Ratings