

High Speed Operational Amplifier

FEATURES

- *Guaranteed* 1.0mV Max. Input Offset Voltage
- *Guaranteed* 100,000 Min. Gain
- *Guaranteed* 50V/ μ s Slew Rate
- *Guaranteed* 20nA Max. Input Offset Current
- 15MHz Bandwidth
- Unity Gain Stable

APPLICATIONS

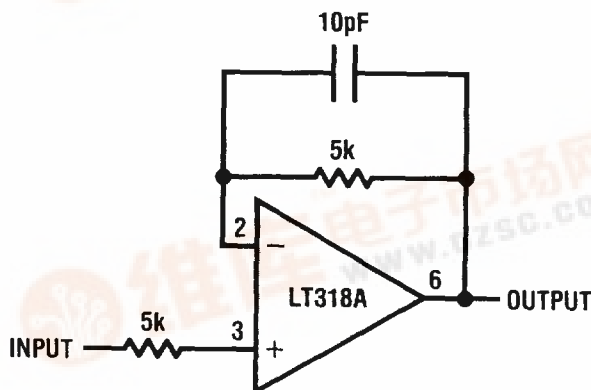
- Wideband Amplifiers
- High Frequency Absolute Value Circuits
- D/A Converter Amplifiers
- Fast Integrators

DESCRIPTION

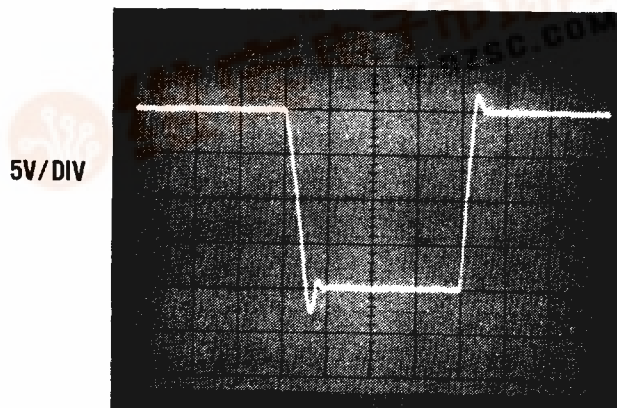
The LT118A is an improved version of the industry standard LM118. The LT118A features lower input offset voltage, lower input offset currents, higher gain and higher common mode and power supply rejection. Because of these enhancements, the LT118A will improve the accuracy of most applications. Unlike many wideband amplifiers, the LT118A is unity gain stable and has a slew rate of 50V/ μ s. When used in inverting amplifier applications, feedforward compensation can be used to achieve slew rates in excess of 150V/ μ s. Linear Technology Corporation's advanced processing techniques make the LT118A an ideal choice for high speed applications.

2

Voltage Follower



Voltage Follower Pulse Response



TIME $\rightarrow$ 0.5 μ s/DIV.

LT118A/LT318A
LM118/LM318

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Differential Input Current (Note 1)	±10mA
Input Voltage (Note 2)	±20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT118A/LM118	−55°C to 125°C
LT318A/LM318	0°C to 70°C
Storage Temperature Range	
All Devices	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW COMP 2 COMP 1 -IN +IN V-(CASE) METAL CAN H PACKAGE	ORDER PART NUMBER
	LT118AH LM118H LT318AH LM318H
TOP VIEW COMP 1 -IN +IN V- HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE	LT118AJ8 LM118J8 LT318AJ8 LM318J8 LT318AN8 LM318N8

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LT118A			LM118			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage		●		0.5 1	1 2	2	4 6		mV mV
I _{OS}	Input Offset Current		●		6 10	20 30	6	50 100		nA nA
I _B	Input Bias Current		●		120	250 500	120	250 500		nA nA
R _{IN}	Input Resistance			1	3		1	3		MΩ
A _V	Large Signal Voltage Gain	V _S = ±15V, V _{OUT} = ±10V, R _L ≥ 2kΩ	●	100 100	500		50 25	200		V/mV V/mV
SR	Slew Rate	V _S = ±15V, A _V = 1		50	70		50	70		V/μs
GBW	Gain Bandwidth Product	V _S = ±15V			15			15		MHz
	Output Voltage Swing	V _S = ±15V, R _L = 2kΩ	●	±12	±13		±12	±13		V
	Input Voltage Range	V _S = ±15V	●	±11.5			±11.5			V
I _S	Supply Current	T _A = 125°C			5 4.5	8 7		5 4.5	8 7	mA mA
CMRR	Common Mode Rejection Ratio		●	86	100		80	100		dB
PSRR	Power Supply Rejection Ratio		●	86	100		70	80		dB

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LT318A			LM318			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●		0.5	1 2		4	10 15	mV mV
I_{OS}	Input Offset Current		●		10	20 30		30	200 750	nA nA
I_B	Input Bias Current		●		150	250 500		150	500 750	nA nA
R_{IN}	Input Resistance			0.5	3		0.5	3		MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100 100	500		25 20	200		V/mV V/mV
SR	Slew Rate	$V_S = \pm 15V$, $A_V = 1$		50	70		50	70		V/ μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$			15			15		MHz
	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$	●	± 12	± 13		± 12	± 13		V
	Input Voltage Range	$V_S = \pm 15V$	●	± 11.5			± 11.5			V
I_S	Supply Current				5	10		5	10	mA
CMRR	Common Mode Rejection Ratio		●	86	100		70	100		dB
PSRR	Power Supply Rejection Ratio		●	86	100		65	80		dB

The ● denotes those specifications which apply over the full operating temperature range.

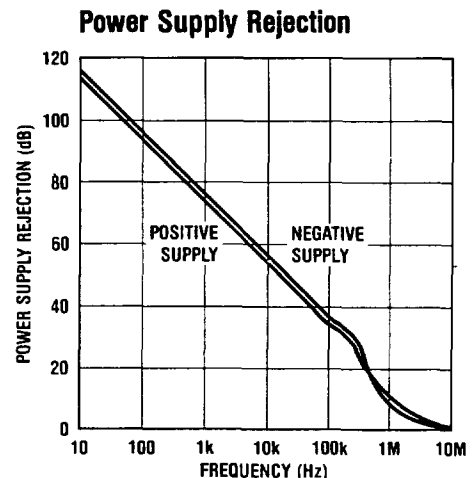
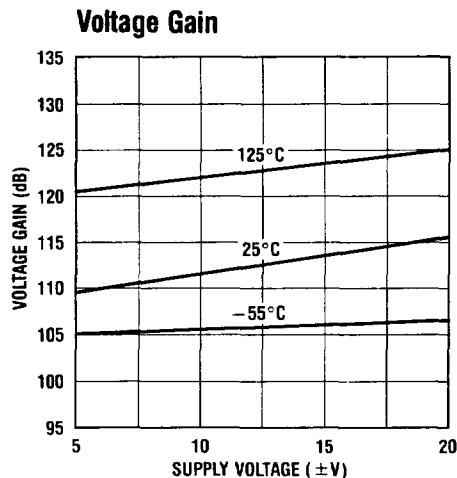
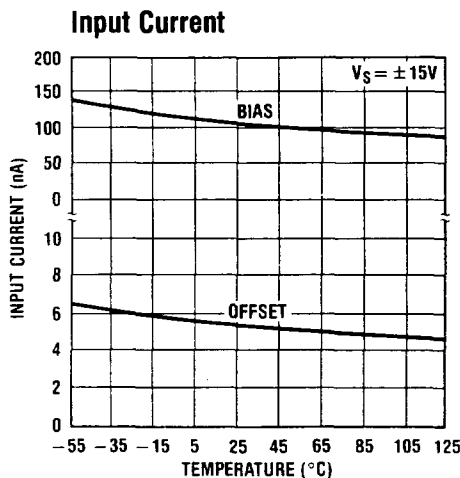
The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$. The power supplies must be bypassed with a $0.1\mu F$ or greater disc capacitor within 4 inches of the device.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

Figure 10 is a graph showing Output Swing ($\pm V$) versus Frequency (Hz). The y-axis ranges from 0 to 14 V, and the x-axis ranges from 0.5M to 50M Hz. The output swing is constant at approximately 12.5V up to 1M Hz, then decreases sharply, reaching near 0V at 20M Hz. The conditions are $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{V}$.

Figure 1 is a graph showing the frequency response of the amplifier. The x-axis represents Frequency (Hz) on a logarithmic scale from 10 to 100M. The left y-axis represents Voltage Gain (dB) from -20 to 120. The right y-axis represents Phase from 0 to 2. Two curves are plotted: GAIN and PHASE. The GAIN curve starts at approximately 110 dB at 10 Hz, remains flat until about 100 Hz, then decreases with a slope of -20 dB/decade, reaching about -10 dB at 100M Hz. The PHASE curve starts at 0 at 10 Hz, remains flat until about 100 Hz, then rises to a peak of about 1.5 at 300 kHz, dips to about 0.8 at 1 MHz, and rises again to about 1.8 at 10M Hz. Test conditions are noted as $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{V}$.

The graph shows the unity gain bandwidth of the 741C op-amp as a function of temperature. The y-axis represents the unity gain bandwidth in MHz, ranging from 0 to 24. The x-axis represents the temperature in degrees Celsius, ranging from -55 to 125. Two lines are plotted, corresponding to different supply voltages: $V_S = \pm 15V$ and $V_S = \pm 10V$. Both lines show a linear decrease in bandwidth as temperature increases.

Temperature (°C)	Unity Gain Bandwidth (MHz) at $V_S = \pm 15V$	Unity Gain Bandwidth (MHz) at $V_S = \pm 10V$
-55	20.5	19.5
-35	19.5	18.5
-15	18.5	17.5
5	17.5	16.5
25	16.5	15.5
45	15.5	14.5
65	14.5	13.5
85	13.5	12.5
105	12.5	11.5
125	11.5	10.5

A graph showing the output swing (in $\pm V$) versus frequency (in Hz) for the FEEDFORWARD circuit. The y-axis ranges from 0 to 14 in increments of 2. The x-axis is logarithmic, ranging from 1M to 100M Hz, with major ticks at 1M, 3M, 10M, 30M, and 100M. The curve starts at approximately 12.5V for frequencies up to 2M Hz, then drops sharply, reaching about 2V at 10M Hz and 0.2V at 30M Hz. The graph is labeled "FEEDFORWARD" in the lower right quadrant. Test conditions are noted as $T_A = 25^\circ C$ and $V_S = \pm 15V$.

Frequency (Hz)	Output Swing ($\pm V$)
1M	12.5
2M	12.5
3M	12.0
5M	8.0
10M	2.0
20M	0.5
30M	0.2
100M	0.1

Figure 1 is a graph showing the frequency response of the feedforward circuit. The Y-axis represents Voltage Gain (dB), ranging from -20 to 120. The X-axis represents Frequency (Hz), ranging from 10 to 100M (100 MHz). The graph displays two curves: GAIN and PHASE. The GAIN curve starts at approximately 110 dB at 10 Hz and decreases steadily, reaching about -10 dB at 100 MHz. The PHASE curve starts at 40 dB at 10 Hz, remains relatively flat until 100 kHz, then rises to about 60 dB at 100 MHz. The operating conditions are $V_S = \pm 15V$ and $T_A = 25^\circ C$.

$V_S = \pm 15V$
 $R_S = R_T = 10k\Omega$
 $C_T = 5pF$

Temperature (°C)	Positive Slew Rate (V/μs)	Negative Slew Rate (V/μs)
-55	105	82
-35	106	82
-15	107	82
5	107	82
25	106	80
45	104	78
65	101	75
85	98	72
105	95	69
125	93	69

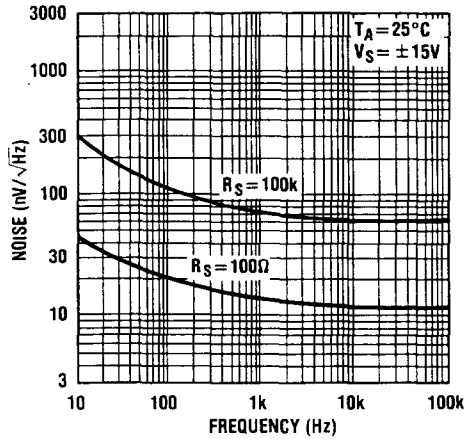
5V/DIV

0 0.4 0.8 1.6 2.0 2.4

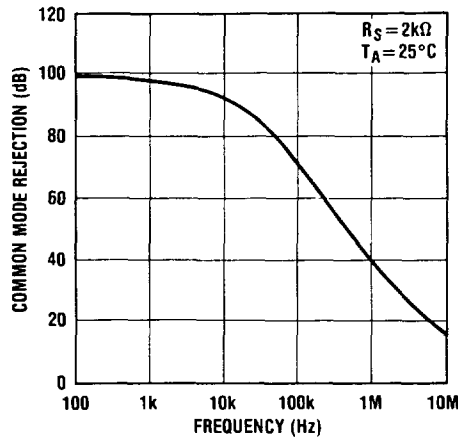
TIME—0.2 μ s/DIV

TYPICAL PERFORMANCE CHARACTERISTICS

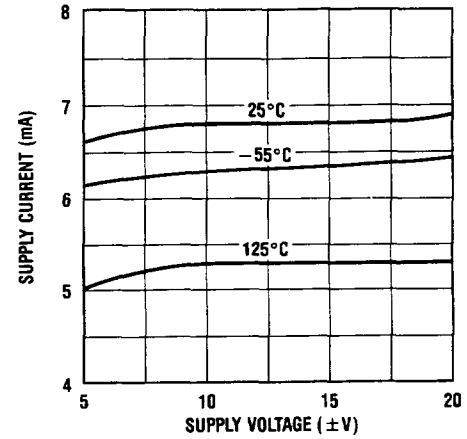
Input Noise Voltage



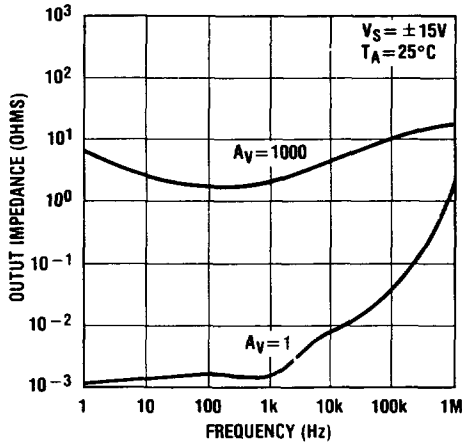
Common Mode Rejection



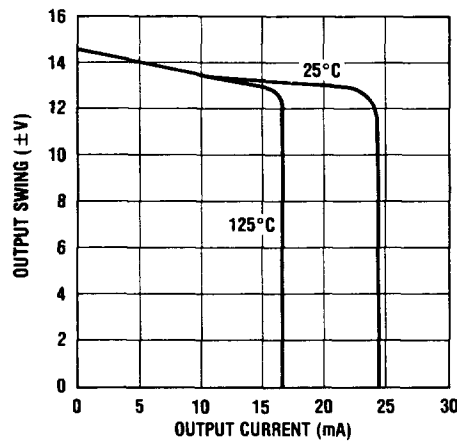
Supply Current



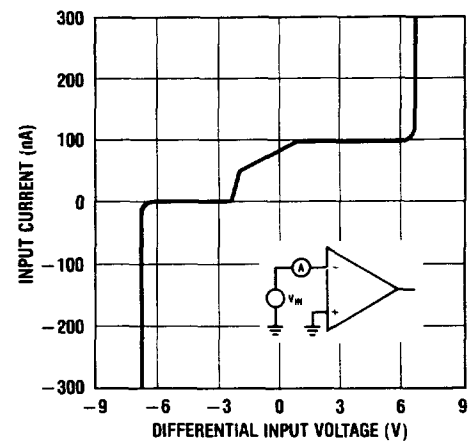
Closed Loop Output Impedance



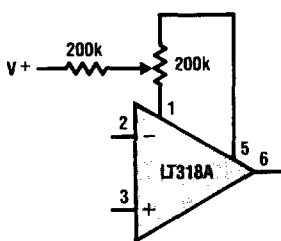
Current Limiting



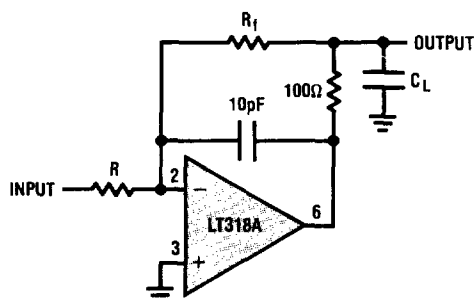
LT118A Input Current



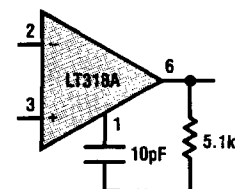
Offset Balancing



Isolating Large Capacitive Loads

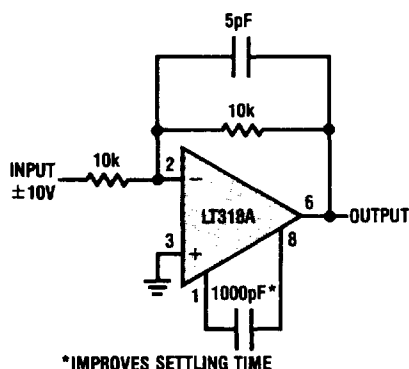


Overcompensation for Increased Stability

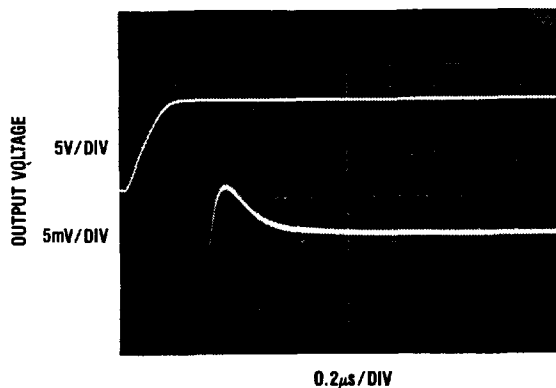


SETTLING TIME CIRCUITS

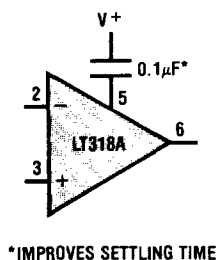
Settling Time Test Circuit



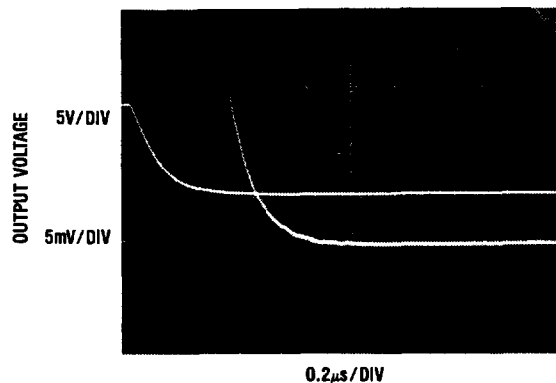
Settling Time



Alternate Compensation for Improved Settling Time



Settling Time



APPLICATIONS INFORMATION

Because of their wider bandwidth, the LT118A and LM118 operational amplifiers require more application care than most general purpose low frequency amplifiers. One of the most critical requirements is that power supplies should be bypassed with a 0.1 μF (or larger) disc ceramic capacitor within an inch of the device. Also, stray capacitance at either the input or output can cause oscillation. While input capacitance can be compensated by placing a capacitor across the feedback resistor, load capacitance must be minimized or isolated as shown. Even the 50pF input capacitance of a 1X scope probe can alter the response of the device.

Settling time, an important parameter in many high speed amplifier applications, is difficult to measure and optimize. Settling time is very "application dependent" and is influenced by external components, layout and the amplifier. In general, the settling time to 0.01% can be minimized by using a circuit similar to that shown. In addition to the compensation network shown, a capacitor is needed across the feedback resistor to minimize ringing.

Power supply bypassing can also affect settling time. The amplifier has low power supply rejection ratio at high frequencies, so transients and ringing on the supply leads can appear at the output. Large (22 μF) solid tantalum capacitors are preferred to minimize supply aberrations.

The circuit diagram shows a precision active filter. The input signal is applied to a resistor network consisting of a 10k resistor in series with a 10k resistor in parallel with a 10k resistor. This network is connected to the non-inverting input (pin 2) of the first LT1008 comparator. The inverting input (pin 7) of the first LT1008 is connected to a 1N4148 diode in series with a 300pF capacitor, which is then connected to the non-inverting input (pin 2) of the second LT1008 comparator. The inverting input (pin 7) of the second LT1008 is connected to the output of the first LT1008. The output of the second LT1008 is connected to the non-inverting input (pin 3) of the LT318A op-amp. The inverting input (pin 2) of the LT318A is connected to a 10k resistor in parallel with a 1000pF capacitor, which is then connected to the output of the LT318A. The LT318A op-amp is configured as a voltage follower with its output (pin 6) connected to its inverting input (pin 2). The LT318A is powered by a +15V supply (pin 7) and a -15V supply (pin 4). The LT1008 comparators are also powered by a +15V supply (pin 7) and a -15V supply (pin 4). The output of the LT318A is labeled 'OUTPUT'.

***1% METAL FILM**

FULL POWER BANDWIDTH = 2MHz
SLEW RATE = 50V/ μ sec
SETTLING (10V STEP) = 12 μ s TO 0.01%
BIAS CURRENT DC = 30pA
OFFSET DRIFT = 0.3 μ V/ $^{\circ}$ C
OFFSET VOLTAGE = 30 μ V

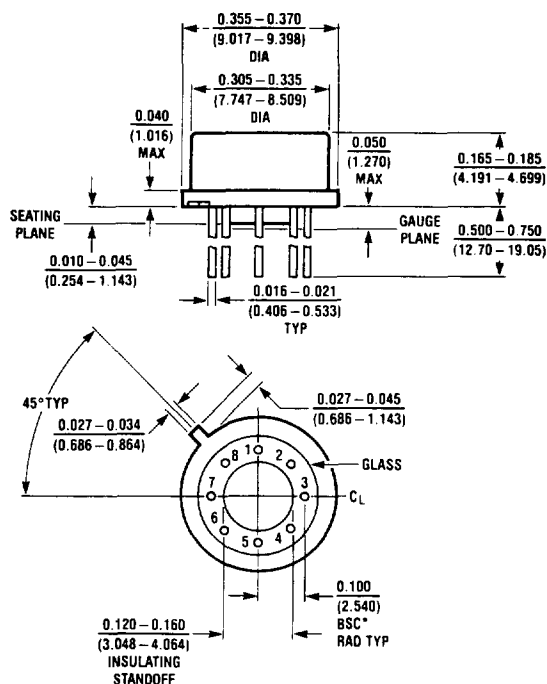
IC DIAGRAM

The diagram is a detailed schematic of an integrated circuit, showing a complex arrangement of transistors, resistors, and capacitors. The circuit is organized into several functional blocks. On the left, there is a multi-stage amplifier or filter section involving transistors Q1, Q2, Q3, Q4, Q5, and Q6, with resistors R1, R2, R3, R4, R5 and capacitors C1, C2. A diode is also present in this section. The central part of the diagram features a large block with transistors Q7 through Q18, including a feedback loop with a 1pF capacitor and a 260 ohm resistor. The right side contains another multi-stage section with transistors Q19 through Q34, resistors R19 through R35, and capacitors C3, C4. The diagram is bounded by a grid with pins labeled 1 through 8 on the top and bottom edges. The overall layout is typical of a high-speed analog or mixed-signal IC design.

LT118A/LT318A LM118/LM318

PACKAGE DESCRIPTION

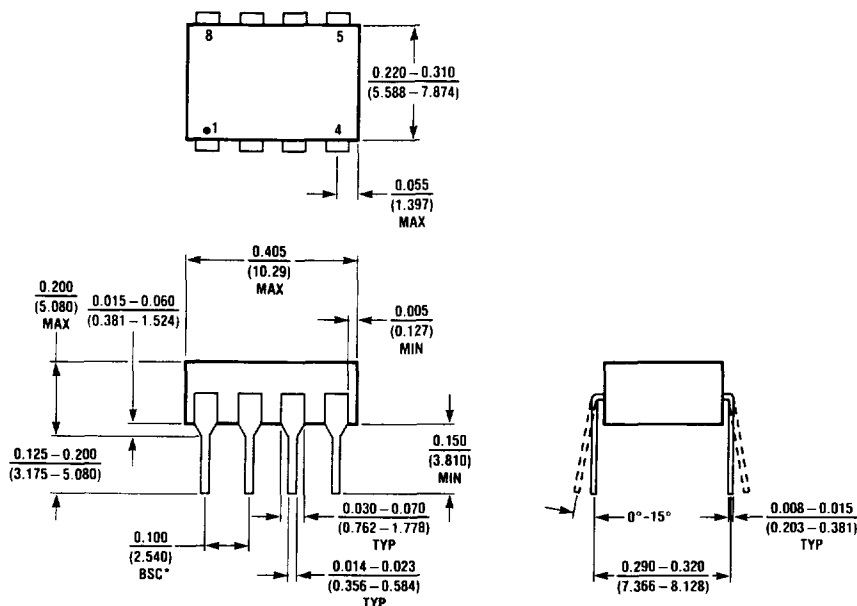
**H Package
Metal Can**



NOTE: DIMENSIONS IN INCHES

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

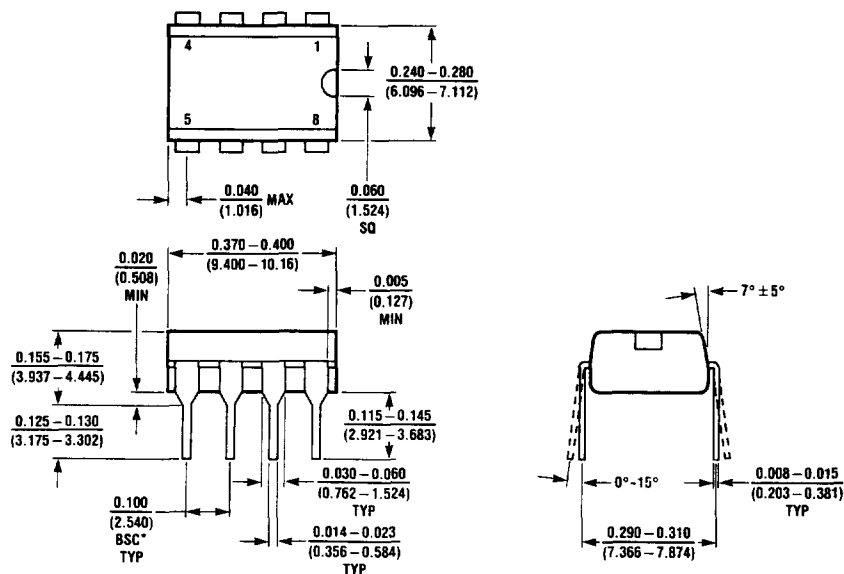
**J8 Package
8 Lead Hermetic DIP**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
 *LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
 *LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
100°C	130°C/W