TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC55VEM208ASTN is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz (typ) and a minimum cycle time of 40 ns. It is automatically placed in low-power mode at 0.7 µA standby current (typ) when chip enable ($\overline{CE}$) is asserted high. There are two control inputs. $\overline{CE}$ is used to select the device and for data retention control, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55VEM208ASTN is available in a plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
  Operating: 9 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6 V
- Power down features using $\overline{CE}$
- Data retention supply voltage of 1.5 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of –40° to 85°C
- Standby Current (maximum):

3.6 V	10 µA
3.0 V	5 µA

- Access Times:

	TC55VEM208ASTN	
	40	55
Access Time	40 ns	55 ns
$\overline{CE}$ Access Time	40 ns	55 ns
$\overline{OE}$ Access Time	25 ns	30 ns

- Package:
  TSOP I 32-P-0.50 (Weight:0.22 g typ)

PIN ASSIGNMENT (TOP VIEW)

32 PIN TSOP

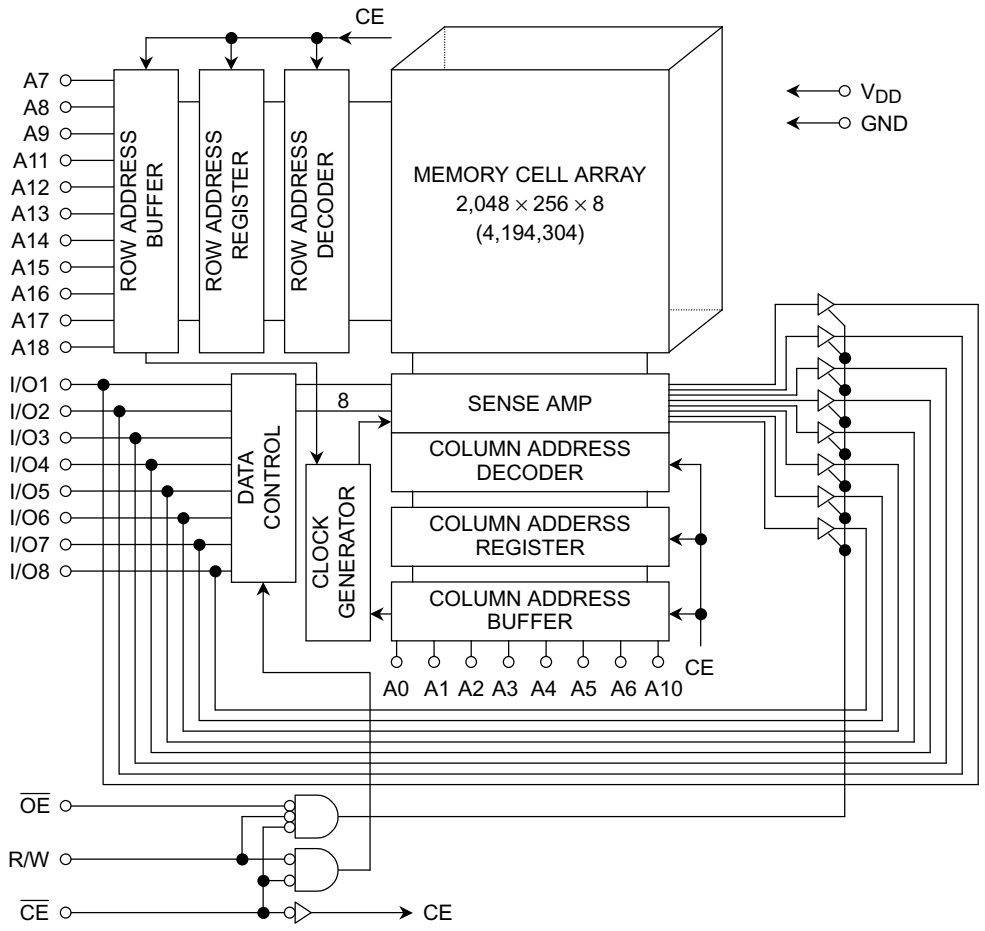
(Normal)

PIN NAMES

A0~A18	Address Inputs
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1~I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A11	A9	A8	A13	R/W	A17	A15	V_{DD}	A18	A16	A14	A12	A7	A6	A5	A4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A3	A2	A1	A0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A10	$\overline{OE}$

BLOCK DIAGRAM



OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

* = don't care
H = logic high
L = logic low

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	−0.3~4.2	V
V_{IN}	Input Voltage	−0.3*~4.2	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	0.6	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

*: −2.0 V when measured at a pulse width of 20ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = –40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage		2.3	—	3.6	V
V_{IH}	Input High Voltage	V_{DD} = 2.3 V~2.7 V	2.0	—	V_{DD} + 0.3	V
		V_{DD} = 2.7 V~3.6 V	2.2			
V_{IL}	Input Low Voltage		–0.3*	—	$V_{DD} \times 0.24$	V
V_{DH}	Data Retention Supply Voltage		1.5	—	3.6	V

*: –2.0 V when measured at a pulse width of 20ns

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 2.3 to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V~V_{DD}				—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = V_{DD}$ – 0.5 V				–0.5	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V				2.1	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 V~V_{DD}				—	—	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} and R/W = V_{IH}, I_{OUT} = 0 mA, Other Input = V_{IH}/V_{IL}	t_{cycle}	MIN		—	—	35	mA
				1 μs		—	—	8	
I_{DDO2}		$\overline{CE}$ = 0.2 V and R/W = V_{DD} – 0.2 V, I_{OUT} = 0 mA, Other Input = V_{DD} – 0.2 V/0.2 V		MIN		—	—	30	mA
				1 μs		—	—	3	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}				—	—	1	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} – 0.2 V	V_{DD} = 3.3V± 0.3 V	Ta = –40~85°C		—	—	10	μA
			V_{DD} =3.0 V	Ta = 25°C		—	0.7	—	
				Ta = –40~40°C		—	—	2	
				Ta = –40~85°C		—	—	5	

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.7 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55VEM208ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	40	—	55	—	ns
t_{ACC}	Address Access Time	—	40	—	55	
t_{CO}	Chip Enable Access Time	—	40	—	55	
t_{OE}	Output Enable Access Time	—	25	—	30	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{OD}	Chip Enable High to Output High-Z	—	20	—	25	
t_{ODO}	Output Enable High to Output High-Z	—	20	—	25	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55VEM208ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	40	—	55	—	ns
t_{WP}	Write Pulse Width	30	—	40	—	
t_{CW}	Chip Enable to End of Write	35	—	45	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	20	—	25	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	20	—	25	—	
t_{DH}	Data Hold Time	0	—	0	—	

Note: t_{OD}, t_{ODO} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = –40° to 85°C, V_{DD} = 2.3 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55VEM208ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{ACC}	Address Access Time	—	55	—	70	
t_{CO}	Chip Enable Access Time	—	55	—	70	
t_{OE}	Output Enable Access Time	—	30	—	35	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{OD}	Chip Enable High to Output High-Z	—	25	—	30	
t_{ODO}	Output Enable High to Output High-Z	—	25	—	30	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55VEM208ASTN				UNIT
		40		55		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	
t_{CW}	Chip Enable to End of Write	45	—	55	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	25	—	30	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	25	—	30	—	
t_{DH}	Data Hold Time	0	—	0	—	

Note: t_{OD}, t_{ODO} and t_{ODW} are specified in time when an output becomes high impedance, and are not judged depending on an output voltage level.

AC TEST CONDITIONS

PARAMETER	TEST CONDITION
Input pulse level	0.2 V, $V_{DD} \times 0.7$ V + 0.2 V
t_R, t_F	1V / ns(Fig.1)
Timing measurements	$V_{DD} \times 0.5$
Reference level	$V_{DD} \times 0.5$
Output load	30 pF + 1 TTL Gate(Fig.2)

Fig.1 : Input rise and fall time

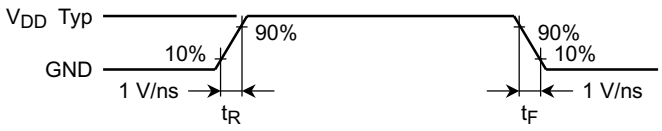
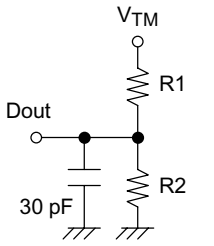


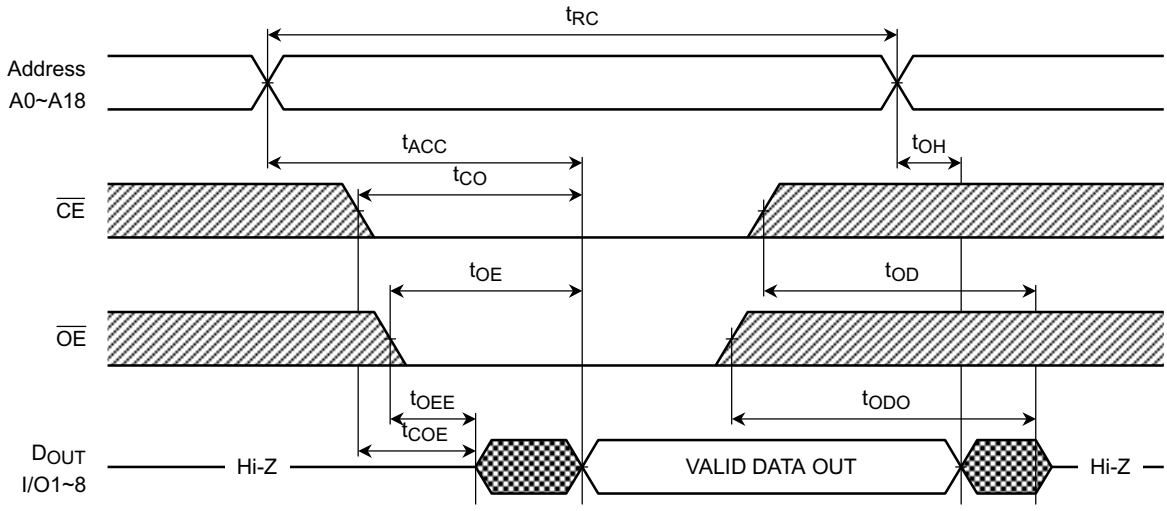
Fig.2 : Output load



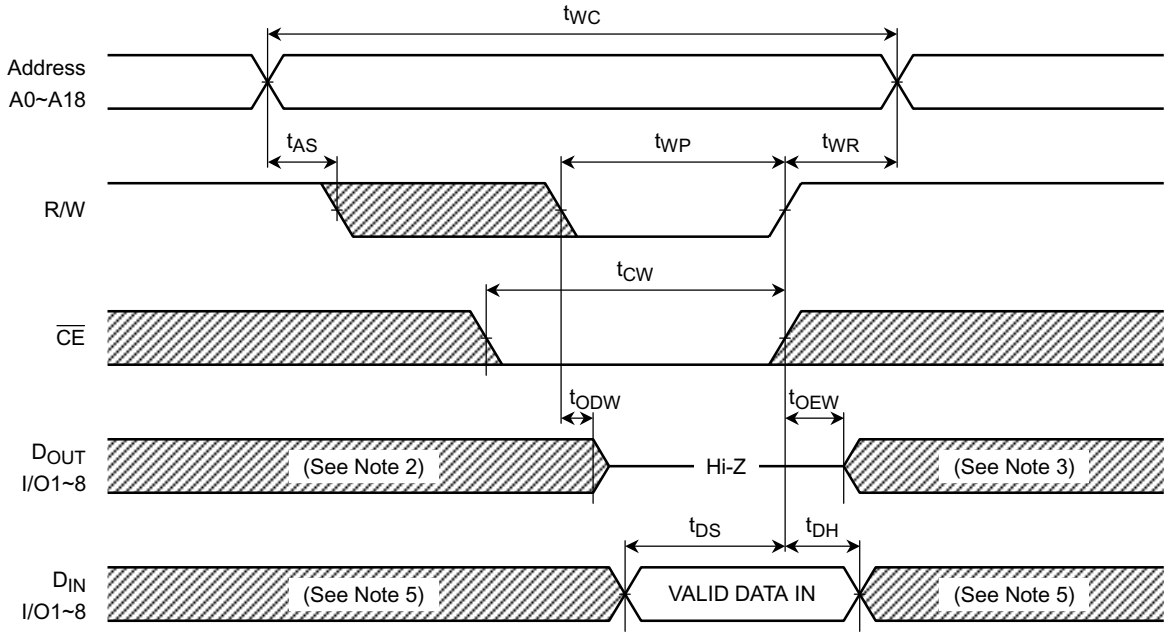
R1 = 810 Ω
R2 = 1610 Ω
V_{TM} = 2.3 V

TIMING DIAGRAMS

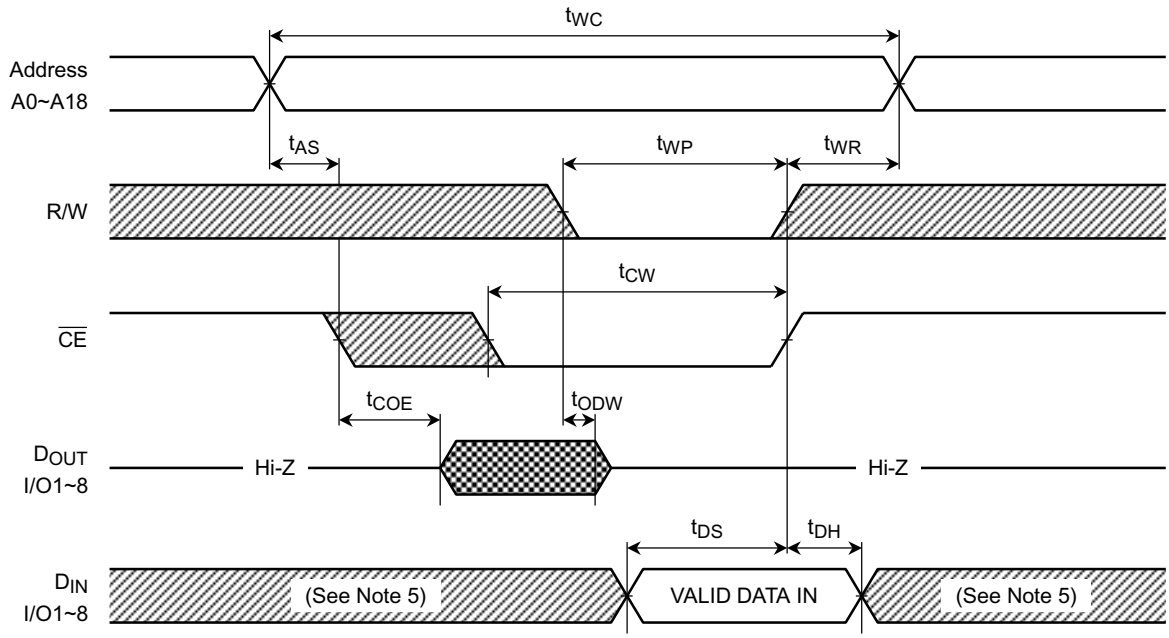
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)



Note:

(1) R/W remains HIGH for the read cycle.

(2) If $\overline{CE}$ goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If $\overline{CE}$ goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

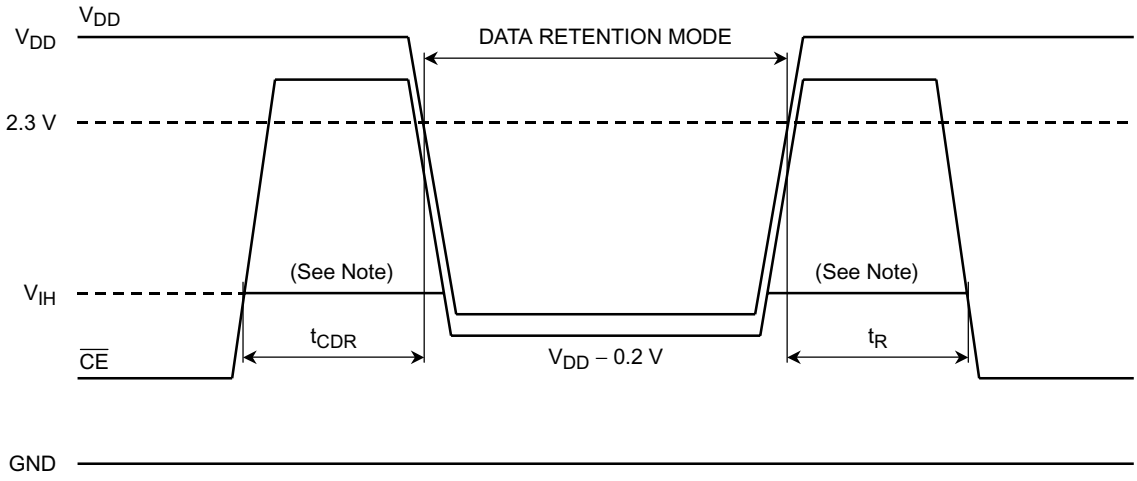
(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = –40° to 85°C)

SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V_{DH}	Data Retention Supply Voltage			1.5	—	3.6	V
I_{DDS2}	Standby Current	V_{DH} = 3.6 V	Ta = –40~85°C	—	—	10	μA
		V_{DH} = 3.0 V	Ta = –40~40°C	—	—	2	
			Ta = –40~85°C	—	—	5	
t_{CDR}	Chip Deselect to Data Retention Mode Time			0	—	—	ns
t_R	Recovery Time			5	—	—	ms

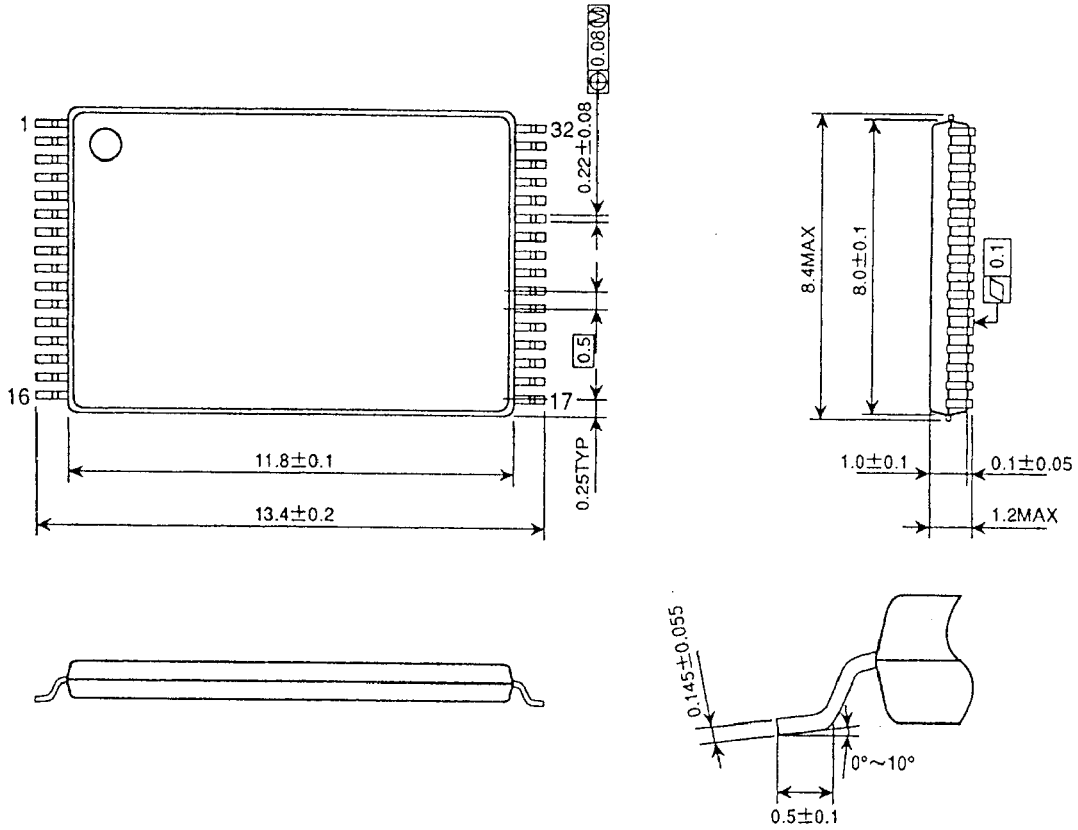
$\overline{CE}$ CONTROLLED DATA RETENTION MODE



Note: When $\overline{CE}$ is operating at the V_{IH}(min.) level, the operating current is given by I_{DDS1} during the transition of V_{DD} from 2.3(2.7) to 2.2V(2.4 V).

PACKAGE DIMENSIONS

TSOPI32-P-0.50 Unit: mm



Weight:0.22 g (typ)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.