

MC14528B

Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X .

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

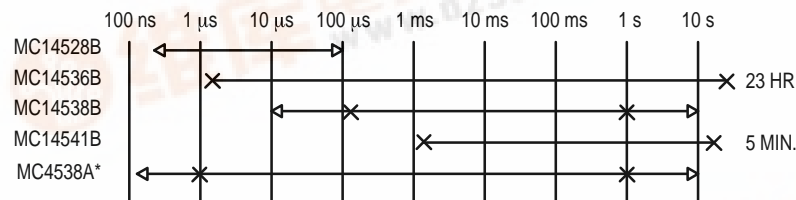
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

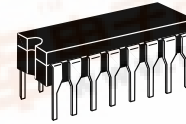
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C
 Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

ONE-SHOT SELECTION GUIDE

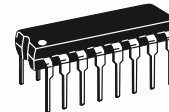


*LIMITED OPERATING VOLTAGE (2-6 V)

TOTAL OUTPUT PULSE WIDTH RANGE ← →
 RECOMMENDED PULSE WIDTH RANGE X X



L SUFFIX
 CERAMIC
 CASE 620



P SUFFIX
 PLASTIC
 CASE 648



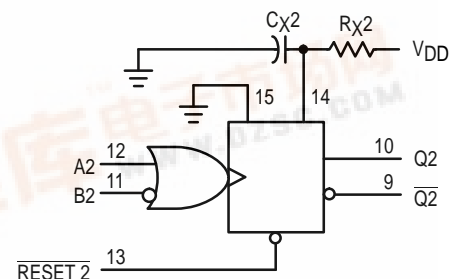
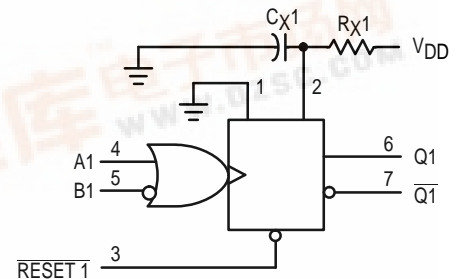
D SUFFIX
 SOIC
 CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
 MC14XXXBCL Ceramic
 MC14XXXBD SOIC

$T_A = - 55^\circ$ to 125°C for all packages.

BLOCK DIAGRAM



$V_{DD} = \text{PIN } 16$
 $V_{SS} = \text{PIN } 1, \text{ PIN } 8, \text{ PIN } 15$
 R_X AND C_X ARE EXTERNAL COMPONENTS

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

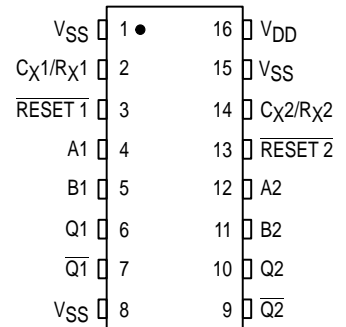
Characteristic	Symbol	V _{DD} Vdc	- 55 °C		25 °C			125 °C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
15		—	0.05	—	0	0.05	—	0.05		
	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
15		11	—	11	8.25	—	11	—		
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source	I _{OH}	5.0	- 1.2	—	- 1.0	- 1.7	—	- 0.7	mAdc
			5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	
	10		- 1.6	—	- 1.3	- 2.25	—	- 0.9		
	15		- 4.2	—	- 3.4	- 8.8	—	- 2.4		
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	mAdc
			10	1.6	—	1.3	2.25	—	0.9	
			15	4.2	—	3.4	8.8	—	2.4	
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
**Total Supply Current at an external load Capacitance (C _L) and at external timing capacitance (C _X), use the formula —	I _T	—	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD}^{-2})^2 f] \times 10^{-3}$ where: I _T in µA (per circuit), C _L and C _X in pF, R _X in megohms, V _{DD} in Vdc, f in kHz is input frequency.							µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

** The formulas given are for the typical characteristics only at 25 °C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS** ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	C_X pF	R_X k Ω	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	—	—	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH} , t_{PHL}	15	5.0	5.0 10 15	— — —	325 120 90	650 240 180	ns
Turn-Off, Turn-On Delay Time — A or B to Q or \bar{Q} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	t_{PLH} , t_{PHL}	1000	10	5.0 10 15	— — —	705 290 210	— — —	ns
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0 10 15	150 75 55	70 30 30	— — —	ns
	t_{WL}	1000	10	5.0 10 15	— — —	70 30 30	— — —	ns
Output Pulse Width — Q or \bar{Q} (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0 10 15	— — —	550 350 300	— — —	ns
Output Pulse Width — Q or \bar{Q} (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln [V_{DD} - V_{SS}]^\dagger$)	t_W	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	μs
Pulse Width Match between Circuits in the same package	$t_1 - t_2$	10,000	10	5.0 10 15	— — —	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — $\overline{\text{Reset}}$ to Q or \bar{Q}	t_{PLH} , t_{PHL}	15	5.0	5.0 10 15	— — —	325 90 60	600 225 170	ns
		1000	10	5.0 10 15	— — —	1000 300 250	— — —	ns
Retrigger Time	t_{rr}	15	5.0	5.0 10 15	0 0 0	— — —	— — —	ns
		1000	10	5.0 10 15	0 0 0	— — —	— — —	ns
External Timing Resistance	R_X	—	—	—	5.0	—	1000	k Ω
External Timing Capacitance	C_X	—	—	—	No Limits*			μF

$\dagger R_X$ is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{Out} in seconds.

* If $C_X > 15 \mu\text{F}$, Use Discharge Protection Diode D_X , per Fig. 9.

** The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	\bar{Q}
H		H		
H	L			
H		L	Not Triggered	Not Triggered
H	H		Not Triggered	Not Triggered
H	L, H,	H	Not Triggered	Not Triggered
H	L	L, H,	Not Triggered	Not Triggered
L	X	X	L	H
	X	X	Not Triggered	

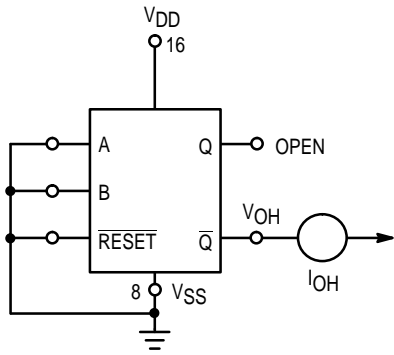


Figure 1. Output Source Current Test Circuit

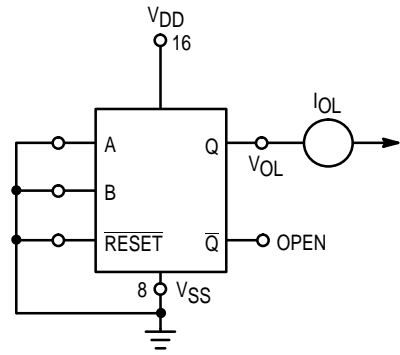


Figure 2. Output Sink Current Test Circuit

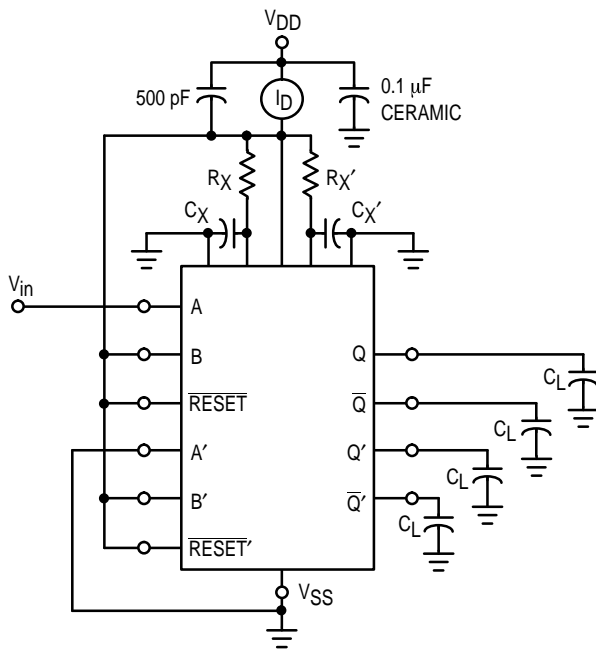


Figure 3. Power Dissipation Test Circuit and Waveforms

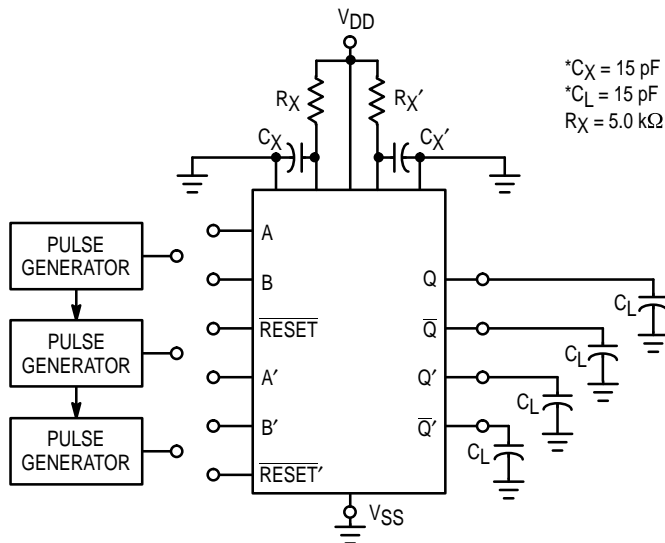


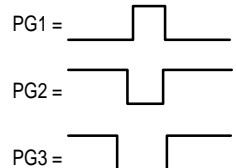
Figure 4. AC Test Circuit

INPUT CONNECTIONS

Characteristics	Reset	A	B
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} , t_W	VDD	PG1	VDD
t_{PLH} , t_{PHL} , t_{TLH} , t_{THL} , t_W	VDD	VSS	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

* Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.



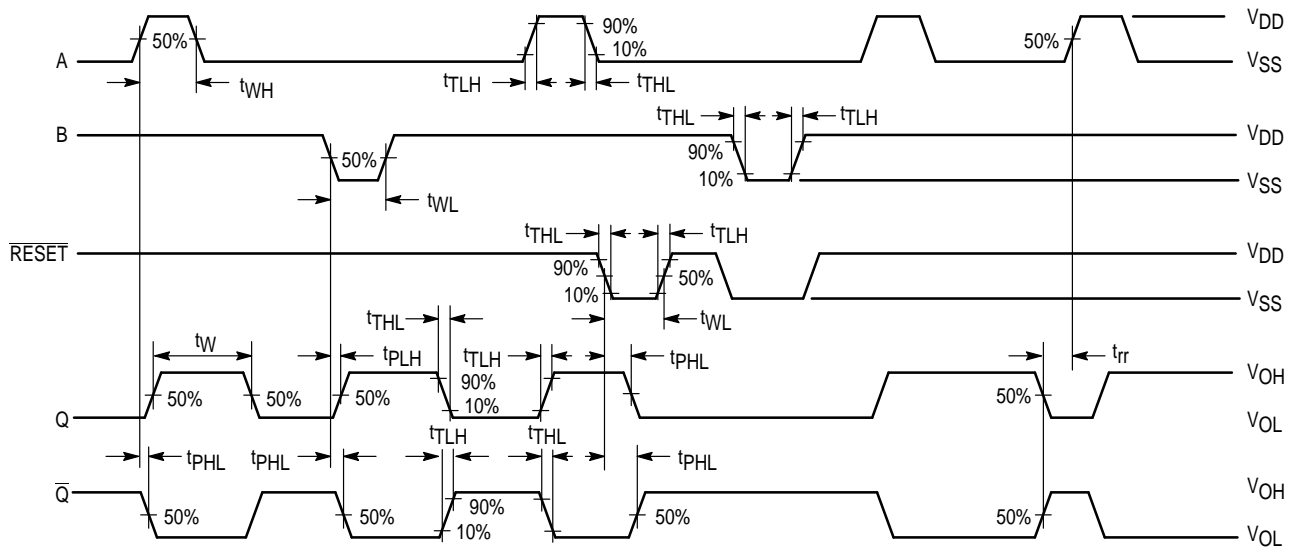


Figure 5. AC Test Waveforms

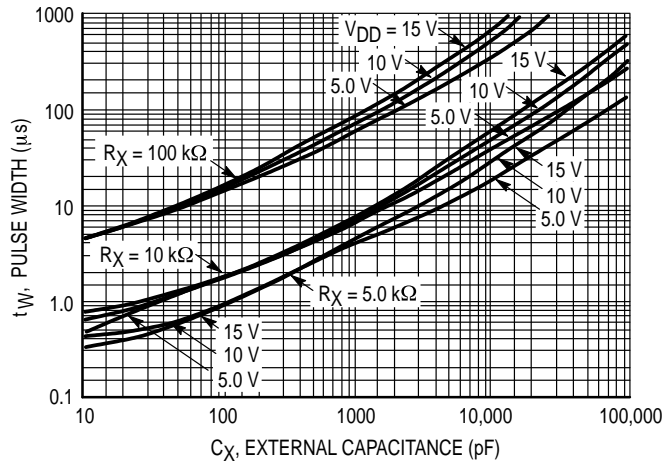


Figure 6. Pulse Width versus C_X

TYPICAL APPLICATIONS

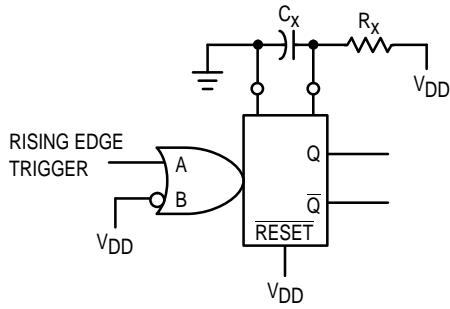


Figure 7. Retriggerable Monostables Circuitry

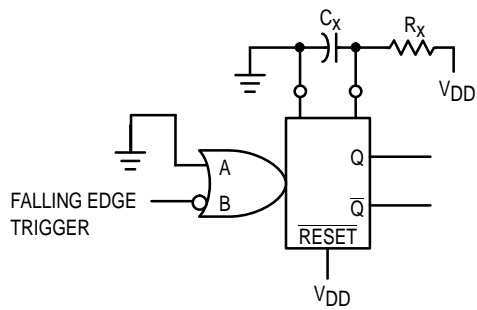


Figure 7. Retriggerable Monostables Circuitry

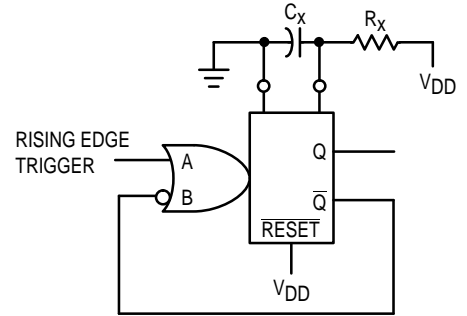


Figure 8. Non-Retriggerable Monostables Circuitry

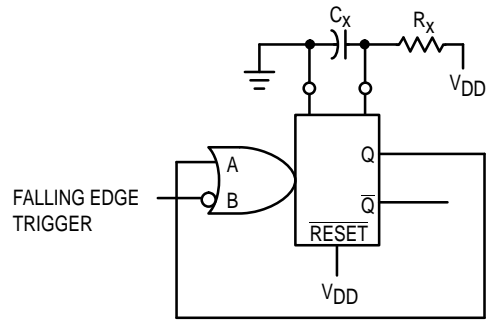


Figure 8. Non-Retriggerable Monostables Circuitry

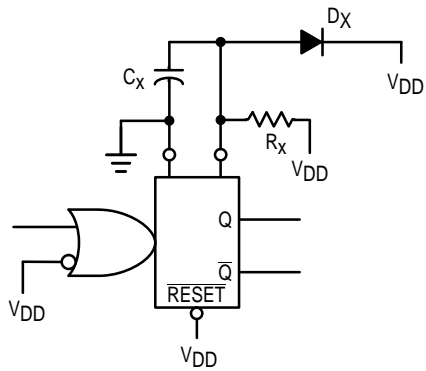


Figure 9. Use of a Diode to Limit Power Down Current Surge

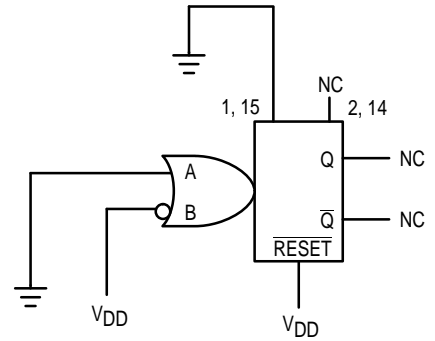
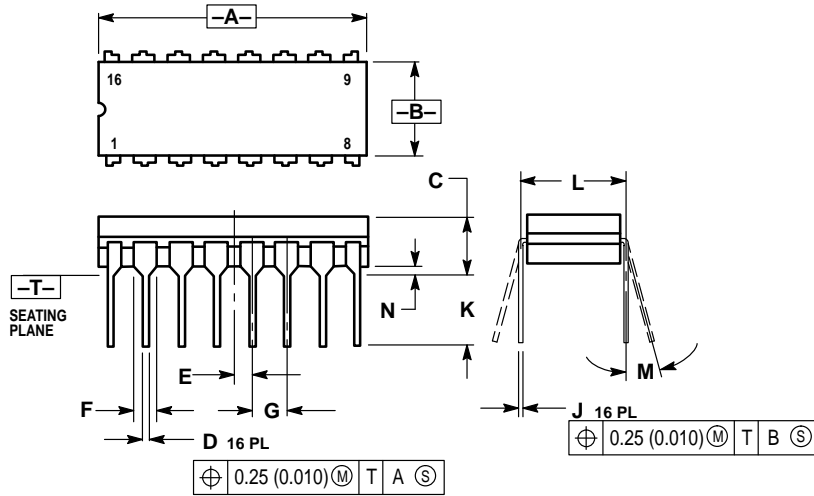


Figure 10. Connection of Unused Sections

OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

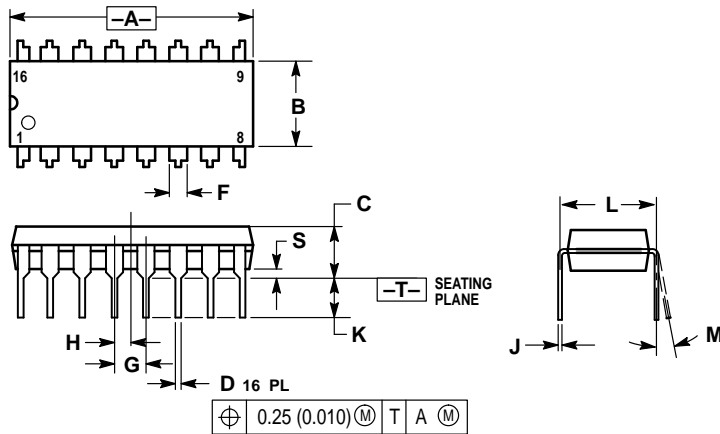


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



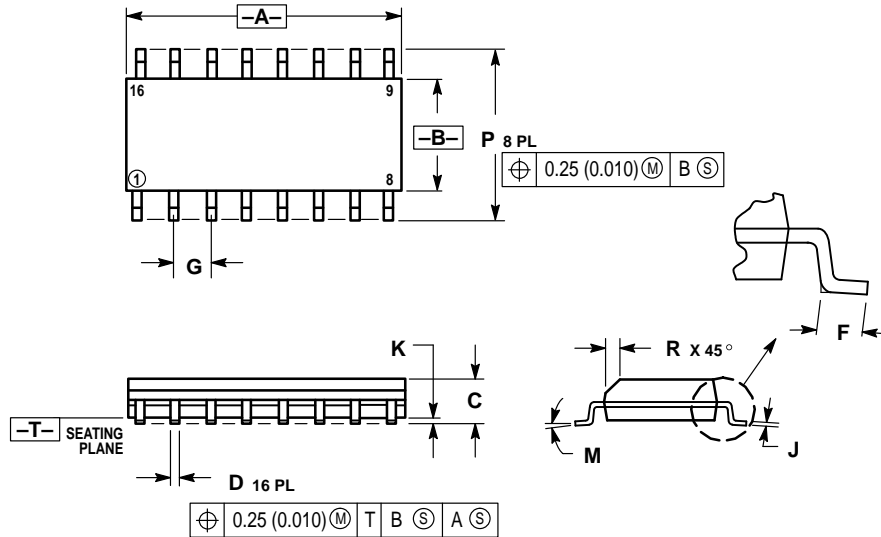
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298