

intersil

CD4508BMS

December 1992

CMOS Dual 4-Bit Latch

Features

- High-Voltage Types (20-Volt Rating)
- Two Independent 4-Bit Latches
- Individual Master Reset for Each 4-Bit Latch
- 3-State Outputs with High-Impedance State for Bus Line Applications
- Medium-Speed Operation: $t_{PHL} = t_{PLH} = 70\text{nS}$ (Typ.) at $V_{DD} = 10\text{V}$ and $C_L = 50\text{pF}$
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of $1\mu\text{A}$ at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package-Temperature Range):
 - 1V at $V_{DD} = 5\text{V}$
 - 2V at $V_{DD} = 10\text{V}$
 - 2.5V at $V_{DD} = 15\text{V}$
- Meets all Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Buffer Storage
- Holding Registers
- Data Storage and Multiplexing

Description

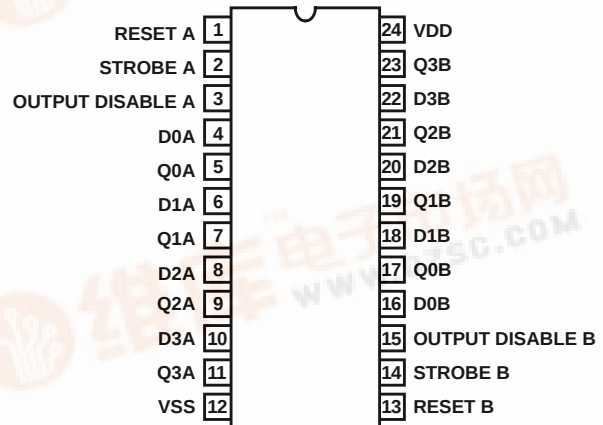
CD4508BMS dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

The CD4508BMS is supplied in these 24 lead outline packages:

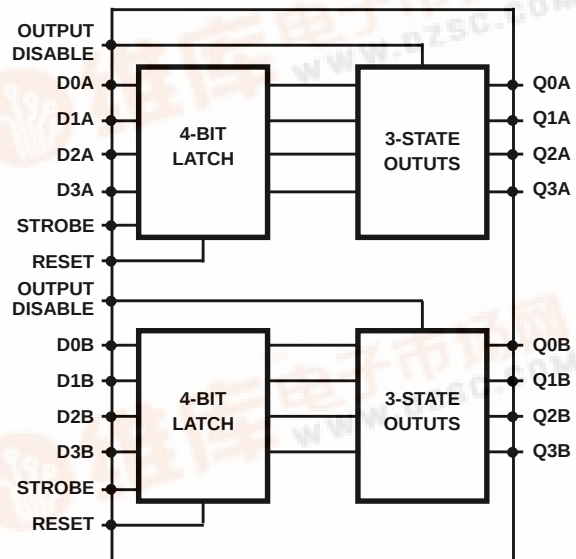
Braze Seal DIP	H4V
Frit Seal DIP	H1Z
Ceramic Flatpack	H4P

Pinout

CD4508BMS
TOP VIEW



Functional Diagram



Specifications CD4508BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input $\pm 10\text{mA}$
 Operating Temperature Range -55°C to +125°C
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to +150°C
 Lead Temperature (During Soldering) +265°C
 At Distance 1/16 $\pm$ 1/32 Inch (1.59mm $\pm$ 0.79mm) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at +125°C
 For $T_A = -55^\circ\text{C}$ to +100°C (Package Type D, F, K) 500mW
 For $T_A = +100^\circ\text{C}$ to +125°C (Package Type D, F, K) Derate
 Linearity at 12mW/°C to 200mW
 Device Dissipation per Output Transistor 100mW
 For $T_A =$ Full Package Temperature Range (All Package Types)
 Junction Temperature +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	μA
				2	+125°C	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10 μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10 μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V
Tri-State Output Leakage	IOZL	VIN = VDD or GND VOUT = 0V	VDD = 20V	1	+25°C	-0.4	-	μA
				2	+125°C	-12	-	μA
			VDD = 18V	3	-55°C	-0.4	-	μA
Tri-State Output Leakage	IOZH	VIN = VDD or GND VOUT = VDD	VDD = 20V	1	+25°C	-	0.4	μA
				2	+125°C	-	12	μA
			VDD = 18V	3	-55°C	-	0.4	μA

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
 2. Go/No Go test with limits applied to inputs.

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Strobe In to Data Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	260	ns
			10, 11	+125°C, -55°C	-	351	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND (Note 1, 2)	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Strobe In to Data Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Data In to Data Out	TPHL2 TPLH2	VDD = 5V	1, 2, 3	+25°C	-	210	ns
		VDD = 10V	1, 2, 3	+25°C	-	120	ns
		VDD = 15V	1, 2, 3	+25°C	-	90	ns
Propagation Delay Reset to Data Out	TPHL3 TPLH3	VDD = 5V	1, 2, 3	+25°C	-	180	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Propagation Delay 3-State	TPHZ TPZH	VDD = 5V	1, 2, 4	+25°C	-	180	ns
		VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time 3-State	TPLZ TPZL	VDD = 5V	1, 2, 4	+25°C	-	180	ns
		VDD = 10V	1, 2, 4	+25°C	-	100	ns
		VDD = 15V	1, 2, 4	+25°C	-	70	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Minimum Strobe Pulse Width	TWS	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns
Minimum Data Setup Time	TS	VDD = 5V	1, 2, 3	+25°C	-	50	ns
		VDD = 10V	1, 2, 3	+25°C	-	30	ns
		VDD = 15V	1, 2, 3	+25°C	-	20	ns
Minimum Data Hold Time	TH	VDD = 5V	1, 2, 3	+25°C	-	0	ns
		VDD = 10V	1, 2, 3	+25°C	-	0	ns
		VDD = 15V	1, 2, 3	+25°C	-	0	ns
Minimum Reset Pulse Width	TWR	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	140	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V

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TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
N Threshold Voltage Delta	ΔV_{TN}	VDD = 10V, ISS = -10 μ A	1, 4	+25°C	-	± 1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10 μ A	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔV_{TP}	VSS = 0V, IDD = 10 μ A	1, 4	+25°C	-	± 1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND. 3. See Table 2 for +25°C limit.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	$\pm 1.0\mu$ A
Output Current (Sink)	IOL5	$\pm 20\%$ x Pre-Test Reading
Output Current (Source)	IOH5A	$\pm 20\%$ x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

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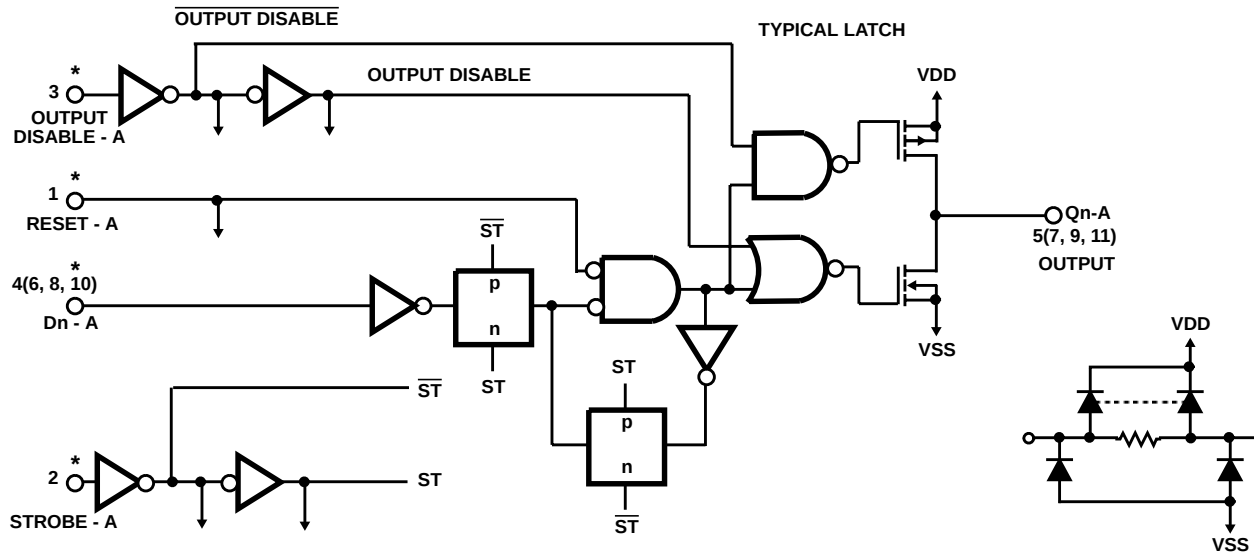
TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	5, 7, 9, 11, 17, 19, 21, 23	1-4, 6, 8, 10, 12-16, 18, 20, 22	24			
Static Burn-In 2 Note 1	5, 7, 9, 11, 17, 19, 21, 23	12	1-4, 6, 8, 10, 13- 16, 18, 20, 22, 24			
Dynamic Burn-In Note 1	-	1, 3, 12, 13, 15	2, 14, 24	5, 7, 9, 11, 17, 19, 21, 23	4, 6, 8, 10, 16, 18, 20, 22	-
Irradiation Note 2	5, 7, 9, 11, 17, 19, 21, 23	12	1-4, 6, 8, 10, 13- 16, 18, 20, 22, 24			

NOTES:

- Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$, VDD = $18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = $10V \pm 0.5V$

Logic Diagram



* All inputs protected by CMOS protection network.

FIGURE 1. LOGIC DIAGRAM (A-SECTION), 1 OF 4 IDENTICAL LATCHES WITH COMMON OUTPUT DISABLE, RESET AND STROBE

TRUTH TABLE

RESET	DISABLE	STROBE	D INPUT	Q OUTPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	LATCHED
1	0	X	X	0
X	1	X	X	Z

1 = HIGH LEVEL
0 = LOW LEVEL

X = DON'T CARE
Z = HIGH IMPEDANCE

CD4508BMS

Typical Performance Characteristics

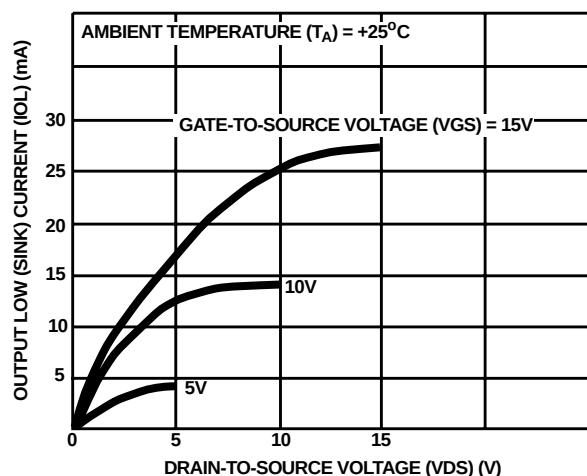


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

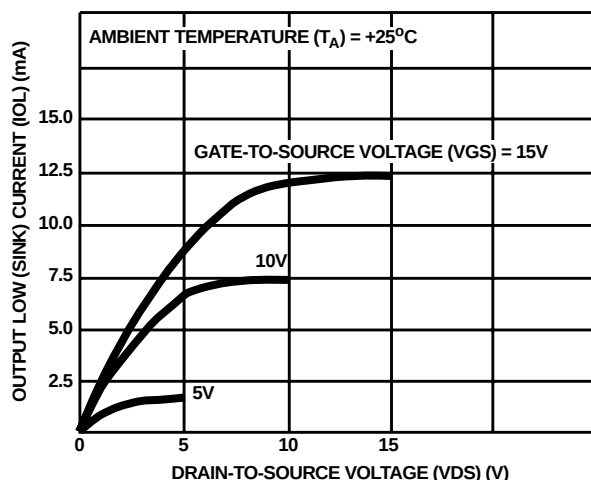


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

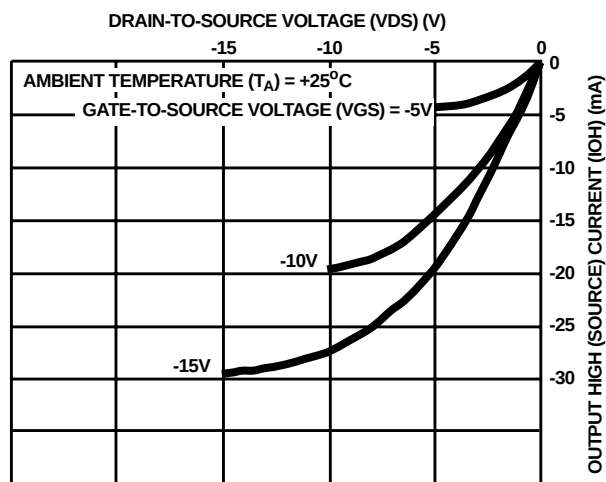


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

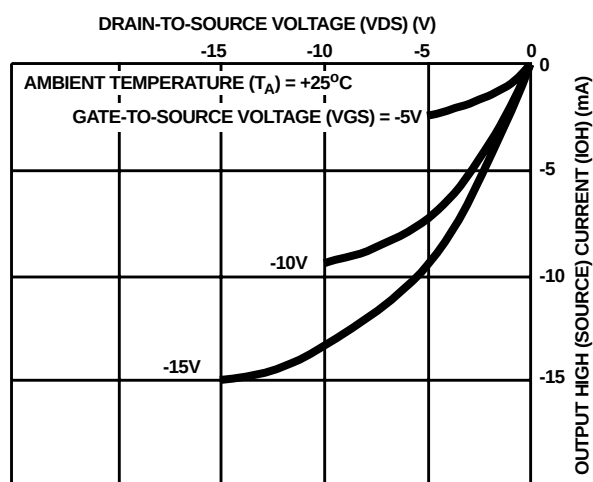


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

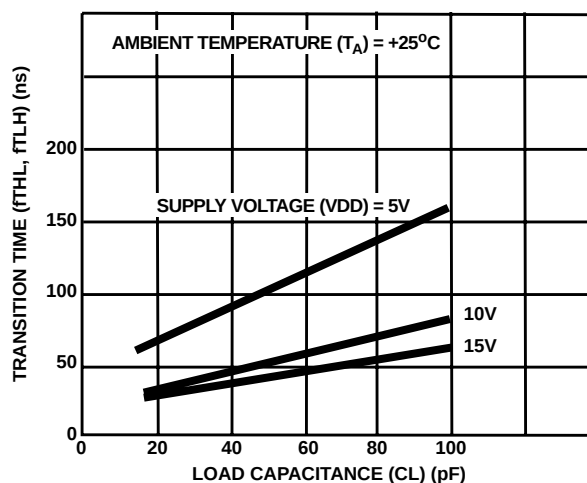


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

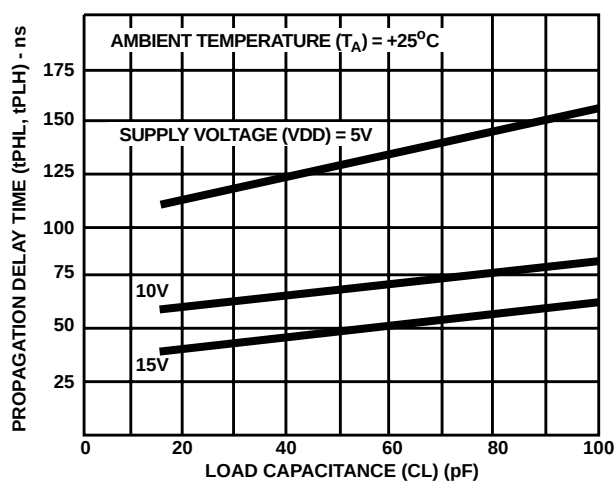


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (STROBE TO DATA OUT)

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Typical Performance Characteristics (Continued)

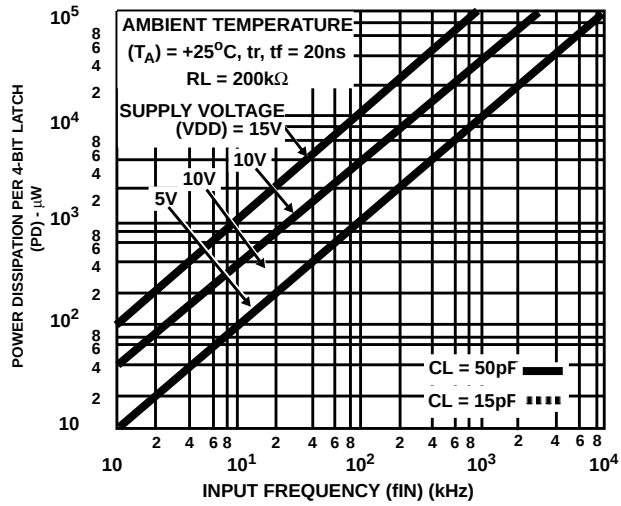


FIGURE 8. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Waveforms and Test Circuits

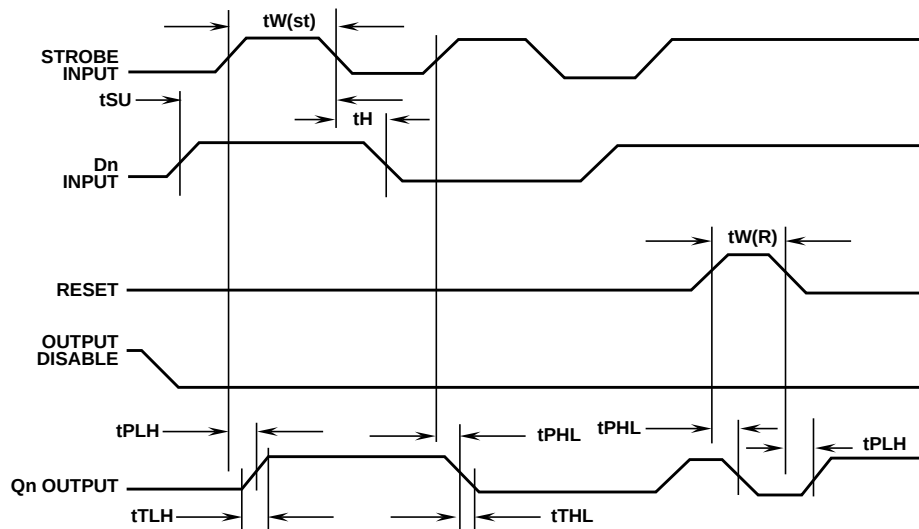


FIGURE 9. TEST WAVEFORMS

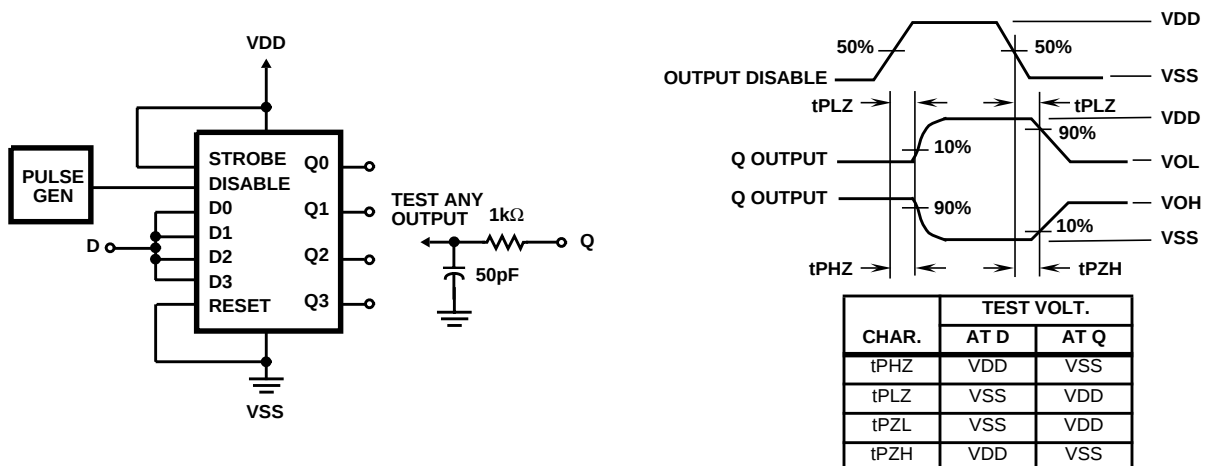


FIGURE 10. OUTPUT DISABLE TEST CIRCUIT AND WAVEFORMS

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Bus Registers

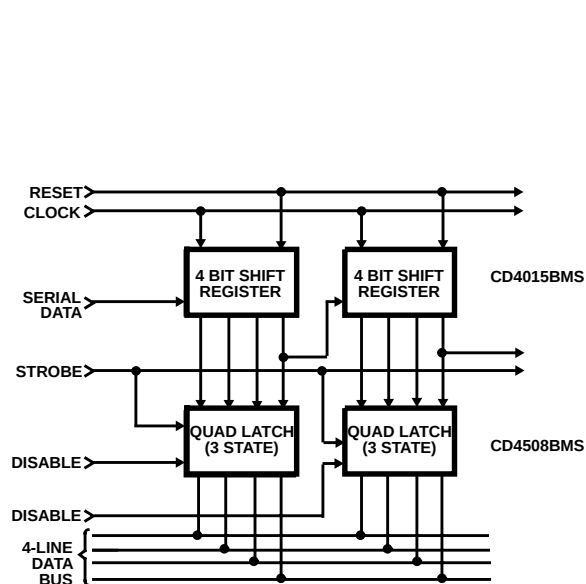


FIGURE 11. BUS REGISTER

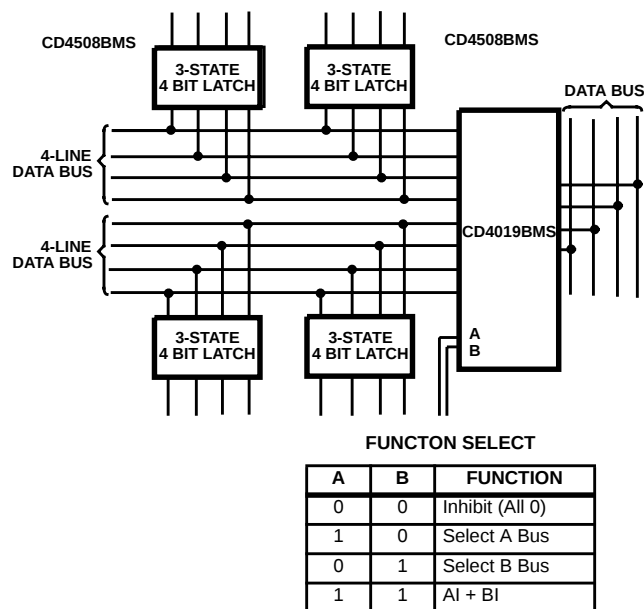
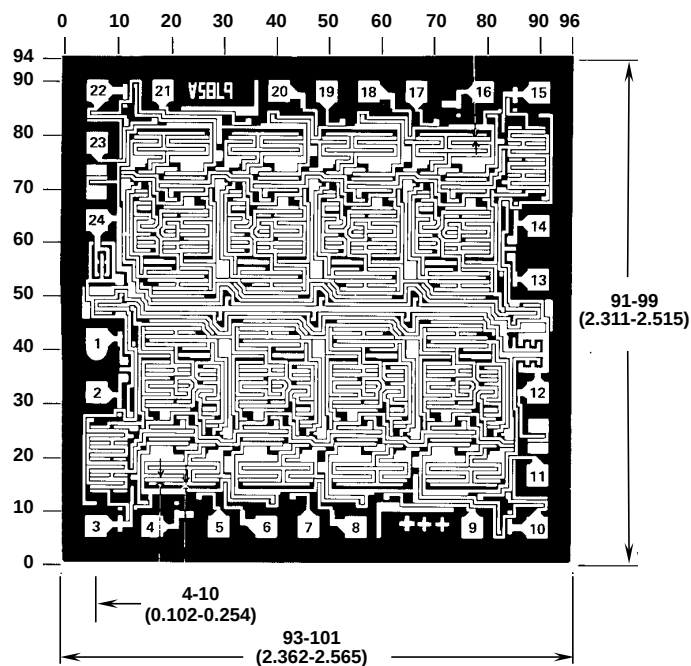


FIGURE 12. DUAL MULTIPLEXED BUS REGISTER WITH FUNCTION SELECT

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch.)

METALLIZATION: Thickness: $11\text{k}\text{\AA}$ - $14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA}$ - $15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches