

LT1678/LT1679

Dual/Quad Low Noise, Rail-to-Rail, Precision Op Amps

FEATURES

- Rail-to-Rail Input and Output
- 100% Tested Low Voltage Noise:
 - $3.9 \text{nV}/\sqrt{\text{Hz}}$ Typ at 1kHz
 - 5.5nV/√Hz Max at 1kHz
- Single Supply Operation from 2.7V to 36V
- Offset Voltage: 100µV Max
- Low Input Bias Current: 20nA Max
- High A_{VOI} : $3V/\mu V$ Min, $R_{I} = 10k$
- High CMRR: 100dB Min
- High PSRR: 106dB Min
- Gain Bandwidth Product: 20MHz
- Operating Temperature Range: -40°C to 85°C
- Matching Specifications
- No Phase Inversion
- 8-Lead SO and 14-Lead SO Packages

APPLICATIONS

- Strain Gauge Amplifiers
- Portable Microphones
- Battery-Powered Rail-to-Rail Instrumentation
- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Infrared Detectors

DESCRIPTION

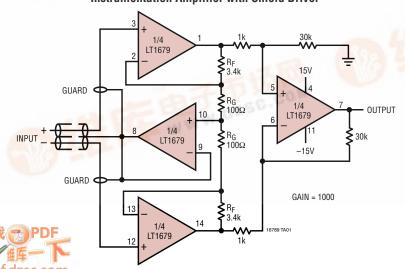
The LT®1678/LT1679 are dual/quad rail-to-rail op amps offering both low noise and precision: 3.9nV/√Hz wideband noise, 1/f corner frequency of 4Hz and 90nV peak-to-peak 0.1Hz to 10Hz noise are combined with outstanding precision: 100μV maximum offset voltage, greater than 100dB common mode and power supply rejection and 20MHz gain bandwidth product. The LT1678/LT1679 bring precision as well as low noise to single supply applications as low as 3V. The input range exceeds the power supply by 100mV with no phase inversion while the output can swing to within 170mV of either rail.

The LT1678/LT1679 are offered in the SO-8 and SO-14 packages. A full set of matching specifications are also provided, facilitating their use in matching dependent applications such as a two op amp instrumentation amplifier design. The LT1678/LT1679 are specified for supply voltages of ±15V, single 5V as well as single 3V. For a single amplifier with similiar performance, see the LT1677 data sheet.

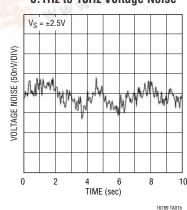
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TYPICAL APPLICATION

Instrumentation Amplifier with Shield Driver



0.1Hz to 10Hz Voltage Noise

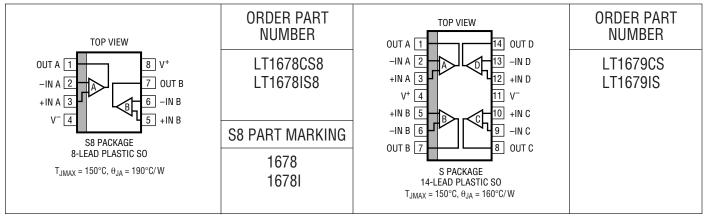


ABSOLUTE MAXIMUM RATINGS

(Note 1)	
Supply Voltage	±18V
Input Voltages (Note 2) 0.3V	Beyond Either Rail
Differential Input Current (Note 2)	±25mA
Output Short-Circuit Duration (Note 3) Indefinite
Storage Temperature Range	65°C to 150°C

Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
(Note 4)	40°C to 85°C
Specified Temperature Range	
(Note 5)	40°C to 85°C

PACKAGE/ORDER INFORMATION



Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_S = 3V$, $V_{CM} = V_0 = 1.7V$; $V_S = 5V$, $V_{CM} = V_0 = 2.5V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	(Note 11) $0^{\circ}C \le T_{A} \le 70^{\circ}C$ $-40^{\circ}C \le T_{A} \le 85^{\circ}C$	•		35 55 75	100 270 350	μV μV μV
		$ \begin{array}{c c} V_S = & 5V, \ V_{CM} = V_S + 0.1V \\ V_S = & 5V, \ V_{CM} = V_S - 0.3V, \ 0^{\circ}C \leq T_A \leq 70^{\circ}C \\ V_S = & 5V, \ V_{CM} = V_S - 0.3V, -40^{\circ}C \leq T_A \leq 85^{\circ}C \end{array} $	• •		150 180 200	550 750 1000	μV μV μV
		$ \begin{array}{c} V_S = 5V, V_{CM} = -0.1V \\ V_S = 5V, V_{CM} = 0V, 0^{\circ}C \leq T_A \leq 70^{\circ}C \\ V_S = 5V, V_{CM} = 0V, -40^{\circ}C \leq T_A \leq 85^{\circ}C \end{array} $	• •		1.5 1.8 2.0	30 45 50	mV mV mV
$\Delta V_{OS} \over \Delta Temp$	Average Input Offset Drift (Note 10)		•		0.40	3	μV/°C
l _B	Input Bias Current	(Note 11) 0°C ≤ T _A ≤ 70°C -40°C ≤ T _A ≤ 85°C	•		±2 ±3 ±7	±20 ±35 ±50	nA nA nA
		$ \begin{array}{c} V_S = 5V, \ V_{CM} = V_S + 0.1V \\ V_S = 5V, \ V_{CM} = V_S - 0.3V, \ 0^{\circ}C \leq T_A \leq 70^{\circ}C \\ V_S = 5V, \ V_{CM} = V_S - 0.3V, -40^{\circ}C \leq T_A \leq 85^{\circ}C \end{array} $	•		0.19 0.19 0.25	0.40 0.60 0.75	μΑ μΑ Αμ
		$ \begin{aligned} &V_S = 5V, V_{CM} = -0.1V \\ &V_S = 5V, V_{CM} = 0V, 0^{\circ}C \leq T_A \leq 70^{\circ}C \\ &V_S = 5V, V_{CM} = 0V, -40^{\circ}C \leq T_A \leq 85^{\circ}C \end{aligned} $	•	-5 -8.4 -10	-0.41 -0.45 -0.47		μΑ μΑ Αμ

ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_S = 3V$, $V_{CM} = V_0 = 1.7V$; $V_S = 5V$, $V_{CM} = V_0 = 2.5V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	M	N TYP	MAX	UNITS
I _{OS}	Input Offset Current	4000 T 0500	•	4 5 8	25 35 55	nA nA nA
		$V_S = 5V$, $V_{CM} = V_S + 0.1V$ $V_S = 5V$, $V_{CM} = V_S - 0.3V$, $0^{\circ}C \le T_A \le 70^{\circ}C$ $V_S = 5V$, $V_{CM} = V_S - 0.3V$, $-40^{\circ}C \le T_A \le 85^{\circ}C$	•	6 10 15	30 40 65	nA nA nA
		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	•	0.1 0.1 0.15	1.6 2.0 2.4	μΑ μΑ μΑ
e _n	Input Noise Voltage	0.1Hz to 10Hz (Note 7) V _{CM} = V _S V _{CM} = 0V		90 180 1600		nV _{P-P} nV _{P-P} nV _{P-P}
	Input Noise Voltage Density (Note 8)	$f_0 = 10$ Hz $V_{CM} = V_S, f_0 = 10$ Hz $V_{CM} = 0V, f_0 = 10$ Hz		4.4 6.6 19		nV/√Hz nV/√Hz nV/√Hz
		$f_0 = 1 \text{kHz}$ $V_{CM} = V_S, f_0 = 1 \text{kHz}$ $V_{CM} = 0V, f_0 = 1 \text{kHz}$		3.9 5.3 9	5.5	nV/√Hz nV/√Hz nV/√Hz
i _n	Input Noise Current Density	$f_0 = 10Hz$ $f_0 = 1kHz$		1.2 0.3		pA/√Hz pA/√Hz
V _{CM}	Input Voltage Range		- 0		V _S + 0.1V V _S - 0.3V	V
R _{IN}	Input Resistance	Common Mode		2		GΩ
C _{IN}	Input Capacitance			4.2		pF
CMRR	Common Mode Rejection Ratio	V _S = 5V, V _{CM} = 1.9V to 3.9V V _S = 5V, V _{CM} = 1.9V to 3.9V	• 9 9			dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.7V \text{ to } 36V, V_{CM} = V_0 = 1.7V$ $V_S = 3.1V \text{ to } 36V, V_{CM} = V_0 = 1.7V$	• 10 • 9			dB dB
A _{VOL}	Large-Signal Voltage Gain	$V_S = 3V$, $R_L = 10k$, $V_0 = 2.5V$ to 0.7V	• 0. • 0.			V/μV V/μV
		4000 T 0500	0. 0. 0.	4 0.9		V/μV V/μV V/μV
		- A - 1 - A	0.2 0.2 0.3	15 0.40		V/μV V/μV V/μV
		$V_S = 5V$, $R_L = 10k$, $V_0 = 4.5V$ to 0.7V $0^{\circ}C < T_A < 70^{\circ}C$ $-40 < T_A < 85^{\circ}C$	0. 0.	6 2		V/μV V/μV V/μV
		1 1010 7	0. 0. 0.	6 3.2		V/μV V/μV V/μV
		1 1010 7	0. 0. 0.	5 2.8		V/μV V/μV V/μV
V _{OL}	Output Voltage Swing Low (Note 11)	Above GND $I_{SINK} = 0.1 mA$ $0°C \le T_A \le 70°C$ $-40°C \le T_A \le 85°C$	•	80 125 130	170 200 250	mV mV mV

ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_S = 3V$, $V_{CM} = V_0 = 1.7V$; $V_S = 5V$, $V_{CM} = V_0 = 2.5V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		MIN	TYP	MAX	UNITS
V _{OL}	Output Voltage Swing Low (Note 11)	Above GND $I_{SINK} = 2.5mA$ $0^{\circ}C \le T_{A} \le 70^{\circ}C$ $-40^{\circ}C \le T_{A} \le 85^{\circ}C$ Above GND	•		170 195 205	250 320 350	mV mV
		$\begin{array}{l} I_{SINK} = 10\text{mA} \\ 0^{\circ}\text{C} \leq T_{A} \leq 70^{\circ}\text{C} \\ -40^{\circ}\text{C} \leq T_{A} \leq 85^{\circ}\text{C} \end{array}$	•		370 440 465	600 720 770	mV mV mV
V _{OH}	Output Voltage Swing High (Note 11)	Below V_S $I_{SOURCE} = 0.1 \text{ mA}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	•		75 85 93	150 200 250	mV mV mV
		Below V_S $I_{SOURCE} = 2.5 \text{mA}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	•		110 195 205	250 350 375	mV mV mV
		Below V_S $I_{SOURCE} = 10 \text{mA}$ $0^{\circ}\text{C} \le T_A \le 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \le T_A \le 85^{\circ}\text{C}$	•		170 200 230	400 500 550	mV mV mV
I _{SC}	Output Short-Circuit Current (Note 3)	$V_S = 3V$ $V_S = 5V$	•	15 13 18	22 19 29		mA mA mA
		vS - 3v	•	14	25		mA
SR	Slew Rate (Note 13)	$A_V = -1$, $R_L = 10k$ $R_L = 10k$, $0^{\circ}C \le T_A \le 70^{\circ}C$ $R_L = 10k$, $-40^{\circ}C \le T_A \le 85^{\circ}C$	•	4 3.5 3	6 5.8 5.5		V/μs V/μs V/μs
GBW	Gain Bandwidth Product (Note 11)	$f_0 = 100 \text{kHz}$ $f_0 = 100 \text{kHz}$	•	13 12.5	20 19		MHz MHz
t _S	Settling Time	2V Step 0.1%, A _V = +1 2V Step 0.01%, A _V = +1			1.4 2.4		μS μS
R_0	Open-Loop Output Resistance Closed-Loop Output Resistance	I _{OUT} = 0 A _V = 100, f = 10kHz			100 1		Ω
Is	Supply Current per Amplifier (Note 12)		•		2 2.5	3.4 3.8	mA mA
ΔV_{0S}	Offset Voltage Match (Notes 11, 15)	$0^{\circ}C \le T_{A} \le 70^{\circ}C$ - $40^{\circ}C \le T_{A} \le 85^{\circ}C$	•		35 55 75	150 400 525	μV μV μV
ΔΙΒ+	Noninverting Bias Current Match (Notes 11, 15)	$0^{\circ}\text{C} \le \text{T}_{\text{A}} \le 70^{\circ}\text{C}$ $-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le 85^{\circ}\text{C}$	•		±2 ±3 ±7	±30 ±55 ±75	nA nA nA
ΔCMRR	Common Mode Rejection Match (Notes 11, 14, 15)	V _S = 5V, V _{CM} = 1.9V to 3.9V	•	94 88	110 110		dB dB
ΔPSRR	Power Supply Rejection Match (Notes 11, 14, 15)	$V_S = 2.7V \text{ to } 36V, V_{CM} = V_0 = 1.7V$ $V_S = 3.1V \text{ to } 36V, V_{CM} = V_0 = 1.7V$	•	96 94	120 120		dB dB

ELECTRICAL CHARACTERISTICS The ullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25\,^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = V_0 = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		MIN	TYP	MAX	UNITS
V _{0S}	Input Offset Voltage	$0^{\circ}C \le T_{A} \le 70^{\circ}C$ -40°C \le T_{A} \le 85°C	•		20 30 45	150 350 420	μV μV μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift (Note 10)		•		0.40	3	μV/°C
I _B	Input Bias Current	$0^{\circ}C \le T_{A} \le 70^{\circ}C$ -40°C \le T_{A} \le 85°C	•		±2 ±3 ±7	±20 ±35 ±50	nA nA nA
I _{OS}	Input Offset Current	$0^{\circ}C \le T_{A} \le 70^{\circ}C$ -40°C \le T_{A} \le 85°C	•		3 5 8	25 35 55	nA nA nA
e _n Input Noise Voltage	Input Noise Voltage	0.1Hz to 10Hz (Note 7) $V_{CM} = 15V$ $V_{CM} = -15V$			90 180 1600		nV _{P-P} nV _{P-P}
Input Noise Voltage Dens	Input Noise Voltage Density	$f_0 = 10$ Hz $V_{CM} = 15$ V, $f_0 = 10$ Hz $V_{CM} = -15$ V, $f_0 = 10$ Hz			4.4 6.6 19		nV/√Hz nV/√Hz nV/√Hz
		$f_0 = 1 \text{kHz}$ $V_{CM} = 15 \text{V}, f_0 = 1 \text{kHz}$ $V_{CM} = -15 \text{V}, f_0 = 1 \text{kHz}$			3.9 5.3 9	5.5	nV/√Hz nV/√Hz nV/√Hz
i _n	Input Noise Current Density	f ₀ = 10Hz f ₀ = 1kHz			1.2 0.3		pA/√Hz pA/√Hz
V _{CM}	Input Voltage Range (Note 16)		•	-13.3		14	V
R _{IN}	Input Resistance	Common Mode			2		GΩ
C _{IN}	Input Capacitance				4.2		pF
CMRR	Common Mode Rejection Ratio	$V_{CM} = -13.3V$ to 14V	•	100 96	130 124		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.7 V \text{ to } \pm 18 V$	•	106 100	130 125		dB dB
A _{VOL}	Large-Signal Voltage Gain	$R_L = 10k$, $V_0 = \pm 14V$ $0^{\circ}C \le T_A \le 70^{\circ}C$ $-40^{\circ}C \le T_A \le 85^{\circ}C$	•	3 2 1	7 6 4		V/μV V/μV V/μV
		$R_L = 2k, V_0 = \pm 13.5V$ $0^{\circ}C \le T_A \le 70^{\circ}C$ $-40^{\circ}C \le T_A \le 85^{\circ}C$	•	0.8 0.5 0.4	1.7 1.4 1.1		V/μV V/μV V/μV

ELECTRICAL CHARACTERISTICS The ullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_S = \pm 15V$, $V_{CM} = V_0 = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		MIN	TYP	MAX	UNITS
V _{OL}	Output Voltage Swing Low	Above –V _S					
		$I_{SINK} = 0.1 mA$			110	200	mV
		$0^{\circ}C \leq T_{A} \leq 70^{\circ}C$			125	230	mV
		$-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$	•		130	260	mV
		Above – V _S I _{SINK} = 2.5mA			170	280	mV
		$0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 70^{\circ}\text{C}$			195	350	mV
		$-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$			205	380	mV
		Above -V _S	+				
		I _{SINK} = 10mA			370	600	mV
		$0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 70^{\circ}\text{C}$			440	700	mV
		$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le 85^{\circ}\text{C}$	•		450	750	mV
V _{OH}	Output Voltage Swing High	Below +V _S					
		I _{SOURCE} = 0.1mA			80	150	mV
		$0^{\circ}C \leq T_{A} \leq 70^{\circ}C$			90	200	mV
		$-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$	•		100	250	mV
		Below +V _S			110	200	m\/
		$I_{SOURCE} = 2.5mA$ $0^{\circ}C \le T_A \le 70^{\circ}C$			110 120	300	mV mV
		$-40^{\circ}\text{C} \le T_{A} \le 70^{\circ}\text{C}$			120	350	mV
		Below +V _S			120	000	1111
		I _{SOURCE} = 10mA			200	450	mV
		0°C ≤ T _A ≤ 70°C			250	500	mV
		$-40^{\circ}\text{C} \le \text{T}_{A} \le 85^{\circ}\text{C}$	•		250	550	mV
I _{SC}	Output Short-Circuit Current (Note 3)			20	35		mA
			•	15	28		mA
SR	Slew Rate	R _L = 10k (Note 9)		4	6		V/µs
		$R_L = 10k \text{ (Note 9) } 0^{\circ}\text{C} \le T_A \le 70^{\circ}\text{C}$		3.5 3	5.8 5.5		V/µs
ODW/	0 : 0	$R_L = 10k \text{ (Note 9)} - 40^{\circ}\text{C} \le T_A \le 85^{\circ}\text{C}$	•				V/µs
GBW	Gain Bandwidth Product	$f_0 = 100 \text{kHz}$ $f_0 = 100 \text{kHz}$		13 12.5	20 19		MHz MHz
THD	Total Harmonic Distortion	$R_L = 2k, A_V = 1, f_0 = 1kHz, V_0 = 20V_{P-P}$		12.0	0.00025		%
	Settling Time	$10V \text{ Step } 0.1\%, A_V = +1$			2.7		
ts	Setting Time	10V Step 0.1%, $A_V = +1$ 10V Step 0.01%, $A_V = +1$			3.9		μS μS
R_0	Open-Loop Output Resistance	I _{OUT} = 0			100		Ω
	Closed-Loop Output Resistance	$A_V = 100, f = 10kHz$			1		Ω
I _S	Supply Current per Amplifier				2.5	3.5	mA
			•		3	4.5	mA
	Channel Separation	$f = 10Hz, V_0 = \pm 10V, R_L = 10k$			132		dB
ΔV_{OS}	Offset Voltage Match				5	225	μV
	(Note 15)	$0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 70^{\circ}\text{C}$	•		30	525	μV
		-40°C ≤ T _A ≤ 85°C	•		45	630	μV
ΔIB+	Noninverting Bias Current Match				±2	±30	nA
	(Note 15)	$0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq 70^{\circ}\text{C}$	•		±3	±55	nA
		$-40^{\circ}\text{C} \le \text{T}_{\text{A}} \le 85^{\circ}\text{C}$	•		±7	±75	nA
∆CMRR	Common Mode Rejection Match	$V_{CM} = -13.3V \text{ to } 14V$		96	120		dB
	(Notes 14, 15)		•	92	115		dB
ΔPSRR	Power Supply Rejection Match	$V_S = \pm 1.7V \text{ to } \pm 18V$		100	123		dB
	(Notes 14, 15)			96	120		dB

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 1.4V$, the input current should be limited to 25mA. If the common mode range exceeds either rail, the input current should be limited to 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1678C/LT1679C and LT1678I/LT1679I are guaranteed functional over the Operating Temperature Range of –40°C to 85°C.

Note 5: The LT1678C/LT1679C are guaranteed to meet specified performance from 0°C to 70°C. The LT1678C/LT1679C are designed, characterized and expected to meet specified performance from -40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1678I/LT1679I are guaranteed to meet specified performance from -40°C to 85°C.

Note 6: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifier; i.e., out of 100 LT1678/LT1679s, typically 60 op amps will be better than the indicated specification.

Note 7: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section.

Note 8: Noise is 100% tested at ±15V supplies.

Note 9: Slew rate is measured in $A_V = -1$; input signal is $\pm 10V$, output measured at $\pm 5V$.

Note 10: This parameter is not 100% tested.

Note 11: $V_S = 5V$ limits are guaranteed by correlation to $V_S = 3V$ and $V_S = \pm 15V$ tests.

Note 12: $V_S = 3V$ limits are guaranteed by correlation to $V_S = 5V$ and $V_S = \pm 15V$ tests.

Note 13: Guaranteed by correlation to slew rate at $V_S = \pm 15V$ and GBW at $V_S = 3V$ and $V_S = \pm 15V$ tests.

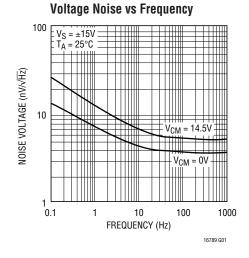
Note 14: ΔCMRR and ΔPSRR are defined as follows:

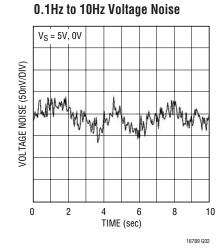
- 1. CMRR and PSRR are measured in $\mu V/V$ on the individual amplifiers.
- 2. The difference is calculated between the matching sides in μ V/V.
- 3. The result is converted to dB.

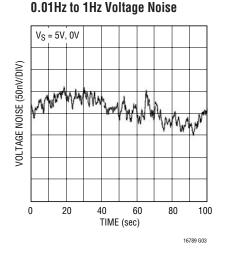
Note 15: Matching parameters are the difference between amplifiers A and B on the LT1678 and between amplifiers A and D and B and C in the LT1679

Note 16: Input range guaranteed by the common mode rejection ratio test.

TYPICAL PERFORMANCE CHARACTERISTICS



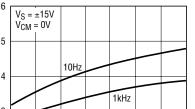




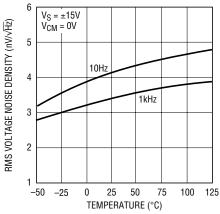
TYPICAL PERFORMANCE CHARACTERISTICS

16789 G04

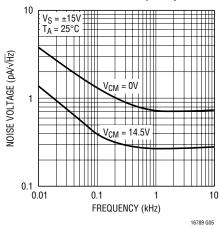
16789 G10



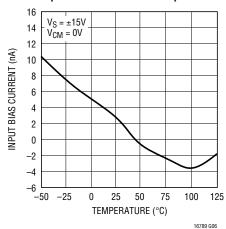
Voltage Noise vs Temperature



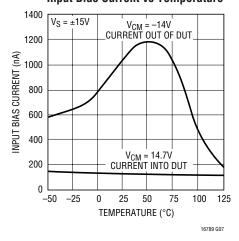
Current Noise vs Frequency



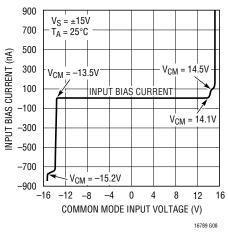
Input Bias Current vs Temperature



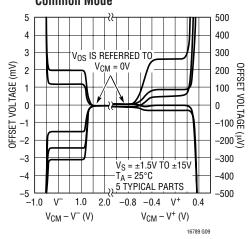
Input Bias Current vs Temperature



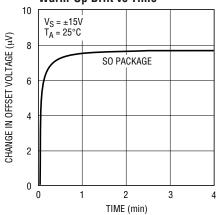
Input Bias Current Over the Common Mode Range



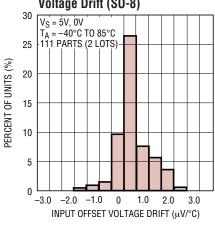
Offset Voltage Shift vs **Common Mode**



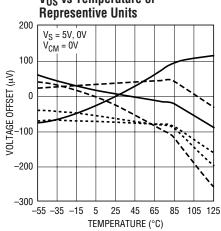
Warm-Up Drift vs Time



Distribution of Input Offset Voltage Drift (SO-8)

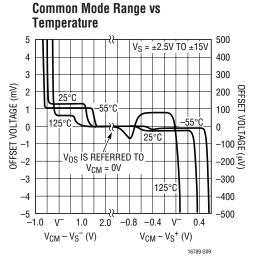


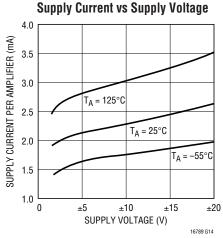
V_{OS} vs Temperature of

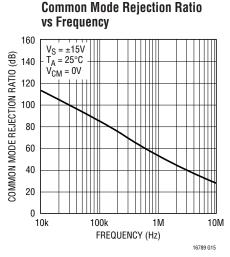


16789 G12

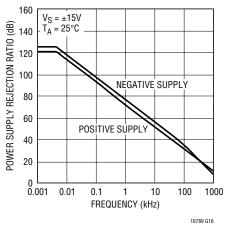
TYPICAL PERFORMANCE CHARACTERISTICS



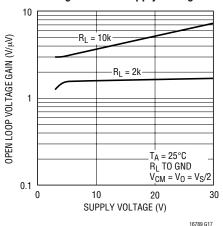




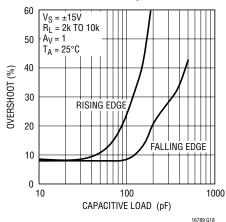




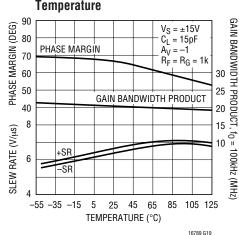




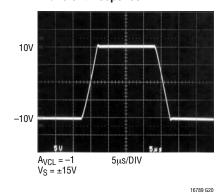
% Overshoot vs Capacitive Load



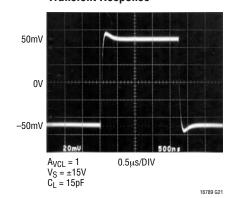
Phase Margin, Gain Bandwidth Product and Slew Rate vs Temperature



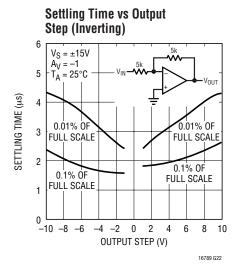
Large Signal Transient Response

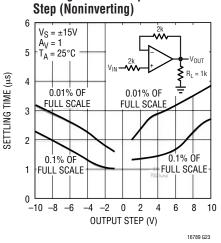


Small Signal Transient Response

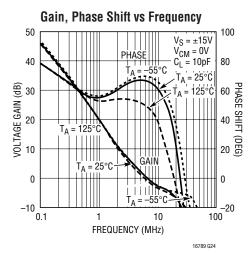


TYPICAL PERFORMANCE CHARACTERISTICS

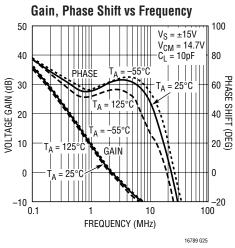


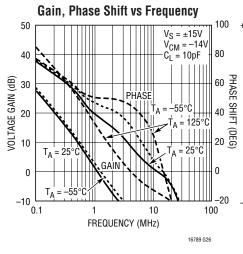


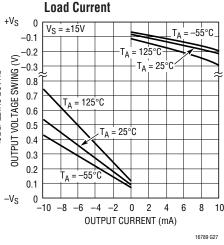
Settling Time vs Output

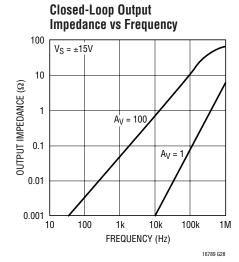


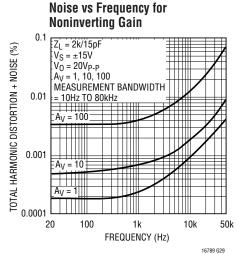
Output Voltage Swing vs



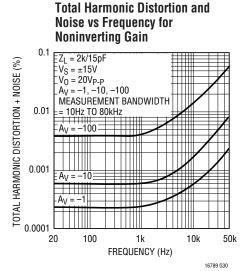








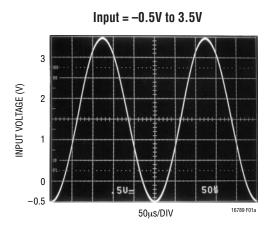
Total Harmonic Distortion and



APPLICATIONS INFORMATION

Rail-to-Rail Operation

To take full advantage of an input range that can exceed the supply, the LT1678/LT1679 are designed to eliminate phase reversal. Referring to the photographs shown in Figure 1, the LT1678/LT1679 are operating in the follower mode (A $_V$ = +1) at a single 3V supply. The output of the LT1678/LT1679 clips cleanly and recovers with no phase reversal. This has the benefit of preventing lock-up in servo systems and minimizing distortion components.



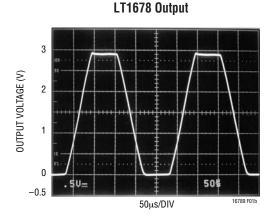


Figure 1. Voltage Follower with Input Exceeding the Supply Voltage ($V_S = 3V$)

Unity-Gain Buffer Application

When $R_F \le 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram (Figure 2).

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the

input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_F \ge 500\Omega$, the output is capable of handling the current requirements ($I_L \le 20 \text{mA}$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_F > 2k$, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_F will eliminate this problem.

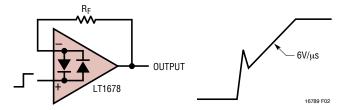


Figure 2. Pulsed Operation

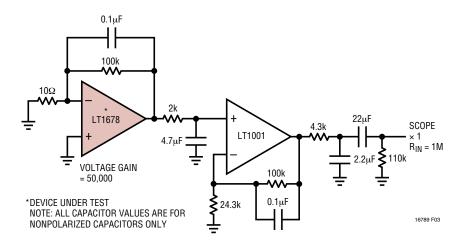
Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1678/LT1679 are measured in the test circuit shown (Figure 3). The frequency response of this noise tester (Figure 4) indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed ten seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 90nV peak-to-peak noise performance of the LT1678/LT1679 requires special test precautions:

- 1. The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically $3\mu V$ due to its chip temperature increasing $10^{\circ}C$ to $20^{\circ}C$ from the moment the power supplies are turned on. In the ten-second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
- For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

APPLICATIONS INFORMATION



90 80 70 60 50 40 30 0.01 0.1 1 10 100 FREQUENCY (Hz)

100

Figure 3. 0.1Hz to 10Hz Noise Test Circuit

Figure 4. 0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response

3. Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

Current noise is measured in the circuit shown in Figure 5 and calculated by the following formula:

$$i_{n} = \frac{\left[\left(e_{no} \right)^{2} - \left(130 \text{nV} \cdot 101 \right)^{2} \right]^{1/2}}{\left(1M\Omega \right) \left(101 \right)}$$

$$= \frac{100\Omega}{500k}$$
Figure 5.

The LT1678/LT1679 achieve their low noise, in part, by operating the input stage at $100\mu A$ versus the typical $10\mu A$ of most other op amps. Voltage noise is inversely proportional while current noise is directly proportional to the square root of the input stage current. Therefore, the LT1678/LT1679's current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency ($\approx 200 \, \text{Hz}$) minimizes current noise to some extent.

In most practical applications, however, current noise will not limit system performance. This is illustrated in the Total Noise vs Source Resistance plot (Figure 6) where: Total Noise = $[(op amp voltage noise)^2 + (resistor noise)^2 + (current noise <math>R_S)^2]^{1/2}$

Three regions can be identified as a function of source resistance:

- (i) $R_S \le 400\Omega$. Voltage noise dominates
- (ii) $400\Omega \le R_S \le 50k$ at 1kHz Resistor Noise $400\Omega \le R_S \le 8k$ at 10Hz Dominates
- (iii) $R_S > 50k$ at 1kHz Current Noise $R_S > 8k$ at 10Hz Dominates

Clearly the LT1678/LT1679 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted. In this region the LT1113 or LT1169 are better choices.

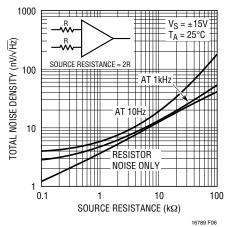


Figure 6. Total Noise vs Source Resistance

APPLICATIONS INFORMATION

Rail-to-Rail Input

The input common mode range for the LT1678/LT1679 can exceed the supplies by at least 100mV. As the common mode voltage approaches the positive rail (+ V_S – 0.7V), the tail current for the input pair (Q1, Q2) is reduced, which prevents the input pair from saturating (refer to the Simplified Schematic). The voltage drop across the load resistors R_{C1} , R_{C2} is reduced to less than 200mV, degrading the slew rate, bandwidth, voltage noise, offset voltage and input bias current (the cancellation is shut off).

When the input common mode range goes below 1.5V above the negative rail, the NPN input pair (Q1, Q2) shuts off and the PNP input pair (Q8, Q9) turns on. The offset voltage, input bias current, voltage noise and bandwidth are also degraded. The graph of Offset Voltage Shift vs Common Mode shows where the knees occur by displaying the change in offset voltage. The change-over points are temperature dependent; see the graph Common Mode Range vs Temperature.

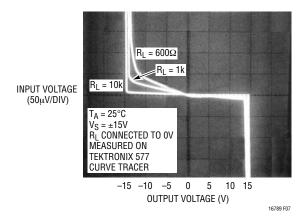


Figure 7. Voltage Gain Split Supply

Rail-to-Rail Output

The rail-to-rail output swing is achieved by using transistor collectors (Q28, Q29 referring to the Simplified Schematic) instead of customary class A-B emitter followers for the output stage. The output NPN transistor (Q29) sinks the current necessary to move the output in the negative direction. The change in Q29's base emitter voltage is reflected directly to the gain node (collectors of Q20 and Q16). For large sinking currents, the delta V_{BE} of Q29 can dominate the gain. Figure 7 shows the change in input voltage for a change in output voltage for different load resistors connected between the supplies. The gain is much higher for output voltages above ground (Q28 sources current) since the change in base emitter voltage of Q28 is attenuated by the gain in the PNP portion of the output stage. Therefore. for positive output swings (output sourcing current) there is hardly any change in input voltage for any load resistance. Highest gain and best linearity are achieved when the output is sourcing current, which is the case in single supply operation when the load is ground referenced. Figure 8 shows gains for both sinking and sourcing load currents for a worst-case load of 600Ω .

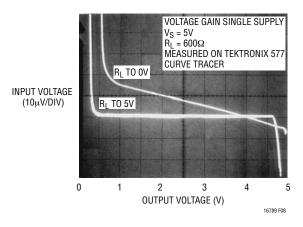
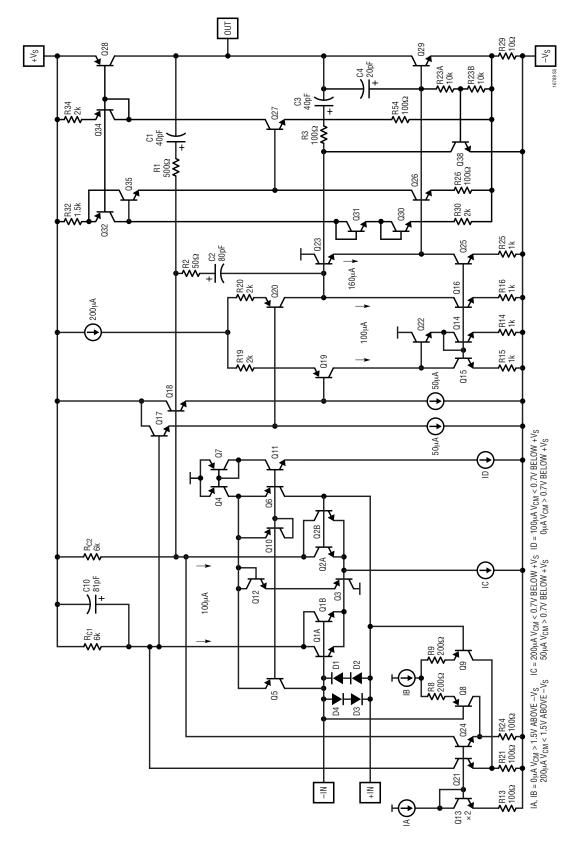


Figure 8. Voltage Gain Single Supply

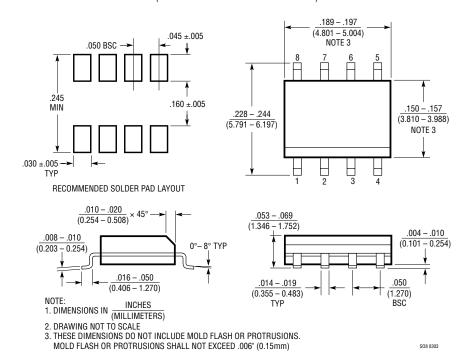
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

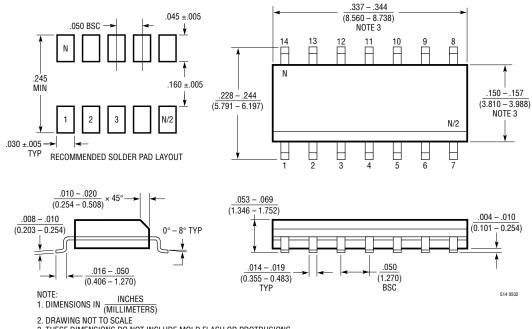
S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch)

(Reference LTC DWG # 05-08-1610)



S Package 14-Lead Plastic Small Outline (Narrow .150 Inch)

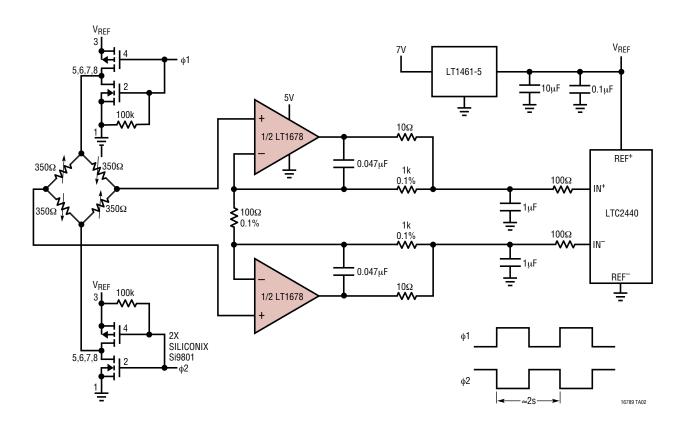
(Reference LTC DWG # 05-08-1610)



 THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATION

Bridge Reversal Eliminates 1/f Noise and Offset Drift of a Low Noise, Non-autozeroed, Bipolar Amplifier. Circuit Gives 14nV Noise Level or 19 Effective Bits Over a 10mV Span



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1028/LT1128	Ultralow Noise Precision Op Amps	Lowest Noise 0.85nV/√Hz
LT1115	Ultralow Noise, Low distortion Audio Op Amp	0.002% THD, Max Noise 1.2nV/√Hz
LT1124/LT1125	Dual/Quad Low Noise, High Speed Precision Op Amps	Similar to LT1007
LT1126/LT1127	Dual/Quad Decompensated Low Noise, High Speed Precision Op Amps	Similar to LT1037
LT1226	Low Noise, Very High Speed Op Amp	1GHz, 2.6nV/√Hz, Gain of 25 Stable
LT1498/LT1499	10MHz, 5V/µs, Dual/Quad Rail-to-Rail Input and Output Op Amps	Precision C-Load™ Stable
LT1677	Single Version of LT1678/LT1679	Rail-to-Rail 3.2nV/√Hz
LT1792	Low Noise, Precision JFET Input Op Amp	4.2nV/√Hz, 10fA/√Hz
LT1793	Low Noise, Picoampere Bias Current Op Amp	$6nV/\sqrt{Hz}$, $1fA/\sqrt{Hz}$, $I_B = 10pA$ Max
LT1806	Low Noise, 325MHz Rail-to-Rail Input and Output Op Amp	3.5nV/√Hz
LT1881/LT1882	Dual/Quad Rail-to-Rail Output Picoamp Input Precision Op Amps	C _{LOAD} to 1000pF, I _B = 200pA Max
LT1884/LT1885	Dual/Quad Rail-to-Rail Output Picoamp Input Precision Op Amps	2.2MHz Bandwidth, 1.2V/µs SR

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