

Thyristors  
logic levelBT148S-600Z  
BT148M-600Z

## GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristor in a plastic envelope, suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices feature a gate-cathode reverse breakdown voltage specification. They can be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

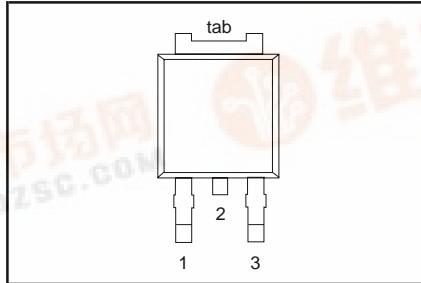
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DRM}$ , $V_{RRM}$	BT148S (or BT148M)- Repetitive peak off-state voltage	600Z	V
$I_{T(AV)}$	Average on-state current	600	
$I_{T(RMS)}$	RMS on-state current	2.5	A
$I_{TSM}$	Non-repetitive peak on-state current	4	A
		35	A

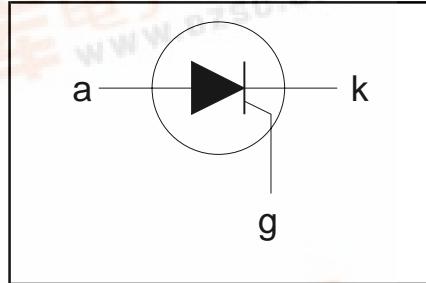
## PINNING - SOT428

PIN NUMBER	Standard S	Alternative M
1	cathode	gate
2	anode	anode
3	gate	cathode
tab	anode	anode

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DRM}$ , $V_{RRM}$	Repetitive peak off-state voltage		-	600 <sup>1</sup>	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 111^\circ C$	-	2.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	4	A
$I_{TSM}$	Non-repetitive peak on-state current	half sine wave; $T_j = 25^\circ C$ prior to surge	-		
$I^2t$	$I^2t$ for fusing	$t = 10$ ms	-	35	A
$dI_T/dt$	Repetitive rate of rise of on-state current after triggering	$t = 8.3$ ms	-	38	A
$I_{GM}$	Peak gate current	$t = 10$ ms	-	6.1	A <sup>2</sup> s
$P_{GM}$	Peak gate power	$I_{TM} = 10$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/ $\mu$ s	-	50	A/ $\mu$ s
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	2	A
$T_{stg}$	Storage temperature		-	5	W
$T_j$	Operating junction temperature		-	0.5	W
			-40	150	°C
			-	125 <sup>2</sup>	°C

<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu$ s.

<sup>2</sup> Note: Operation above 110°C may require the use of a gate to cathode resistor of 1k $\Omega$  or less.

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## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	pcb (FR4) mounted; footprint as in Fig.14	-	-	3.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	75	-	K/W

## STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{GT}$	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	15	200	$\mu\text{A}$
$I_L$	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	0.17	10	$\text{mA}$
$I_H$	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	0.10	6	$\text{mA}$
$V_T$	On-state voltage	$I_T = 5\text{ A}$	-	1.23	1.8	$\text{V}$
$V_{GR}$	Gate-cathode reverse breakdown voltage	$I_G = -20\text{ }\mu\text{A}$	14	-	-	$\text{V}$
		$I_G = -150\text{ }\mu\text{A}$	-	-	20	$\text{V}$
$V_{GT}$	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.4	1.5	$\text{V}$
		$V_D = V_{DRM(\text{max})}; I_T = 0.1\text{ A}; T_j = 110^\circ\text{C}$	0.1	0.2	-	$\text{V}$
$I_D, I_R$	Off-state leakage current	$V_D = V_{DRM(\text{max})}; V_R = V_{RRM(\text{max})}; T_j = 125^\circ\text{C}$	-	0.1	0.5	$\text{mA}$

## DYNAMIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$dV_D/dt$	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(\text{max})}; T_j = 125^\circ\text{C};$ exponential waveform; $R_{GK} = 100\ \Omega$	-	50	-	$\text{V}/\mu\text{s}$
$t_{gt}$	Gate controlled turn-on time	$I_{TM} = 10\text{ A}; V_D = V_{DRM(\text{max})}; I_G = 5\text{ mA};$ $dl_G/dt = 0.2\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$
$t_q$	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(\text{max})}; T_j = 125^\circ\text{C}; I_{TM} = 8\text{ A};$ $V_R = 10\text{ V}; dl_{TM}/dt = 10\text{ A}/\mu\text{s};$ $dV_D/dt = 2\text{ V}/\mu\text{s}; R_{GK} = 1\text{ k}\Omega$	-	100	-	$\mu\text{s}$

# Thyristors

## logic level

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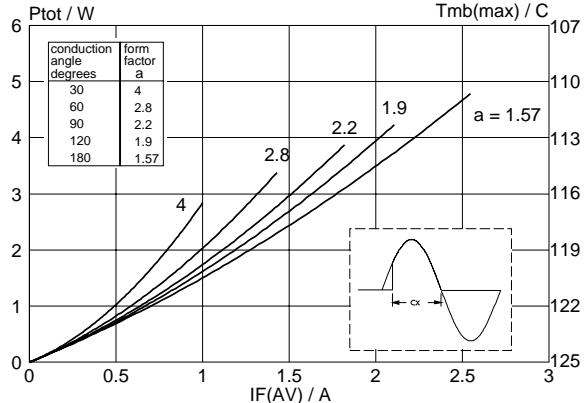


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)}/I_{T(AV)}$ .

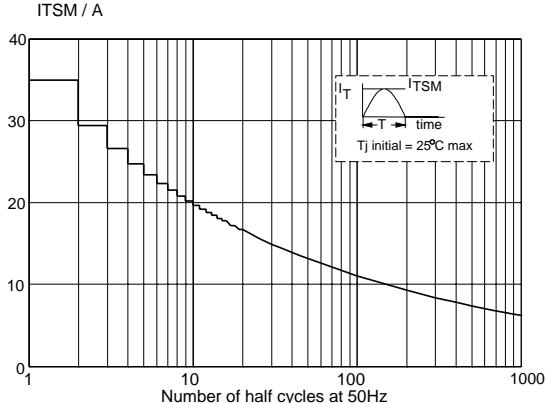


Fig.4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.

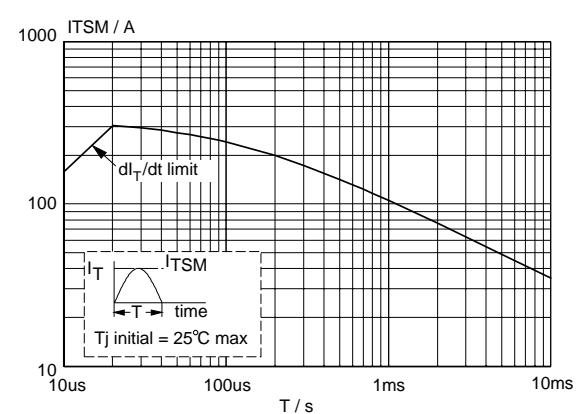


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10$  ms.

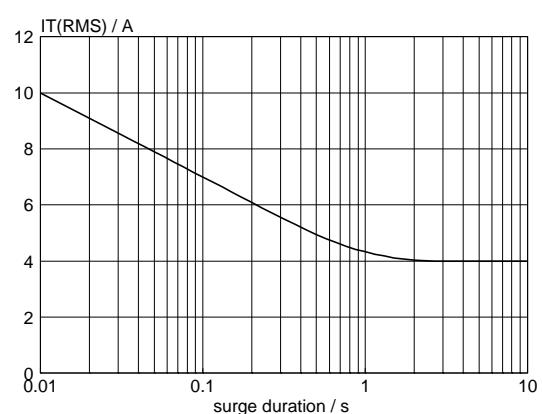


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{mb} \leq 111^\circ\text{C}$ .

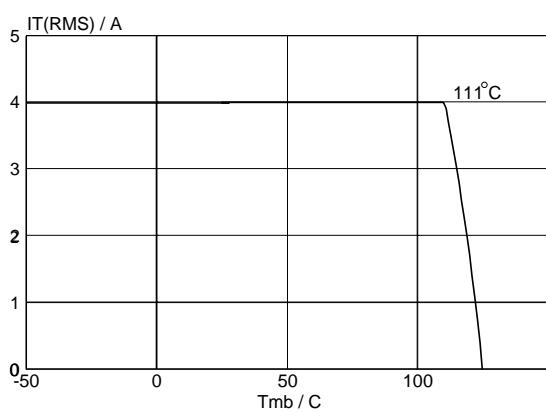


Fig.3. Maximum permissible rms current  $I_{T(RMS)}$ , versus mounting base temperature  $T_{mb}$ .

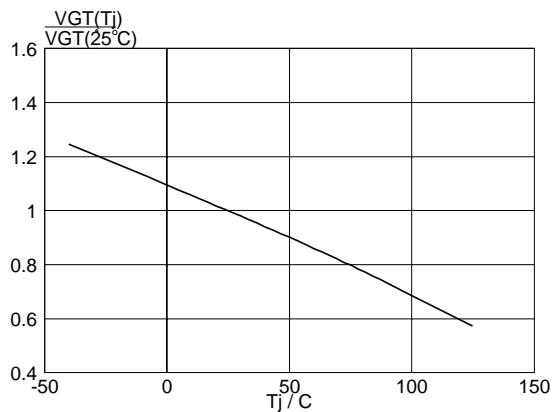


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

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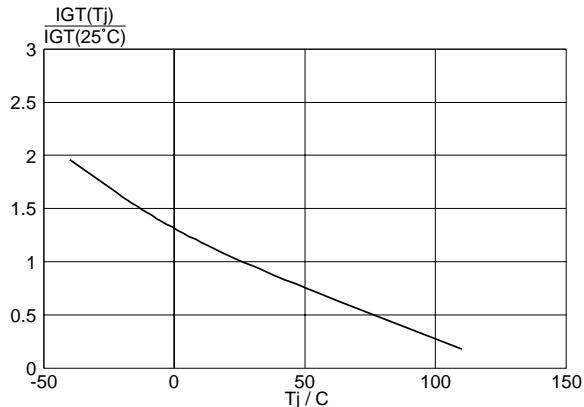


Fig.7. Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ C)$ , versus junction temperature  $T_j$ .

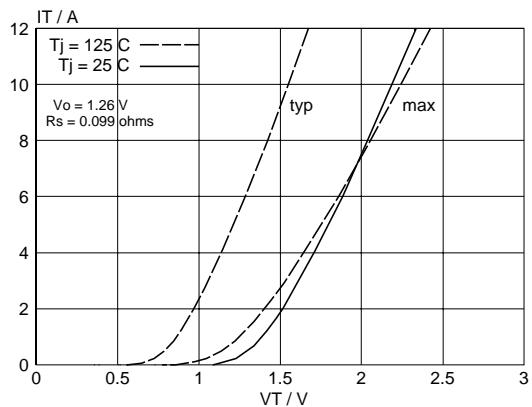


Fig.10. Typical and maximum on-state characteristic.

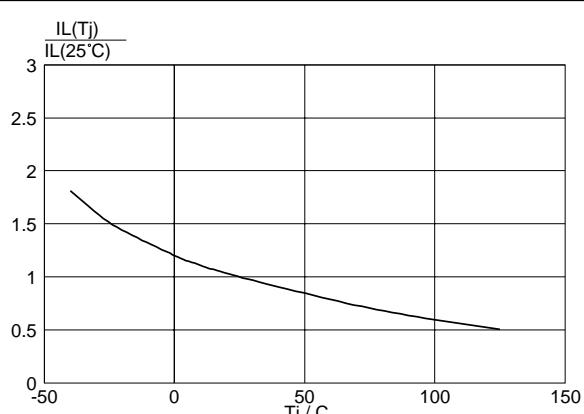


Fig.8. Normalised latching current  $I_L(T_j)/I_L(25^\circ C)$ , versus junction temperature  $T_j$ .

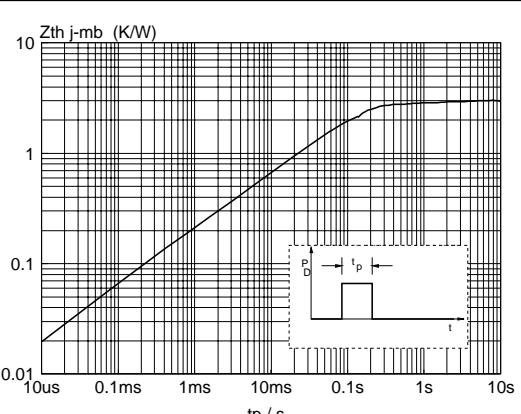


Fig.11. Transient thermal impedance  $Z_{th,j-mb}$ , versus pulse width  $t_p$ .

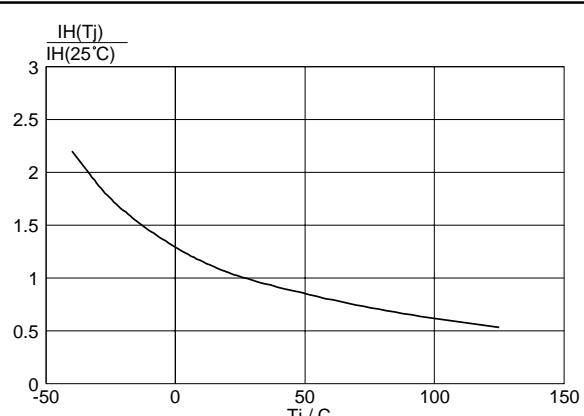


Fig.9. Normalised holding current  $I_H(T_j)/I_H(25^\circ C)$ , versus junction temperature  $T_j$ .

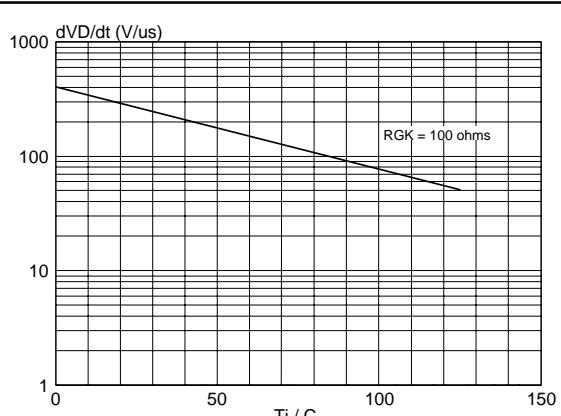


Fig.12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$ .

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## MECHANICAL DATA

Dimensions in mm

Net Mass: 1.1 g

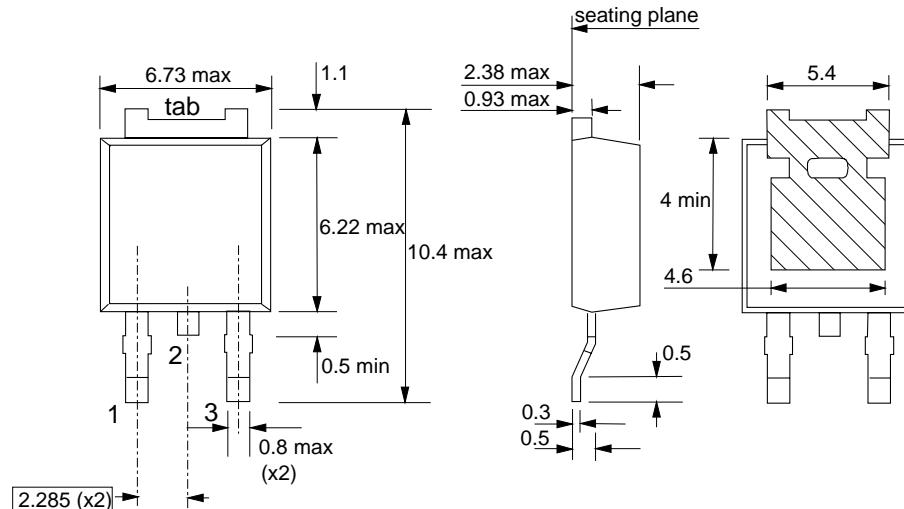


Fig.13. SOT428 : centre pin connected to tab.

## MOUNTING INSTRUCTIONS

Dimensions in mm

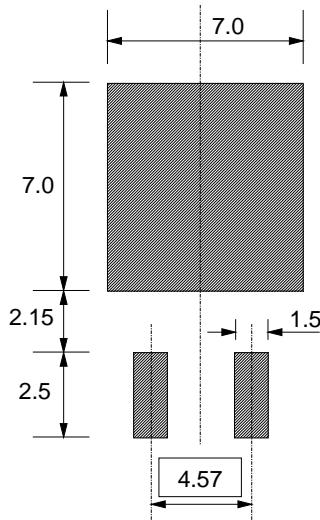


Fig.14. SOT428 : minimum pad sizes for surface mounting.

## Notes

1. Plastic meets UL94 V0 at 1/8".

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<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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