M58MR064C
M58MR064D

64 Mbit (4Mb x16, Mux I/O, Dual Bank, Burst)
1.8V Supply Flash Memory

- SUPPLY VOLTAGE
  - V_{DD} = V_{DDQ} = 1.65V to 2.0V for Program, Erase and Read
  - V_{PP} = 12V for fast Program (optional)
- MULTIPLEXED ADDRESS/DATA
- SYNCHRONOUS / ASYNCHRONOUS READ
  - Burst mode Read: 54MHz
  - Page mode Read (4 Words Page)
  - Random Access: 100ns
- PROGRAMMING TIME
  - 10µs by Word typical
  - Two or four words programming option
- MEMORY BLOCKS
  - Dual Bank Memory Array: 16/48 Mbit
  - Parameter Blocks (Top or Bottom location)
- DUAL OPERATIONS
  - Read within one Bank while Program or Erase within the other
  - No delay between Read and Write operations
- PROTECTION/SECURITY
  - All Blocks protected at Power-up
  - Any combination of Blocks can be protected
  - 64 bit unique device identifier
  - 64 bit user programmable OTP cells
  - One parameter block permanently lockable
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M58MR064C: 88DCh
  - Bottom Device Code, M58MR064D: 88DDh

TFBGA48 (ZC)
10 x 4 ball array

Figure 1. Logic Diagram

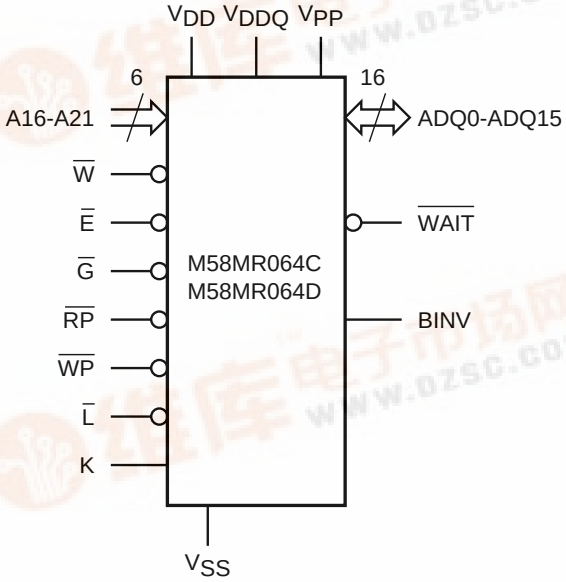
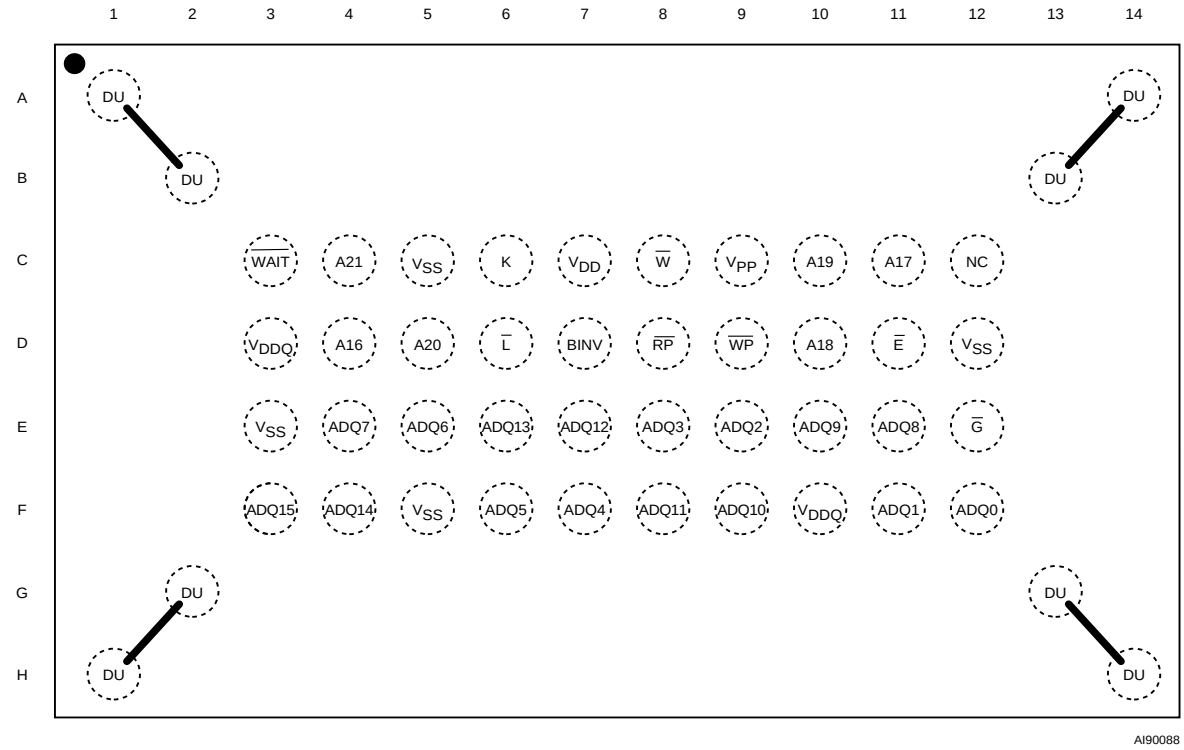


Figure 2. TFBGA Connections (Top view through package)



DESCRIPTION

The M58MR064 is a 64 Mbit non-volatile Flash memory that may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.65V to 2.0V V_{DD} supply for the circuitry. For Program and Erase operations the necessary high voltages are generated internally. The device supports synchronous burst read and asynchronous read from all the blocks of the memory array; at power-up the device is configured for page mode read. In synchronous burst mode, a new data is output at each clock cycle for frequencies up to 54MHz.

The array matrix organization allows each block to be erased and reprogrammed without affecting other blocks. All blocks are protected against programming and erase at Power-up.

Blocks can be unprotected to make changes in the application and then re-protected.

A parameter block "Security block" can be permanently protected against programming and erasing in order to increase the data security. An optional 12V V_{PP} power supply is provided to speed up the program phase at costumer production. An internal command interface (C.I.) decodes the instructions to access/modify the memory content. The program/erase controller (P/E.C.) automatically executes the algorithms taking care of the timings necessary for program and erase operations. Two status registers indicate the state of each bank.

Instructions for Read Array, Read Electronic Signature, Read Status Register, Clear Status Register, Write Read Configuration Register, Program, Block Erase, Bank Erase, Program Suspend, Program Resume, Erase Suspend, Erase Resume, Block Protect, Block Unprotect, Block Locking, Protection Program, CFI Query, are written to the memory through a Command Interface (C.I.) using standard micro-processor write timings.

The memory is offered in TFBGA48, 0.5 mm ball pitch packages and it is supplied with all the bits erased (set to '1').

Table 1. Signal Names

A16-A21	Address Inputs
ADQ0-ADQ15	Data Input/Outputs or Address Inputs, Command Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power-down
$\overline{WP}$	Write Protect
K	Burst Clock
$\overline{L}$	Latch Enable
$\overline{WAIT}$	Wait Data in Burst Mode
BINV	Bus Invert
V_{DD}	Supply Voltage
V_{DDQ}	Supply Voltage for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
DU	Don't Use as Internally Connected
NC	Not Connected Internally

Organization

The M58MR064 is organized as 4Mb by 16 bits. The first sixteen address lines are multiplexed with the Data Input/Output signals on the multiplexed address/data bus ADQ0-ADQ15. The remaining address lines A16-A21 are the MSB addresses.

Chip Enable $\overline{E}$, Output Enable $\overline{G}$ and Write Enable $\overline{W}$ inputs provide memory control.

The clock K input synchronizes the memory to the microprocessor during burst read.

Reset $\overline{RP}$ is used to reset all the memory circuitry and to set the chip in power-down mode if a proper setting of the Read Configuration Register enables this function.

$\overline{WAIT}$ output indicates to the microprocessor the status of the memory during the burst mode operations.

Memory Blocks

The device features asymmetrically blocked architecture. M58MR064 has an array of 135 blocks and is divided into two banks A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible into Bank B or vice versa. Only one bank at the time is allowed to be in program or erase mode. It is possible to perform burst reads that cross bank boundaries.

The memory features an erase suspend allowing reading or programming in another block. Once suspended the erase can be resumed. Program can be suspended to read data in another block and then resumed. The Bank Size and sectorization are summarized in Table 3. Parameter Blocks are located at the top of the memory address space for the M58MR064C, and at the bottom for the M58MR064D. The memory maps are shown in Figure 3.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–40 to 125	°C
T_{STG}	Storage Temperature	–55 to 155	°C
V_{IO} (3)	Input or Output Voltage	–0.5 to V_{DDQ}+0.5	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.5 to 2.7	V
V_{PP}	Program Voltage	–0.5 to 13	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

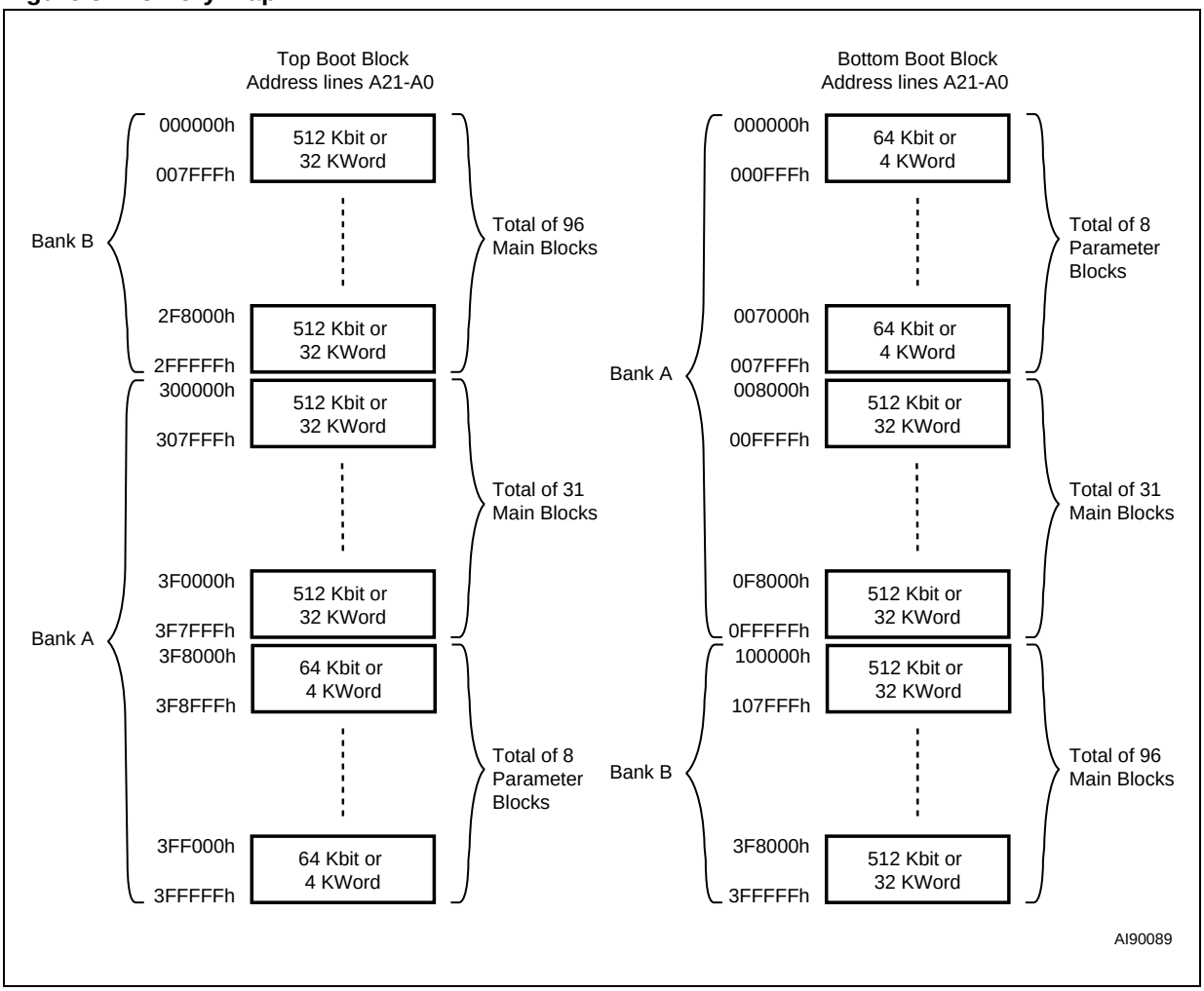
The architecture includes a 128 bits Protection register that is divided into two 64-bits segments. In the first one is written a unique device number, while the second one is programmable by the user. The user programmable segment can be permanently protected programming the bit 1 of the Protection Lock Register (see protection register and Security Block). The parameter block (# 0) is a security block. It can be permanently protected by the user programming the bit 2 of the Protection Lock Register.

Block protection against Program or Erase provides additional data security. All blocks are protected and unlocked at Power-up. Instructions are provided to protect or un-protect any block in the application. A second register locks the protection status while WP is low (see Block Locking description).

Table 3. Bank Size and Sectorization

	Bank Size	Parameter Blocks	Main Blocks
Bank A	16 Mbit	8 blocks of 4 KWord	31 blocks of 32 KWord
Bank B	48 Mbit	-	96 blocks of 32 KWord

Figure 3. Memory Map



SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs or Data Input/Output (ADQ0-ADQ15). When Chip Enable $\overline{E}$ is at V_{IL} and Output Enable $\overline{G}$ is at V_{IH} the multiplexed address/data bus is used to input addresses for the memory array, data to be programmed in the memory array or commands to be written to the C.I. The address inputs for the memory array are latched on the rising edge of Latch Enable L. The address latch is transparent when L is at V_{IL}. In synchronous operations the address is also latched on the first rising/falling edge of K (depending on clock configuration) when L is low. Both input data and commands are latched on the rising edge of Write Enable $\overline{W}$. When Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are at V_{IL} the address/data bus outputs data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Block Protection status the Read Configuration Register status, the protection register or the Status Register. The address/data bus is high impedance when the chip is deselected, Output Enable $\overline{G}$ is at V_{IH}, or $\overline{RP}$ is at V_{IL}.

Address Inputs (A16-A21). The five MSB addresses of the memory array are latched on the rising edge of Latch Enable L. In synchronous operation these inputs are also latched on the first rising/falling edge of K (depending on clock configuration) when L is low.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ at V_{IH} deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at V_{IL}.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. When $\overline{G}$ is at V_{IH} the outputs are High impedance.

Write Enable ($\overline{W}$). This input controls writing to the Command Register and Data latches. Data are latched on the rising edge of $\overline{W}$.

Write Protect ($\overline{WP}$). This input gives an additional hardware protection level against program or erase when pulled at V_{IL}, as described in the Block Lock instruction description.

Reset/Power-down Input ($\overline{RP}$). The $\overline{RP}$ input provides hardware reset of the memory, and/or Power-down functions, depending on the Read Configuration Register status. Reset/Power-down of the memory is achieved by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPH}. When the reset pulse is given, the memory will recover from Power-down (when enabled) in a minimum of t_{PHEL}, t_{PHLL} or t_{PHWL} (see Table 31 and Figure 15) after the rising edge of $\overline{RP}$. Exit from Reset/Power-down changes the contents of the Read Configuration Register bits 14 and 15, setting the memory in asynchronous page mode read and power save function disabled. All blocks are protected and unlocked after a Reset/Power-down.

Latch Enable ($\overline{L}$). $\overline{L}$ latches the address bits ADQ0-ADQ15 and A16-A21 on its rising edge. The address latch is transparent when $\overline{L}$ is at V_{IL} and it is inhibited when $\overline{L}$ is at V_{IH}.

Clock (K). The clock input synchronizes the memory to the micro controller during burst mode read operation; the address is latched on a K edge (rising or falling, according to the configuration settings) when L is at V_{IL}. K is don't care during asynchronous page mode read and in write operations.

Wait ($\overline{WAIT}$). $\overline{WAIT}$ is an output signal used during burst mode read, indicating whether the data on the output bus are valid or a wait state must be inserted. This output is high impedance when $\overline{E}$ or $\overline{G}$ are high or $\overline{RP}$ is at V_{IL}, and can be configured to be active during the wait cycle or one clock cycle in advance.

Bus Invert (BINV). BINV is an input/output signal used to reduce the amount of power needed to switch the external address/data bus. The power saving is achieved by inverting the data output on ADQ0-ADQ15 every time this gives an advantage in terms of number of toggling bits. In burst mode read, each new data output from the memory is compared with the previous data. If the number of transitions required on the data bus is in excess of 8, the data is inverted and the BINV signal will be driven by the memory at V_{OH} to inform the receiving system that data must be inverted before any further processing. By doing so, the actual transitions on the data bus will be less than 8.

In a similar way, when a command is given, BINV may be driven by the system at V_{IH} to inform the memory that the data input must be inverted.

Like the other input/output pins, BINV is high impedance when the chip is deselected, output enable $\overline{G}$ is at V_{IH} or $\overline{RP}$ is at V_{IL}; when used as an input, BINV must follow the same set-up and hold timings of the data inputs.

V_{DD} and V_{DDQ} Supply Voltage (1.65V to 2.0V). V_{DD} is the main power supply for all operations (Read, Program and Erase). V_{DDQ} is the supply voltage for Input and Output.

V_{PP} Program Supply Voltage (12V). V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin; if V_{PP} is kept in a low voltage range (0 to 2V) V_{PP} is seen as a control input, and the current absorption is limited to 5µA (0.2µA typical). In this case with $V_{PP} = V_{IL}$ we obtain an absolute protection against program or erase; with $V_{PP} = V_{PP1}$ these functions are enabled (see Table 26). V_{PP} value is only sampled during program or erase write cycles; a change in its value after the operation has been started does not have any effect and program or erase are carried on regularly. If V_{PP} is used in the 11.4V to 12.6V range (V_{PPH}) then the pin acts as a power supply (see Table 26). This supply voltage must remain stable as long as program or erase are running. In read mode the current sunk is less then 0.5mA, while during program and erase operations the current may increase up to 10mA.

V_{SS} Ground. V_{SS} is the reference for all the voltage measurements.

DEVICE OPERATIONS

The following operations can be performed using the appropriate bus cycles: Address Latch, Read Array (Random, and Page Modes), Write command, Output Disable, Standby, reset/Power-down and Block Locking. See Table 4.

Address Latch. In asynchronous operation, the address is latched on the rising edge of L input. In burst mode the address is latched either on the rising edge of L or on the first rising/falling edge of K (depending on configuration settings) when L is low.

Read. Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the CFI, the Block Protection Status, the Read Configuration Register status and the Protection Register.

Read operation of the Memory Array may be performed in asynchronous page mode or synchronous burst mode. In asynchronous page mode data is internally read and stored in a page buffer. The page has a size of 4 words and is addressed by ADQ0 and ADQ1 address inputs.

According to the device configuration the following Read operations: Electronic Signature - Status Register - CFI - Block Protection Status - Read Configuration Register Status - Protection Register must be accessed as asynchronous read or as single synchronous read (see Figure 4).

Table 4. User Bus Operations (1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{L}$	$\overline{RP}$	$\overline{WP}$	ADQ15-ADQ0
Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IL} (rising edge)	V_{IH}	V_{IH}	Address Input
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	X	V_{IH}	X	Hi-Z
Reset / Power-down	X	X	X	X	V_{IL}	X	Hi-Z
Block Locking	V_{IL}	X	X	X	V_{IH}	V_{IL}	X

Note: 1. X = Don't care.

Table 5. Read Electronic Signature (AS and Read CFI instructions) (1)

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	ADQ1 (3)	ADQ0 (3)	Other Address (2)	ADQ15-0
Manufacturer Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	EA (2)	0020h
Device Code	M58MR064C	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	EA (2)	88DCh
	M58MR064D	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	EA (2)	88DDh

Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. EA means Electronic Signature Address (see Read Electronic Signature)
3. Value during address latch.

Table 6. Read Block Protection (AS and Read CFI instructions) (1)

Block Status	$\overline{E}$	$\overline{G}$	$\overline{W}$	ADQ1 (3)	ADQ0 (3)	Other Address	ADQ15-0
Protected and unlocked	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	BA (4)	0001
Unprotected and unlocked	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	BA (4)	0000
Protected and locked	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	BA (4)	0003
Unprotected and locked (2)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	BA (4)	0002

Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. A locked block can be unprotected only with $\overline{WP}$ at V_{IH}.
3. Value during address latch.
4. BA means Block Address. First cycle command address should indicate the bank of the block address.

Table 7. Read Protection Register (RSIG and RCFI Instruction) (1)

Word	$\overline{E}$	$\overline{G}$	$\overline{W}$	A21-17	ADQ15-8	ADQ7-0	ADQ15-8	ADQ7-3	ADQ2	ADQ1	ADQ0
Lock	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	80h	00h	00000B	Security prot.data	OTP prot.data	0
Unique ID 0	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	81h	ID data	ID data	ID data	ID data	ID data
Unique ID 1	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	82h	ID data	ID data	ID data	ID data	ID data
Unique ID 2	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	83h	ID data	ID data	ID data	ID data	ID data
Unique ID 3	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	84h	ID data	ID data	ID data	ID data	ID data
OTP 0	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	85h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 1	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	86h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 2	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	87h	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 3	V_{IL}	V_{IL}	V_{IH}	X (2)	X (2)	88h	OTP data	OTP data	OTP data	OTP data	OTP data

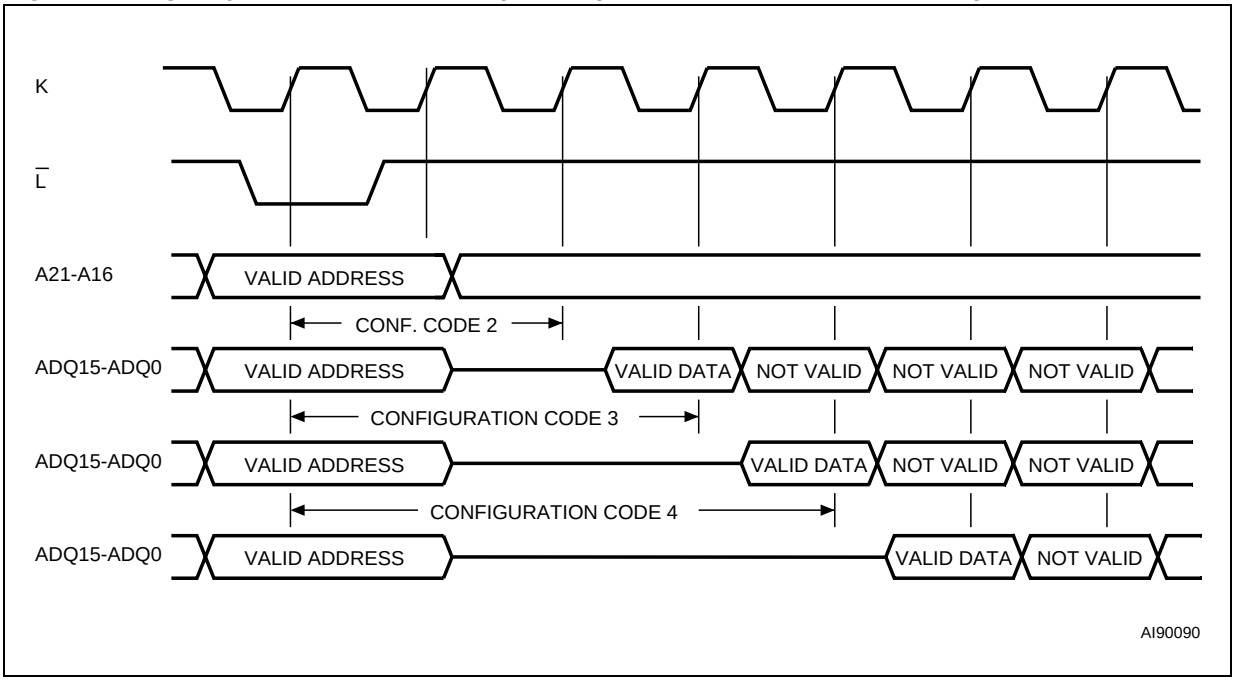
Note: 1. Addresses are latched on the rising edge of $\overline{L}$ input.
2. X = Don't care.

Table 8. Dual Bank Operations (1, 2, 3)

Status of one bank	Commands allowed in the other bank							
	Read Array	Read Status	Read ID/CFI	Program	Erase/ Erase Resume	Program Suspend	Erase Suspend	Protect Unprotect
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Reading	–	–	–	–	–	–	–	–
Programming	Yes	Yes	Yes	–	–	–	–	Yes
Erasing	Yes	Yes	Yes	–	–	–	–	Yes
Program Suspended	Yes	Yes	Yes	–	–	–	–	Yes
Erase Suspended	Yes	Yes	Yes	Yes	–	Yes	–	Yes

Note: 1. For detailed description of command see Table 33 and 34.
2. There is a status register for each bank; status register indicates bank state, not P/E.C. status.
3. Command must be written to an address within the block targeted by that command.

Figure 4. Single Synchronous Read Sequence (RSIG, RCFI, RSR instructions)



Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be at V_{IL} in order to read the output of the memory.

Read array is the default state of the device when exiting power down or after power up.

Burst Read. The device also supports a burst read. In this mode a burst sequence is started at the first clock edge (rising or falling according to configuration settings) after the falling edge of L. After a configurable delay of 2 to 5 clock cycles a new data is output at each clock cycle. The burst sequence may be configured for linear or interleaved order and for a length of 4, 8 words or for continuous burst mode. Wrap and no-wrap modes are also supported.

A $\overline{WAIT}$ signal may be asserted to indicate to the system that an output delay will occur. This delay will depend on the starting address of the burst sequence; the worst case delay will occur when the sequence is crossing a 64 word boundary and the starting address was at the end of a four word boundary. See the Write Read Configuration Register (CR) Instruction for more details on all the possible settings for the synchronous burst read (see Table 14). It is possible to perform burst read across bank boundary (all banks in read array mode).

Write. Write operations are used to give Instruction Commands to the memory or to latch Input Data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are at V_{IL} with Output Enable $\overline{G}$ at V_{IH}. Addresses are latched on the rising edge of L. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first. Noise pulses of less than 5ns typical on $\overline{E}$, $\overline{W}$ and $\overline{G}$ signals do not start a write cycle. Write operations are asynchronous and clock is ignored during write.

Dual Bank Operations. The Dual Bank allows to run different operations simultaneously in the two banks. It is possible to read array data from one bank while the other is programming, erasing or reading any data (CFI, status register or electronic signature).

Read and write cycles can be initiated for simultaneous operations in different banks without any delay. Only one bank at a time is allowed to be in program or erase mode, while the other must be in one of the read modes (see Table 8).

Commands must be written to an address within the block targeted by that command.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is at V_{IH} with Write Enable $\overline{W}$ at V_{IH}.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is at V_{IH} and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Automatic Standby. When in Read mode, after 150ns of bus inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo-standby mode where consumption is reduced to the CMOS standby value, while outputs still drive the bus. The automatic standby feature is not available when the device is configured for synchronous burst mode.

Table 9. Identifier Codes

Code		Address (h)	Data (h)
Manufacturer Code		Bank Address + 00	0020
Device Code	Top	Bank Address + 01	88DC
	Bottom	Bank Address + 01	88DD
Block Protection	Protected and Unlocked	Bank Address + 02	0001
	Unprotected and Unlocked		0000
	Protected and Locked		0003
	Unprotected and Locked		0002
Die Revision Code		Bank Address + 03	DRC (1)
Read Configuration Register		Bank Address + 05	CR (1)
Lock Protection Register		Bank Address + 80	LPR (1)
Protection Register		Bank Address + 81 Bank Address + 88	PR (1)

Note: 1. DRC means Die Revision Code.
CR means Read Configuration Register.
LPR means Lock Protection Register.
PR means Unique Device Number and User Programmable OTP.

Reset/Power-down. The memory is in Power-down when the Read Configuration Register is set for Power-down and RP is at V_{IL}. The power consumption is reduced to the Power-down level, and Outputs are in high impedance, independent of the Chip Enable E, Output Enable G or Write Enable W inputs. The memory is in reset when the Read Configuration Register is set for Reset and RP is at VIL. The power consumption is the same of the standby and the outputs are in high impedance. After a Reset/Power down the device defaults to read array mode, the status register is set to 80h and the read configuration register defaults to asynchronous read.

Block Locking. Any combination of blocks can be temporarily protected against Program or Erase by setting the lock register and pulling WP to V_{IL}. The following summarizes the locking operation. All blocks are protected on power-up. They can then be unprotected or protected with the Unprotect and Protect commands. The Lock command protects a block and prevents it from being unlocked when WP = 0. When WP = 1, Lock is overridden. Lock is cleared only when the device is reset or powered-down (see Protect instruction).

INSTRUCTIONS AND COMMANDS

Eighteen instructions are available (see Tables 10 and 11) to perform Read Memory Array, Read Status Register, Read Electronic Signature, CFI Query, Block Erase, Bank Erase, Program, Tetra Word Program, Double Word Program, Clear Status Register, Program/Erase Suspend, Program/Erase Resume, Block Protect, Block Unprotect, Block Lock, Protection Register Program, Read Configuration Register and Lock Protection Program.

Status Register output may be read at any time, during programming or erase, to monitor the progress of the operation.

An internal Command Interface (C.I.) decodes the instructions while an internal Program/Erase Controller (P/E.C.) handles all timing and verifies the correct execution of the Program and Erase instructions. P/E.C. provides a Status Register whose bits indicate operation and exit status of the internal algorithms. The Command Interface is reset to Read Array when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequence must be followed exactly. Any invalid combination of commands will reset the device to Read Array.

Read (RD)

The Read instruction consists of one write cycle (refer to Device Operations section) and places the addressed bank in Read Array mode. When a device reset occurs, the memory is in Read Array as default. A read array command will be ignored while a bank is programming or erasing. However in the other bank a read array command will be accepted.

Read Status Register (RSR)

A bank's Status Register indicates when a program or erase operation is complete and the success or failure of operation itself. Issue a Read Status Register Instruction (70h) to read the Status Register content of the addressed bank. The status of the other bank is not affected by the command. The Read Status Register instruction may be issued at any time, also when a Program/Erase operation is ongoing. The following Read operations output the content of the Status Register of the addressed bank. The Status Register is latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to V_{IH}. Either $\overline{E}$ or $\overline{G}$ must be toggled to update the latched data.

Read Electronic Signature (RSIG)

The Read Electronic Signature instruction consists of one write cycle (refer to Device Operations section) giving the command 90h to an address within the bank A. A subsequent read in the address of bank A will output the Manufacturer Code, the Device Code, the protection Status of Blocks of bank A, the Die Revision Code, the Protection Register, or the Read Configuration Register (see Table 9).

If the first write cycle of Read Electronic Signature instruction is issued to an address within the bank B, a subsequent read in an address of bank B will output the protection Status of Blocks of bank B. The status of the other bank is not affected by the command (see Table 8).

See Tables 5, 6, 7 and 8 for the valid address. The Electronic Signature can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of M58MR064C and M58MR064D.

Table 10. Commands

Hex Code	Command
00h	Invalid Reset
01h	Protect Confirm
03h	Write Read Configuration Register Confirm
10h	Alternative Program Set-up
20h	Block Erase Set-up
2Fh	Lock Confirm
30h	Double Word Program Set-up
40h	Program Set-up
50h	Clear Status Register
55h	Tetra Word Program Set-up
60h	Protect Set-up and Write Read Configuration Register
70h	Read Status Register
80h	Bank Erase Set-up
90h	Read Electronic Signature
98h	CFI Query
B0h	Program/Erase Suspend
C0h	Protection Program and Lock Protection Program
D0h	Program/Erase Resume, Erase Confirm or Unprotect Confirm
FFh	Read Array

Table 11. Instructions

		Instruction	Cyc.	Operation	Address (1,2)	Data (3)	Operation	Address (1,2)	Data (3)
READ	RD	Read Memory Array	1+	Write	BKA	FFh	Read (1)	Read Address	Data
	RSR	Read Status Register	1+	Write	BKA	70h	Read (1)	BKA	Status Register
	RSIG	Read Electronic Signature	1+	Write	EA	90h	Read (1)	EA	ED
	RCFI	Read CFI	1+	Write	CA	98h	Read (1)	CA	CD
	CLRS (5)	Clear Status Register	1	Write	BKA	50h			
PROGRAM/ERASE	EE	Block Erase	2	Write	BA	20h	Write	BA	D0h
	BE	Bank Erase	2	Write	BKA	80h	Write	BKA	D0h
	PG	Program	2	Write	WA	40h or 10h	Write	WA	WD
	DPG	Double Word Program	3	Write	WA1	30h	Write	WA1	WD1
							Write	WA2	WD2
	TPG	Tetra Word Program	5	Write	WA1	55h	Write	WA1	WD1
							Write	WA2	WD2
							Write	WA3	WD3
							Write	WA4	WD4
	PES	Program Erase Suspend	1	Write	BKA	B0h			
	PER	Program Erase Resume	1	Write	BKA	D0h			
PROTECT	BP	Block Protect	2	Write	BA	60h	Write	BA	01h
	BU	Block Unprotect	2	Write	BA	60h	Write	BA	D0h
	BL	Block Lock	2	Write	BA	60h	Write	BA	2Fh
CONFIGURATION	PRP	Protection Register Program	2	Write	PA	C0h	Write	PA	PD
	LPRP	Lock Protection Register Program	2	Write	LPA	C0h	Write	LPA	LPD
	CR	Write Read Configuration Register	2	Write	RCA	60h	Write	RCA	03h

Note: 1. First cycle command address should be the same as the operation's target address. The first cycle of the RD, RSR, RSIG or RCFI instruction is followed by read operations in the bank array or special register. Any number of read cycles can occur after one command cycle.
2. BKA means Address within the bank;
BA means Block Address;
EA means Electronic Signature Address;
CA means Common Flash Interface Address;
WA means Word Address;
PA means Protection Register Address (see Table 7);
LPA means Lock Protection Register Address (see Table 7);
RCA means Read Configuration Register Address.
3. PD means Protection Data;
CD means Common Flash Interface Data;
ED means Electronic Signature Data;
WD means Data to be programmed at the address location WA;
LPD means Lock protection Register Data
4. WA1, WA2, WA3 and WA4 must be consecutive address differing only for address bits A1-A0.
5. Read cycle after e CLSR instruction will output the memory array.

CFI Query (RCFI)

The CFI Query Mode is associated to bank A. The address of the first write cycle must be within the bank A. The status of the other bank is not affected by the command (see Table 8). Writing 98h the device enters the Common Flash Interface Query mode. Next read operations in the bank A will read the CFI data. Write a read instruction to return to Read mode (refer to the Common Flash Interface section).

Clear Status Register (CLSR)

The Clear Status Register uses a single write operation, which resets bits b1, b3, b4 e b5 of the status register. The Clear Status Register is executed writing the command 50h independently of the applied V_{PP} voltage. After executing this command the device returns to read array mode. The Clear Status Register command clears only the status register of the addressed bank.

Block Erase (EE)

Block erasure sets all the bits within the selected block to '1'. One block at a time can be erased. It is not necessary to pre-program the block as the P/E.C. will do it automatically before erasing. This instruction use two writes cycles. The first command written is the Block Erase Set up command 20h. The second command is the Erase Confirm command D0h. An address within the block to be erased should be given to the memory during the two cycles command. If the second command given is not an erase confirm, the status register bits b4 and b5 are set and the instruction aborts.

After writing the command, the device outputs status register data when any address within the bank is read. At the end of the operation the bank will remain in read status register until a read array command is written.

Status Register bit b7 is '0' while the erasure is in progress and '1' when it has completed. After completion the Status Register bit b5 returns '1' if there has been an Erase Failure. Status register bit b1 returns '1' if the user is attempting to erase a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}. Erase aborts if RP turns to V_{IL}. As data integrity cannot be guaranteed when the erase operation is aborted, the erase must be repeated (see Table 12). A Clear Status Register instruction must be issued to reset b1, b3, b4 and b5 of the Status Register. During the execution of the erase by the P/E.C., the bank with the block in erase accepts only the RSR (Read Status Register) and PES (Program/Erase Suspend) instructions. See figure 19 for Erase Flowchart and Pseudo Code.

Bank Erase (BE)

Bank erase sets all the bits within the selected bank to '1'. It is not necessary to pre-program the block as the P/E.C. will do it automatically before erasing.

This instruction uses two writes cycles. The first command written is the Bank Erase set-up command 80h. The second command is the Erase Confirm command D0h. An address within the bank to be erased should be given to the memory during the two cycles command. See the Block Erase command section for status register bit details.

Table 12. Status Register Bits

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/ECS Status	1	Ready	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits b4 or b5 for Program or Erase Success.
			0	Busy	
ESS	6	Erase Suspend Status	1	Suspended	On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			0	In Progress or Completed	
ES	5	Erase Status	1	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			0	Erase Success	
PS	4	Program Status	1	Program Error	PS bit set to '1' if the P/E.C. has failed to program a word.
			0	Program Success	
VPPS	3	V_{PP} Status	1	V_{PP} Invalid, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPLK} when a Program or Erase instruction is executed. V_{PP} is sampled only at the beginning of the erase/program operation.
			0	V_{PP} OK	
PSS	2	Program Suspend Status	1	Suspended	On a program Suspend instruction P/ECS and PSS bits are set to '1'. PSS remains '1' until a Program Resume Instruction is given.
			0	In Progress or Completed	
BPS	1	Block Protection Status	1	Program/Erase on protected Block, Abort	BPS bit is set to '1' if a Program or Erase operation has been attempted on a protected block.
			0	No operation to protected blocks	
	0	Reserved			

Note: Logic level '1' is V_{IH} and '0' is V_{IL}.

Program (PG)

The Program instruction programs the array on a word-by-word basis. The first command must be given to the target block and only one partition can be programmed at a time; the other partition must be in one of the read modes or in the erase suspended mode (see Table 8).

This instruction uses two write cycles. The first command written is the Program Set-up command 40h (or 10h). A second write operation latches the Address and the Data to be written and starts the P/E.C.

Read operations in the targeted bank output the Status Register content after the programming has started.

The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure (see Table 12). Status register bit b1 returns '1' if the user is attempting to program a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}. Any attempt to write a '1' to an already programmed bit will result in a program fail (status register bit b4 set) if $V_{PP} = V_{PPH}$ and will be ignored if $V_{PP} = V_{PP1}$.

Programming aborts if $\overline{RP}$ goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed. A Clear Status Register instruction must be issued to reset b5, b4, b3 and b1 of the Status Register.

During the execution of the program by the P/E.C., the bank in programming accepts only the RSR (Read Status Register) and PES (Program/Erase Suspend) instructions. See Figure 16 for Program Flowchart and Pseudo Code.

Figure 5. Security Block Memory Map

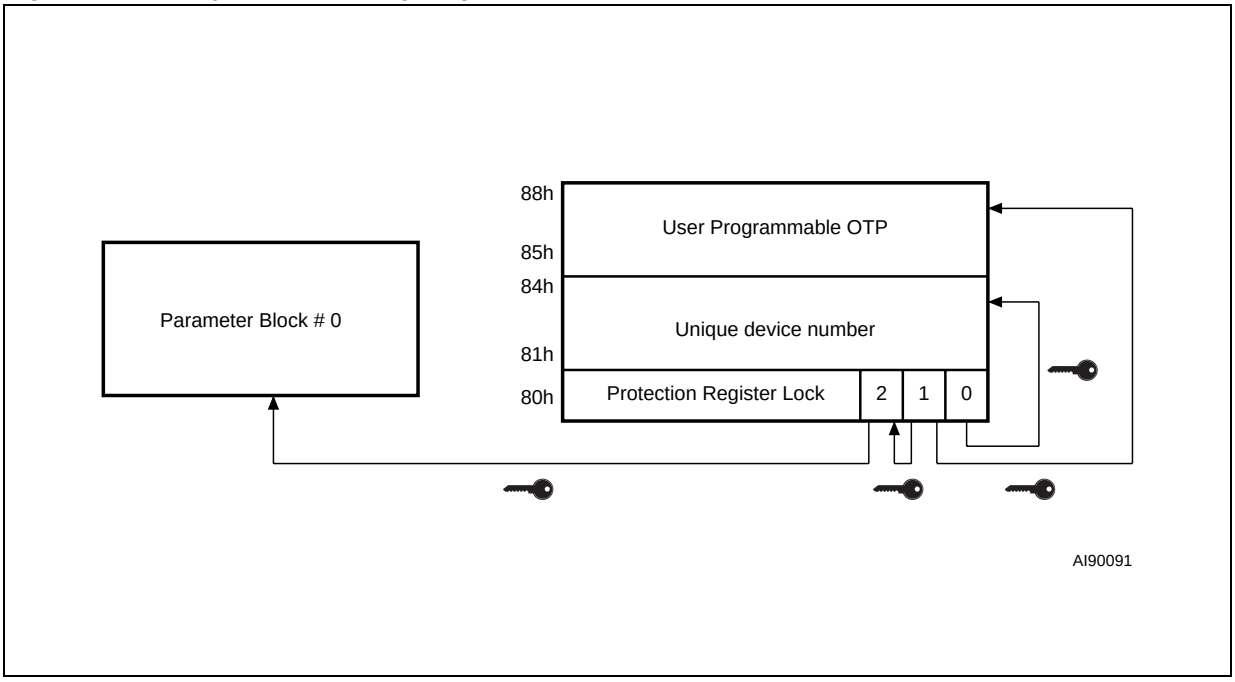


Table 13. Protection States (1)

Current State (2) (WP, DQ1, DQ0)	Program/Erase Allowed	Next State After Event (3)			
		Protect	Unprotect	Lock	WP transition
100	Yes	101	100	111	000
101	No	101	100	111	001
110	Yes	111	110	111	011
111	No	111	110	111	011
000	Yes	001	000	011	100
001	No	001	000	011	101
011	No	011	011	011	111 or 110 (4)

Note: 1. All blocks are protected at power-up, so the default configuration is 001 or 101 according to $\overline{WP}$ status.
2. Current state and Next state gives the protection status of a block. The protection status is defined by the write protect in and by DQ1 (= 1 for a locked block) and DQ0 (= 1 for a protected block) as read in the Read Electronic Signature instruction with A1 = V_{IH} and A0 = V_{IL}.
3. Next state is the protection status of a block after a Protect or Unprotect or Lock command has been issued or after $\overline{WP}$ has changed its logic value.
4. A $\overline{WP}$ transition to V_{IH} on a locked block will restore the previous DQ0 value, giving a 111 or 110.

Double Word Program (DPG)

This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel. The first command must be given to the target block and only one partition can be programmed at a time; the other partition must be in one of the read modes or in the erase suspended mode (see Table 8).

The two words must differ only for the address A0. Programming should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH} but result could be uncertain. These instruction uses three write cycles. The first command written is the Double Word Program Set-Up command 30h. A second write operation latches the Address and the Data of the first word to be written, the third write operation latches the Address and the Data of the second word to be written and starts the P/E.C. (see Table 11).

Read operations in the targeted bank output the Status Register content after the programming has started. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status register bit b1 returns '1' if the user is attempting to program a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}. Any attempt to write a '1' to an already programmed bit will result in a program fail (status register bit b4 set). (See Table 12).

Programming aborts if $\overline{RP}$ goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be erased and reprogrammed. A Clear Status Register instruction must be issued to reset b5, b4, b3 and b1 of the Status Register. During the execution of the program by the P/E.C., the bank in programming accepts only the RSR (Read Status Register) instruction. See Figure 17 for Double Word Program Flowchart and Pseudo code.

Tetra Word Program (TPG)

This feature is offered to improve the programming throughput, writing a page of four adjacent words in parallel. The first command must be given to the target block and only one partition can be programmed at a time; the other partition must be in one of the read modes or in the erase suspended mode (see Table 8).

The four words must differ only for the addresses A0 and A1. Programming should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH} but result could be uncertain. These instruction uses five write cycles. The first command written is the Tetra Word Program Set-Up command 55h. A second write operation latches the Address and the Data of the first word to be written, the third write operation latches the Address and the Data of the second word to be written, the fourth write operation latches the Address and the Data of the third word to be written, the fifth write operation latches the Address and the Data of the fourth word to be written and starts the P/E.C. (see Table 11).

Read operations in the targeted bank output the Status Register content after the programming has started. The Status Register bit b7 returns '0' while the programming is in progress and '1' when it has completed. After completion the Status register bit b4 returns '1' if there has been a Program Failure. Status register bit b1 returns '1' if the user is attempting to program a protected block. Status Register bit b3 returns a '1' if V_{PP} is below V_{PPLK}. Any attempt to write a '1' to an already programmed bit will result in a program fail (status register bit b4 set). (See Table 12).

Programming aborts if $\overline{RP}$ goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be erased and reprogrammed. A Clear Status Register instruction must be issued to reset b5, b4, b3 and b1 of the Status Register. During the execution of the program by the P/E.C., the bank in programming accepts only the RSR (Read Status Register) instruction. See Figure 17 for Tetra Word Program Flowchart and Pseudo code.

Erase Suspend/Resume (PES/PER)

The Erase Suspend freezes, after a certain latency period (within 25us), the erase operation and allows read in another block within the targeted bank or program in the other block.

This instruction uses one write cycle B0h and the address should be within the bank with the block in erase (see Table 11). The device continues to output status register data after the erase suspend is issued. The status register bit b7 and bit b6 are set to '1' then the erase operation has been suspended. Bit b6 is set to '0' in case the erase is completed or in progress (see Table 12).

The valid commands while erase is suspended are: Program/Erase Resume, Program, Read Memory Array, Read Status Register, Read Electronic Signature, CFI Query, Block Protect, Block Unprotect and Block Lock. The user can protect the Block being erased issuing the Block Protect or Block Lock commands.

During a block erase suspend, the device goes into standby mode by taking $\overline{E}$ to V_{IH}, which reduces active current draw. Erase is aborted if $\overline{RP}$ turns to V_{IL}.

If an Erase Suspend instruction was previously executed, the erase operation may be resumed by issuing the command D0h using an address within the suspended bank. The status register bit b6 and bit b7 are cleared when erase resumes and read

operations output the status register after the erase is resumed. Block erase cannot resume until program operations initiated during block erase suspend have completed. It is also possible to nest suspends as follows: suspend erase in the first partition, start programming in the second or in the same partition, suspend programming and then read from the second or the same partition. The suggested flowchart for erase suspend/resume features of the memory is shown from Figure 20.

Program Suspend/Resume (PES/PER)

Program suspend is accepted only during the Program instruction execution. When a Program Suspend command is written to the C.I., the P/E.C. freezes the Program operation.

Program Resume (PER) continues the Program operation. Program Suspend (PES) consists of writing the command B0h and the address should be within the bank with the word in programming (see Table 11).

The Status Register bit b2 is set to '1' (within 5µs) when the program has been suspended. Bit b2 is set to '0' in case the program is completed or in progress (see Table 12).

The valid commands while program is suspended are: Program/Erase Resume, Read Array, Read Status Register, Read Electronic Signature, CFI Query. During program suspend mode, the device goes in standby mode by taking $\overline{E}$ to V_{IH}. This reduces active current consumption. Program is aborted if $\overline{RP}$ turns to V_{IL}.

If a Program Suspend instruction was previously executed, the Program operation may be resumed by issuing the command D0h using an address within the suspended bank (see Table 11). The status register bit b2 and bit b7 are cleared when program resumes and read operations output the status register after the erase is resumed (see Table 12). The suggested flowchart for program suspend/resume features of the memory is shown from Figure 18.

Block Protect (BP)

The BP instruction use two write cycles. The first command written is the protection set-up 60h. The second command is block Protect command 01h, written to an address within the block to be protected (see Table 11). If the second command is not recognized by the C.I the bit 4 and bit 5 of the status register will be set to indicate a wrong sequence of commands (see Table 12). To read the status register write the RSR command.

Block Unprotect (BU)

The instruction use two write cycles. The first command written is the protection set-up 60h. The second command is block Unprotect command D0h, written to an address within the block to be protected (see Table 11). If the second command is not recognized by the C.I the bit 4 and bit 5 of the status register will be set to indicate a wrong sequence of commands (see Table 12). To read the status register write the RSR command.

Block Lock (BL)

The instruction use two write cycles. The first command written is the protection set-up 60h. The second command is block Lock command 2Fh, written to an address within the block to be protected (see Table 11). If the second command is not recognized by the C.I the bit 4 and bit 5 of the status register will be set to indicate a wrong sequence of commands. To read the status register write the RSR command (see Table 12).

BLOCK PROTECTION

The M58MR064C/M58MR064D provide a flexible protection of all the memory providing the protection, un-protection and locking of any blocks. All blocks are protected at power-up. Each block of the array has two levels of protection against programming or erasing operation. The first level is set by the Block Protect instruction; a protected block cannot be programmed or erased until a Block Unprotect instruction is given for that block. A second level of protection is set by the Block Lock instruction, and requires the use of the $\overline{WP}$ pin, according to the following scheme:

– when $\overline{WP}$ is at V_{IH}, the Lock status is overridden and all blocks can be protected or unprotected;
– when $\overline{WP}$ is at V_{IL}, Lock status is enabled; the locked blocks are protected, regardless of their previous protect state, and protection status cannot be changed. Blocks that are not locked can still change their protection status;
– the lock status is cleared for all blocks at power up.

The protection and lock status can be monitored for each block using the Read Electronic Signature (RSIG) instruction. Protected blocks will output a '1' on DQ0 and locked blocks will output a '1' in DQ1 (see Table 13).

PROTECTION REGISTER PROGRAM (PRP) and LOCK PROTECTION REGISTER PROGRAM (LPRP)

The M58MR064C/M58MR064D features a 128-bit protection register and a security Block in order to increase the protection of a system design. The Protection Register is divided in two 64-bit segments. The first segment (81h to 84h) is a unique device number, while the second one (85h to 88h) can be programmed by the user. When shipped the user programmable segment is read at '1'. It can be only programmed at '0'.

The user programmable segment can be protected writing the bit 1 of the Protection Lock register (80h). The bit 1 protects also the bit 2 of the Protection Lock Register.

The M58MR064C/M58MR064D feature a security Block. The security Block is located at 3FF000-3FFFFF (M58MR064C) or at 000000-000FFF (M58MR064D) of the device. This block can be permanently protected by the user programming the bit 2 of the Protection Lock Register (see Figure 5).

The protection Register and the Protection Lock Register can be read using the RSIG and RCFI instructions. A subsequent read in the address starting from 80h to 88h, the user will retrieve respectively the Protection Lock register, the unique device number segment and the OTP user programmable register segment (see Table 23).

WRITE READ CONFIGURATION REGISTER (CR).

This instruction uses two Coded Cycles, the first write cycle is the write Read Configuration Register set-up 60h, the second write cycle is write Read Configuration Register confirm 03h both to Read Configuration Register address (see Table 11).

This instruction writes the contents of address bits ADQ15-ADQ0 to bits CR15-CR0 of the Read Configuration Register (A21-A16 are don't care). At Power-up the Read Configuration Register is set to asynchronous Read mode, Power-down disabled and bus invert (power save function) disabled. A description of the effects of each configuration bit is given in Table 14.

Read mode (CR15). The device supports an asynchronous page mode and a synchronous burst mode. In asynchronous page mode, the default at power-up, data is internally read and stored in a buffer of 4 words selected by ADQ0 and ADQ1 address inputs. In synchronous burst mode, the device latches the starting address and then outputs a sequence of data that depends on the Read Configuration Register settings (see Figures 10, 11 and 12).

Synchronous burst mode is supported in both parameter and main blocks; it is also possible to perform burst mode read across the banks.

Bus Invert configuration (CR14). This register bit is used to enable the BINV pin functionality. BINV functionality depends upon configuration bits CR14 and CR15 (see Table 14 for configuration bits definition) as shown in Table 15. As output pin BINV is active only when enabled (CR14 = 1) in Read Array burst mode (CR15 = 0). As input pin BINV is active only when enabled (CR14 = 1). BINV is ignored when ADQ0-ADQ15 lines are used as address inputs (addresses must not be inverted).

X-Latency (CR13-CR11). These configuration bits define the number of clock cycles elapsing from L going low to valid data available in burst mode (see Figure 6). The correspondence between X-Latency settings and the maximum sustainable frequency must be calculated taking into account some system parameters.

Two conditions must be satisfied:

– $(n + 2)\, t_K \geq t_{ACC} + t_{QVK\_CPU} + t_{AVK\_CPU}$
– $t_K > t_{KQV} + t_{QVK\_CPU}$

where "n" is the chosen X-Latency configuration code, t_K is the clock period, t_{AVK_CPU} is the address setup time guaranteed by the system CPU, and t_{QVK_CPU} is the data setup time required by the system CPU.

Table 14. Read Configuration Register (AS and Read CFI instructions) (1)

Configuration Register	Function
CR15	Read mode 0 = Synchronous Burst mode read 1 = Asynchronous Page mode read (default)
CR14	Bus Invert configuration (power save) 0 = disabled (default) 1 = enabled
CR13-CR11	X-Latency 010 = 2 clock latency 011 = 3 clock latency 100 = 4 clock latency 101 = 5 clock latency 111 = reserved Other configurations reserved
CR10	Power-down configuration 0 = power-down disabled (default) 1 = power-down enabled
CR9	Reserved
CR8	Wait configuration 0 = WAIT is active during wait state 1 = WAIT is active one data cycle before wait state (default)
CR7	Burst order configuration 0 = Interleaved 1 = Linear (default)
CR6	Clock configuration 0 = Address latched and data output on the falling clock edge 1 = Address latched and data output on the rising clock edge (default)
CR5-CR4	Reserved
CR3	Burst Wrap 0 = burst wrap within burst length set by CR2-CR0 1 = Don't wrap accesses within burst length set by CR2-CR0 (default)
CR2-CR0	Burst length 001 = 4 word burst length 010 = 8 word burst length 111 = Continuous burst mode (requires CR7 = 1)

Note: 1. The RCR can be read via the RSIG command (90h). Bank A Address + 05h contains the RCR data. See Table 9.
2. All the bits in the RCR are set to default on device power-up or reset.

Table 15. BINV Configuration Bits

CR15	CR14	BINV	
		IN	OUT
0	0	X	0
0	1	Active	Active
1	0	X	0
1	1	Active	0

Power-down configuration (CR10). The $\overline{RP}$ pin may be configured to give very low power consumption when driven low (power-down state). In power-down the I_{CC} supply current is reduced to a typical figure of I_{CC2}; if this function is disabled (default at power-up) the $\overline{RP}$ pin causes only a reset of the device and the supply current is the stand-by value. The recovery time after a $\overline{RP}$ pulse is significantly longer when power-down is enabled (see Table 31).

Wait configuration (CR8). In burst mode WAIT indicates whether the data on the output bus are valid or a wait state must be inserted. The configuration bit determines if WAIT will be asserted one clock cycle before the wait state or during the wait state (see Figure 7). WAIT is asserted during a continuous burst and also during a 4 or 8 burst length if no-wrap configuration is selected.

Burst order configuration (CR7) and Burst Wrap configuration (CR3). See Table 16 for burst order and length.

Clock configuration (CR6). In burst mode determines if address is latched and data is output on the rising or falling edge of the clock.

Burst length (CR2-CR0). In burst mode determines the number of words output by the memory. It is possible to have 4 words, 8 words or a continuous burst mode, in which all the words are read sequentially. In continuous burst mode the burst sequence can cross the end of each of the two banks (all banks in read array mode). In continuous burst mode or in 4, 8 words no-wrap it may happen that the memory will stop the data output flow for a few clock cycles; this event is signaled by WAIT going low until the output flow is resumed. The initial address determines if the output delay will occur as well as its duration. If the starting address is aligned to a four words boundary no wait states will be needed. If the starting address is shifted by 1,2 or 3 positions from the four word boundary, WAIT will be asserted for 1, 2 or 3 clock cycles when the burst sequence is crossing the first 64 word boundary. WAIT will be asserted only once during a continuous burst access. See also Table 16.

Figure 6. X-Latency Configuration Sequence

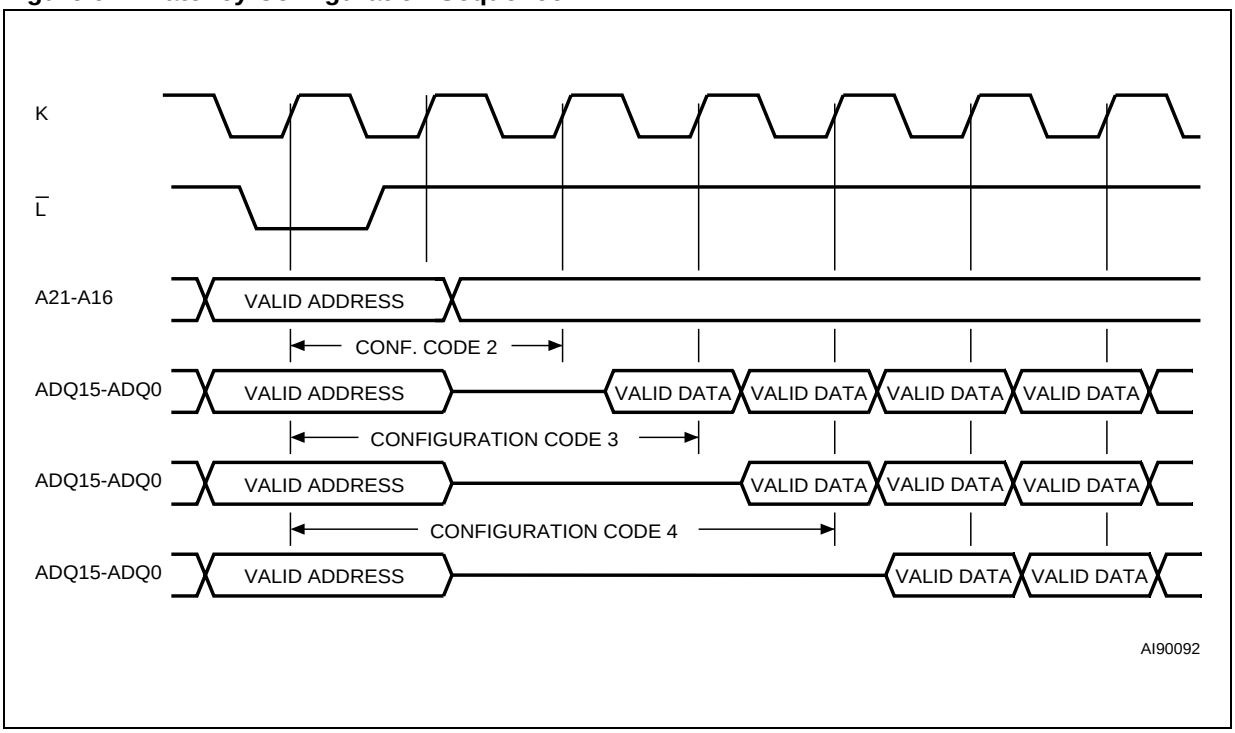


Figure 7. Wait Configuration Sequence

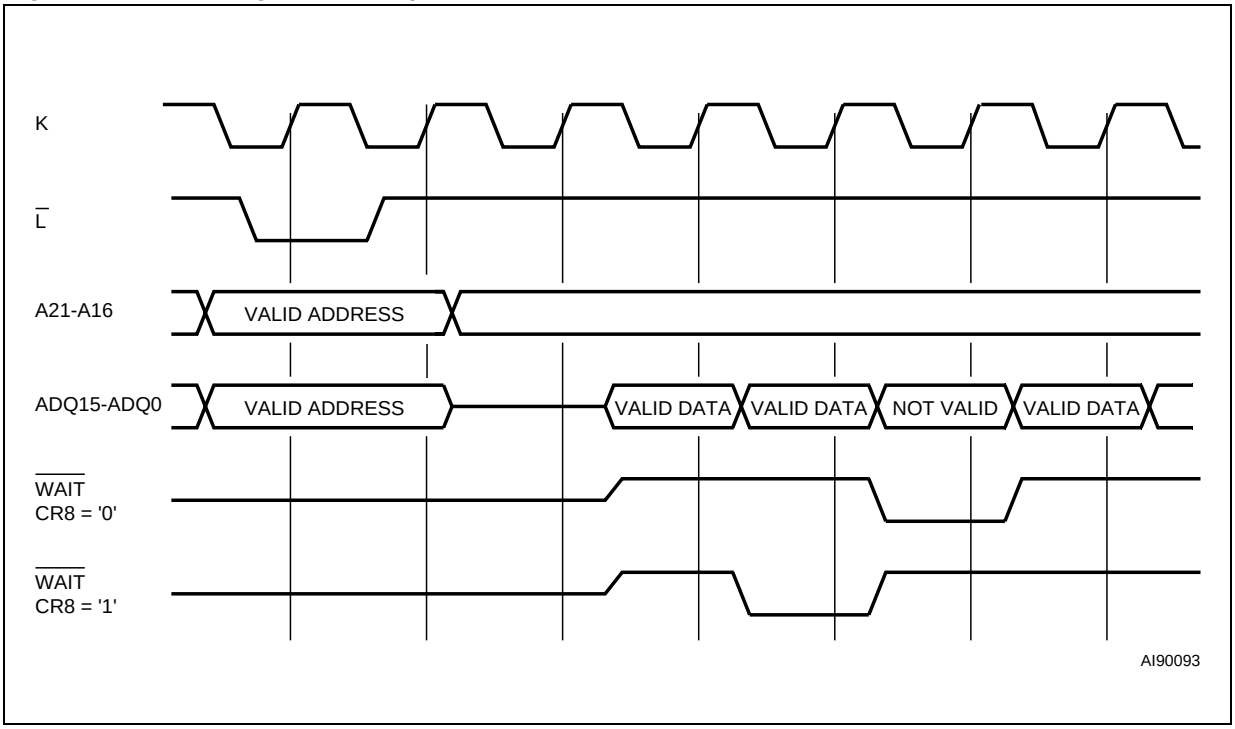


Table 16. Burst Order and Length Configuration

Mode	Starting Address	4 Words		8 Words		Continuous Burst
		Linear	Interleaved	Linear	Interleaved	
Wrap	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6...
	1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7...
	2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8...
	3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9...
	...					
	7	7-4-5-6	7-6-5-4	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13...
	...					
	60					60-61-62-63-64-65-66...
	61					61-62-63-WAIT-64-65-66...
	62					62-63-WAIT-WAIT-64-65-66...
	63					63-WAIT-WAIT-WAIT-64-65-66...
		Linear	**Interleaved**	**Linear**	**Interleaved**	
No-wrap	0	0-1-2-3		0-1-2-3-4-5-6-7		0-1-2-3-4-5-6...
	1	1-2-3-4		1-2-3-4-5-6-7-8		1-2-3-4-5-6-7...
	2	2-3-4-5		2-3-4-5-6-7-8-9...		2-3-4-5-6-7-8...
	3	3-4-5-6		3-4-5-6-7-8-9-10		3-4-5-6-7-8-9...
	...					
	7	7-8-9-10		7-8-9-10-11-12-13-14		7-8-9-10-11-12-13...
	...					
	60	60-61-62-63		60-61-62-63-64-65-66-67		60-61-62-63-64-65-66...
	61	61-62-63-WAIT-64		61-62-63-WAIT-64-65-66-67-68		61-62-63-WAIT-64-65-66...
	62	62-63-WAIT-WAIT-64-65		62-63-WAIT-WAIT-64-65-66-67-68-69		62-63-WAIT-WAIT-64-65-66...
	63	63-WAIT-WAIT-WAIT-64-65-66		63-WAIT-WAIT-WAIT-64-65-66-67-68-69-70		63-WAIT-WAIT-WAIT-64-65-66...

POWER CONSUMPTION

Power-down

The memory provides Reset/Power-down control input $\overline{RP}$. The Power-down function can be activated only if the relevant Read Configuration Register bit is set to '1'. In this case, when the $\overline{RP}$ signal is pulled at V_{SS} the supply current drops to typically I_{CC2} (see Table 26), the memory is deselected and the outputs are in high impedance. If $\overline{RP}$ is pulled to V_{SS} during a Program or Erase operation, this operation is aborted and the memory content is no longer valid (see Reset/Power-down input description).

Power-up

The memory Command Interface is reset on Power-up to Read Array. Either $\overline{E}$ or $\overline{W}$ must be tied to V_{IH} during Power-up to allow maximum security and the possibility to write a command on the first rising edge of $\overline{W}$. At Power-up the device is configured as:

– Page mode: (CR15 = 1)

– Power-down disabled: (CR10 = 0)

– BINV disabled: (CR14 = 0).

All blocks are protected and unlocked.

V_{DD}, V_{DDQ} and V_{PP} are independent power supplies and can be biased in any order.

Supply Rails

Normal precautions must be taken for supply voltage decoupling; each device in a system should have the V_{DD} rails decoupled with a 0.1µF capacitor close to the V_{DD}, V_{DDQ} and V_{SS} pins. The PCB trace widths should be sufficient to carry the required V_{DD} program and erase currents.

COMMON FLASH INTERFACE (CFI)

The Common Flash Interface (CFI) specification is a JEDEC approved, standardized data structure that can be read from the Flash memory device. CFI allows a system software to query the flash device to determine various electrical and timing parameters, density information and functions supported by the device. CFI allows the system to easily interface to the Flash memory, to learn about its features and parameters, enabling the software to configure itself when necessary.

Tables 17, 18, 19, 20, 21, 22 and 23 show the address used to retrieve each data. The CFI data structure gives information on the device, such as the sectorization, the command set and some electrical specifications. The CFI data structure contains also a security area; in this section, a 64 bit unique security number is written, starting at address 81h. This area can be accessed only in read mode and there are no ways of changing the code after it has been written by ST. Write a read instruction to return to Read mode (see Table 11). Refer to the CFI Query instruction to understand how the M58MR064 enters the CFI Query mode.

Table 17. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)
80h	Security Code Area	Lock Protection Register Unique device Number and User Programmable OTP

Note: The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in Tables 18, 19, 20, 21, 22 and 23. Query data are always presented on the lowest order data outputs.

Table 18. CFI Query Identification String

Offset	Sub-section Name	Description	Value
00h	0020h	Manufacturer Code	ST
01h	88DCh 88DDh	Device Code	Top Bottom
02h	reserved	Reserved	
03h	DRC (1)	Die Revision Code	
04h-0Fh	reserved	Reserved	
10h	0051h	Query Unique ASCII String "QRY"	"Q"
11h	0052h		"R"
12h	0059h		"Y"
13h	0003h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	
14h	0000h		
15h	offset = P = 0039h	Address for Primary Algorithm extended Query table (see Table 20)	p = 39h
16h	0000h		
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (note: 0000h means none exists)	NA
18h	0000h		
19h	value = A = 0000h	Address for Alternate Algorithm extended Query table (0000h means none exists)	NA
1Ah	0000h		

Note: Query data are always presented on the lowest - order data outputs (ADQ0-ADQ7) only. ADQ8-ADQ15 are '0'.
1. DRC means Die Revision Code.

Table 19. CFI Query System Interface Information

Offset	Data	Description	Value
1Bh	0017h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts	1.7V
1Ch	0020h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts	2V
1Dh	0017h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts	1.7V
1Eh	00C0h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts	12V
1Fh	0004h	Typical timeout per single byte/word program = 2^n µs	16µs
20h	0004h	Typical timeout for tetra word program = 2^n µs	16µs
21h	000Ah	Typical timeout per individual block erase = 2^n ms	1s
22h	0000h	Typical timeout for full chip erase = 2^n ms	NA
23h	0004h	Maximum timeout for word program = 2^n times typical	256µs
24h	0004h	Maximum timeout for tetra word = 2^n times typical	256µs
25h	0004h	Maximum timeout per individual block erase = 2^n times typical	16s
26h	0000h	Maximum timeout for chip erase = 2^n times typical	NA

Table 20. Device Geometry Definition

Offset Word Mode		Data	Description	Value
27h		0017h	Device Size = 2^n in number of bytes	8 MByte
28h 29h		0001h 0000h	Flash Device Interface Code description	x16 Async.
2Ah 2Bh		0003h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	8 Byte
2Ch		0003h	Number of Erase Block Regions within the device bit 7 to 0 = x = number of Erase Block Regions It specifies the number of regions within the device containing one or more contiguous Erase Blocks of the same size.	3
M58MR064C	2Dh 2Eh	005Fh 0000h	Region 1 Information (main block - Bank B) Number of identical-size erase block = 005Fh+1	96
	2Fh 30h	0000h 0001h	Region 1 Information (main block - Bank B) Block size in Region 1 = 0100h * 256 byte	64 KByte
	31h 32h	001Eh 0000h	Region 2 Information (main block - Bank A) Number of identical-size erase block = 001Eh+1	31
	33h 34h	0000h 0001h	Region 2 Information (main block - Bank A) Block size in Region 2 = 0100h * 256 byte	64 KByte
	35h 36h	0007h 0000h	Region 3 Information (parameter block - Bank A) Number of identical-size erase block = 0007h+1	8
	37h 38h	0020h 0000h	Region 3 Information (parameter block - Bank A) Block size in Region 3 = 0020h * 256 byte	8 KByte
M58MR064D	2Dh 2Eh	0007h 0000h	Region 1 Information (parameter block - Bank A) Number of identical-size erase block = 0007h+1	8
	2Fh 30h	0020h 0000h	Region 1 Information (parameter block - Bank A) Block size in Region 1 = 0020h * 256 byte	8 KByte
	31h 32h	001Eh 0000h	Region 2 Information (main block - Bank A) Number of identical-size erase block = 001Eh+1	31
	33h 34h	0000h 0001h	Region 2 Information (main block - Bank A) Block size in Region 2 = 0001h * 256 byte	64 KByte
	35h 36h	005Fh 0000h	Region 3 Information (parameter block - Bank B) Number of identical-size erase block = 005Fh+1	96
	37h 38h	0000h 0001h	Region 3 Information (parameter block - Bank B) Block size in Region 3 = 0001h * 256 byte	64 KByte

Table 21. Primary Algorithm-Specific Extended Query Table

Offset	Data	Description	Value
(P)h = 39h	0050h		"P"
	0052h	Primary Algorithm extended Query table unique ASCII string “PRI”	"R"
	0049h		"I"
(P+3)h = 3Ch	0031h	Major version number, ASCII	"1"
(P+4)h = 3Dh	0030h	Minor version number, ASCII	"0"
(P+5)h = 3Eh	00E6h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte.	
	0003h		
(P+7)h	0000h	bit 0 Chip Erase supported (1 = Yes, 0 = No)	No
		bit 1 Erase Suspend supported (1 = Yes, 0 = No)	Yes
(P+8)h	0000h	bit 2 Program Suspend supported (1 = Yes, 0 = No)	Yes
		bit 3 Legacy Lock/Unlock supported (1 = Yes, 0 = No)	No
		bit 4 Queued Erase supported (1 = Yes, 0 = No)	No
		bit 5 Instant individual block locking supported (1 = Yes, 0 = No)	Yes
		bit 6 Protection bits supported (1 = Yes, 0 = No)	Yes
		bit 7 Page mode read supported (1 = Yes, 0 = No)	Yes
		bit 8 Synchronous read supported (1 = Yes, 0 = No)	Yes
		bit 9 Simultaneous operation supported (1 = Yes, 0 = No)	Yes
		bit 10 to 31 Reserved; undefined bits are ‘0’. If bit 31 is ’1’ then another 31 bit field of optional features follows at the end of the bit-30 field.	
(P+9)h = 42h	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query	Yes
		bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No)	
		bit 7 to 1 Reserved; undefined bits are ‘0’	
(P+A)h = 43h	0003h	Block Protect Status Defines which bits in the Block Status Register section of the Query are implemented.	
(P+B)h	0000h		
		bit 0 Block protect Status Register Protect/Unprotect bit active (1 = Yes, 0 = No)	Yes
		bit 1 Block Lock Status Register Lock-Down bit active (1 = Yes, 0 = No)	Yes
		bit 15 to 2 Reserved for future use; undefined bits are ‘0’	
(P+C)h = 45h	0018h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance)	1.8V
		bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	
(P+D)h = 46h	00C0h	V_{PP} Supply Optimum Program/Erase voltage	12V
		bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	
(P+E)h = 47h (P+F)h (P+10)h (P+11)h (P+12)h	0000h	Reserved	

Table 22. Burst Read Information

Offset	Data	Description	Value
(P+13)h = 4Ch	0003h	Page-mode read capability bits 0-7 'n' such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	8 Byte
(P+14)h = 4Dh	0003h	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	3
(P+15)h = 4Eh	0001h	Synchronous mode read capability configuration 1 bit 3-7 Reserved bit 0-2 'n' such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bit 0-2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	4
(P+16)h = 4Fh	0002h	Synchronous mode read capability configuration 2	8
(P+17)h = 50h	0007h	Synchronous mode read capability configuration 3	Cont.
(P+18)h = 51h	0036h	Max operating clock frequency (MHz)	54 MHz
(P+19)h = 52h	0001h	Supported handshaking signal ($\overline{WAIT}$ pin) bit 0 during synchronous read (1 = Yes, 0 = No) bit 1 during asynchronous read (1 = Yes, 0 = No)	 Yes No

Table 23. Security Code Area

Offset	Data	Description
80h	0000-0000-0000-0XX0	Lock Protection Register
81h	XXXX	64 bits: unique device number
82h	XXXX	
83h	XXXX	
84h	XXXX	
85h	XXXX	64 bits: User Programmable OTP
86h	XXXX	
87h	XXXX	
88h	XXXX	

Table 24. AC Measurement Conditions

Input Rise and Fall Times	≤ 4ns
Input Pulse Voltages	0 to V_{DDQ}
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$

Figure 8. Testing Input/Output Waveforms

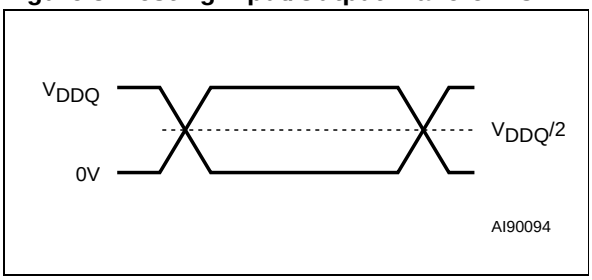


Figure 9. AC Testing Load Circuit

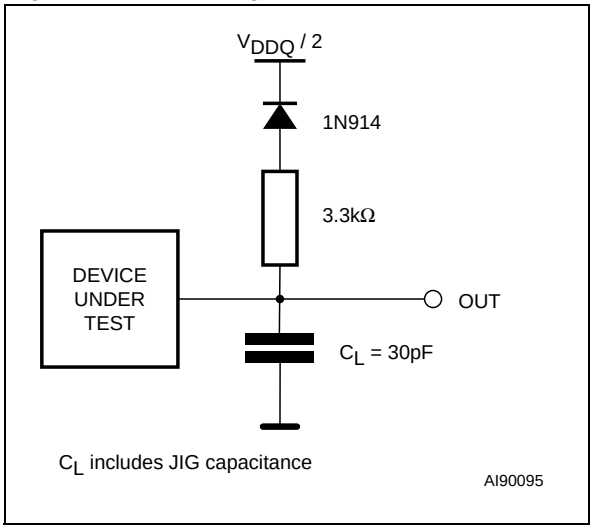


Table 25. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 26. DC Characteristics
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±5	µA
I_{CC1}	Supply Current (Asynchronous Read Mode)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	20	mA
	Supply Current (Synchronous Read Mode Continuous Burst)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 40MHz		20	30	mA
I_{CC2}	Supply Current (Power-down)	$\overline{RP} = V_{SS} \pm 0.2V$		2	10	µA
I_{CC3}	Supply Current (Standby)	$\overline{E} = V_{DD} \pm 0.2V$		15	50	µA
I_{CC4} (1)	Supply Current (Program or Erase)	Word Program, Block Erase in progress		10	20	mA
I_{CC5} (1)	Supply Current (Dual Bank)	Program/Erase in progress in one Bank, Asynchronous Read in the other Bank		20	40	mA
		Program/Erase in progress in one Bank, Synchronous Read in the other Bank		30	50	mA
I_{PP1}	V_{PP} Supply Current (Program or Erase)	V_{PP} = 12V ± 0.6V		5	10	mA
I_{PP2}	V_{PP} Supply Current (Standby or Read)	$V_{PP} \le V_{CC}$		0.2	5	µA
		V_{PP} = 12V ± 0.6V		100	400	µA
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PP} Supply Voltage	Program, Erase	V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{PPH}	V_{PP} Supply Voltage	Double/Tetra Word Program	11.4		12.6	V
V_{PPLK}	Program or Erase Lockout				1	V

Note: 1. Sampled only, not 100% tested.
2. V_{PP} may be connected to 12V power supply for a total of less than 100 hrs.

Table 27. Asynchronous Read AC Characteristics
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	Test Condition	M58MR064				Unit
				100		120		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		ns
t_{AVLH}	t_{AVAVDH}	Address valid to Latch Enable High	$\overline{G}$ = V_{IH}	10		10		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		45		45	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{ELLH}	t_{ELAVDH}	Chip Enable Low to Latch Enable High	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		25		35	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{LHAX}	t_{AVDHAX}	Latch Enable High to Address Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{LHGL}		Latch Enable High to Output Enable Low	$\overline{E}$ = V_{IL}	10		10		ns
t_{LLLH}	$t_{AVDLAVDH}$	Latch Enable Pulse Width	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{LLQV}	t_{AVDLQV}	Latch Enable Low to Output Valid (Random)	$\overline{E}$ = V_{IL}		100		120	ns
t_{LLQV1}		Latch Enable Low to Output Valid (Page)	$\overline{E}$ = V_{IL}		45		45	ns

Note: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 10. Asynchronous Read AC Waveforms

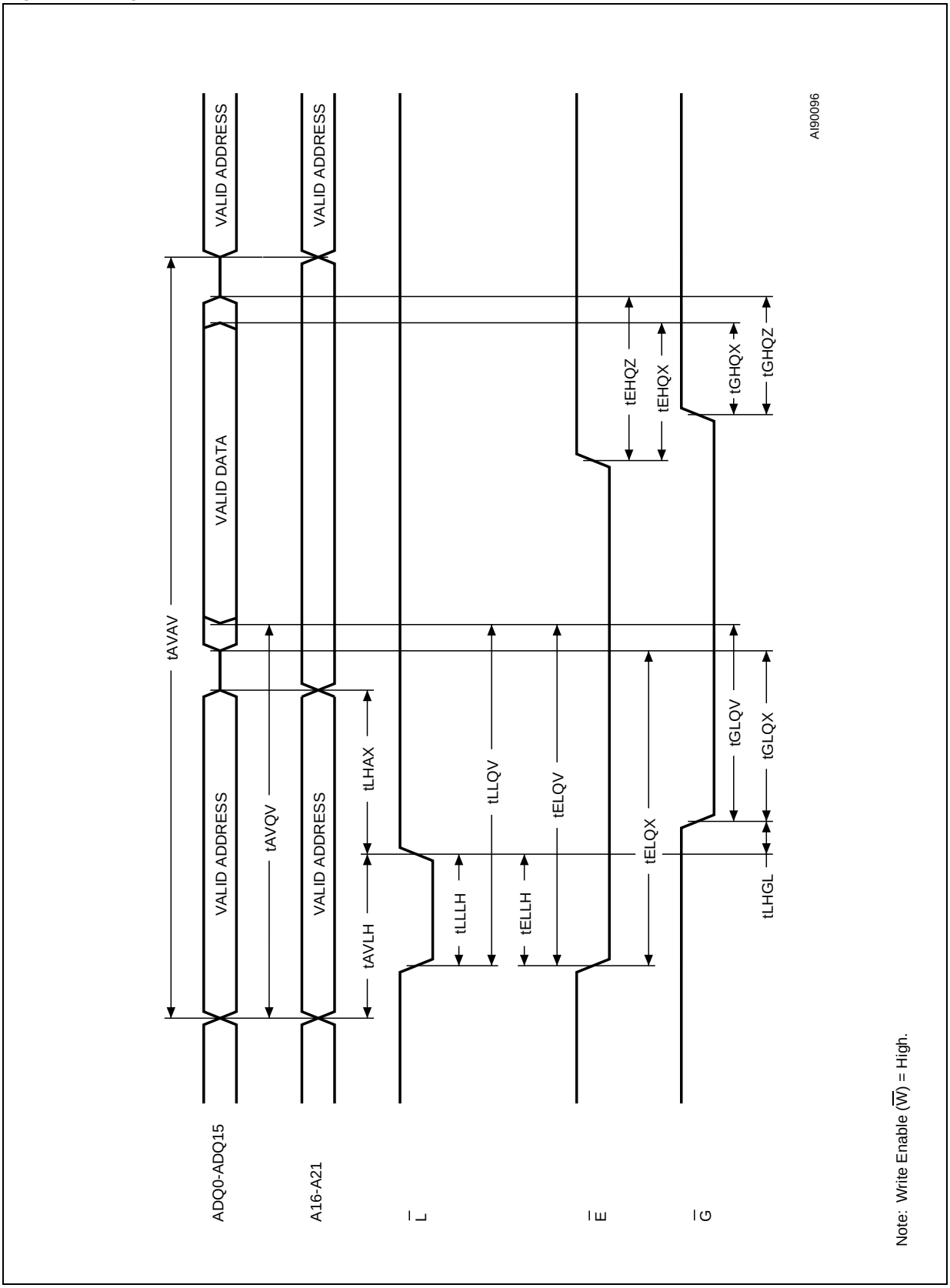


Figure 11. Page Read AC Waveforms

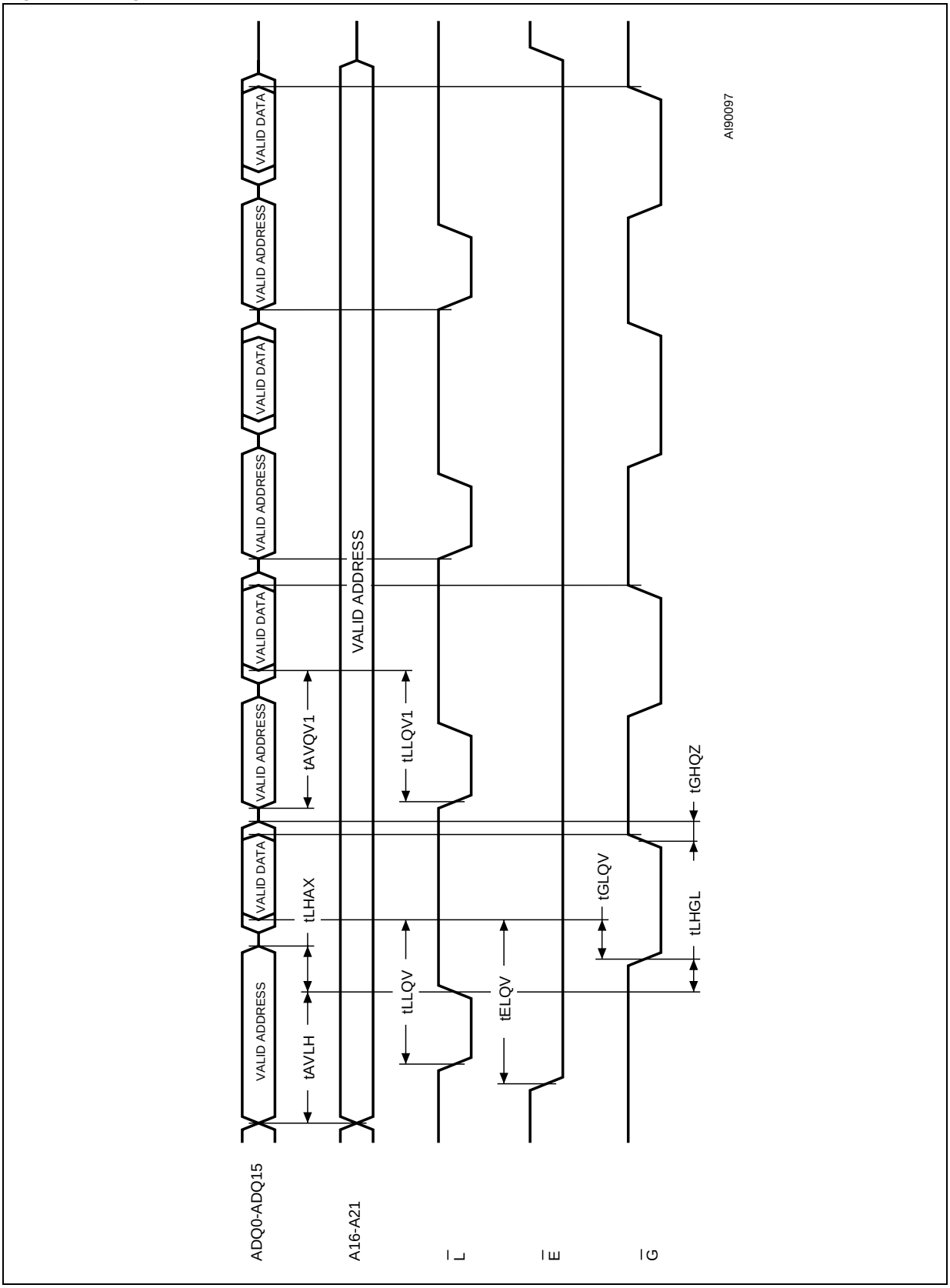
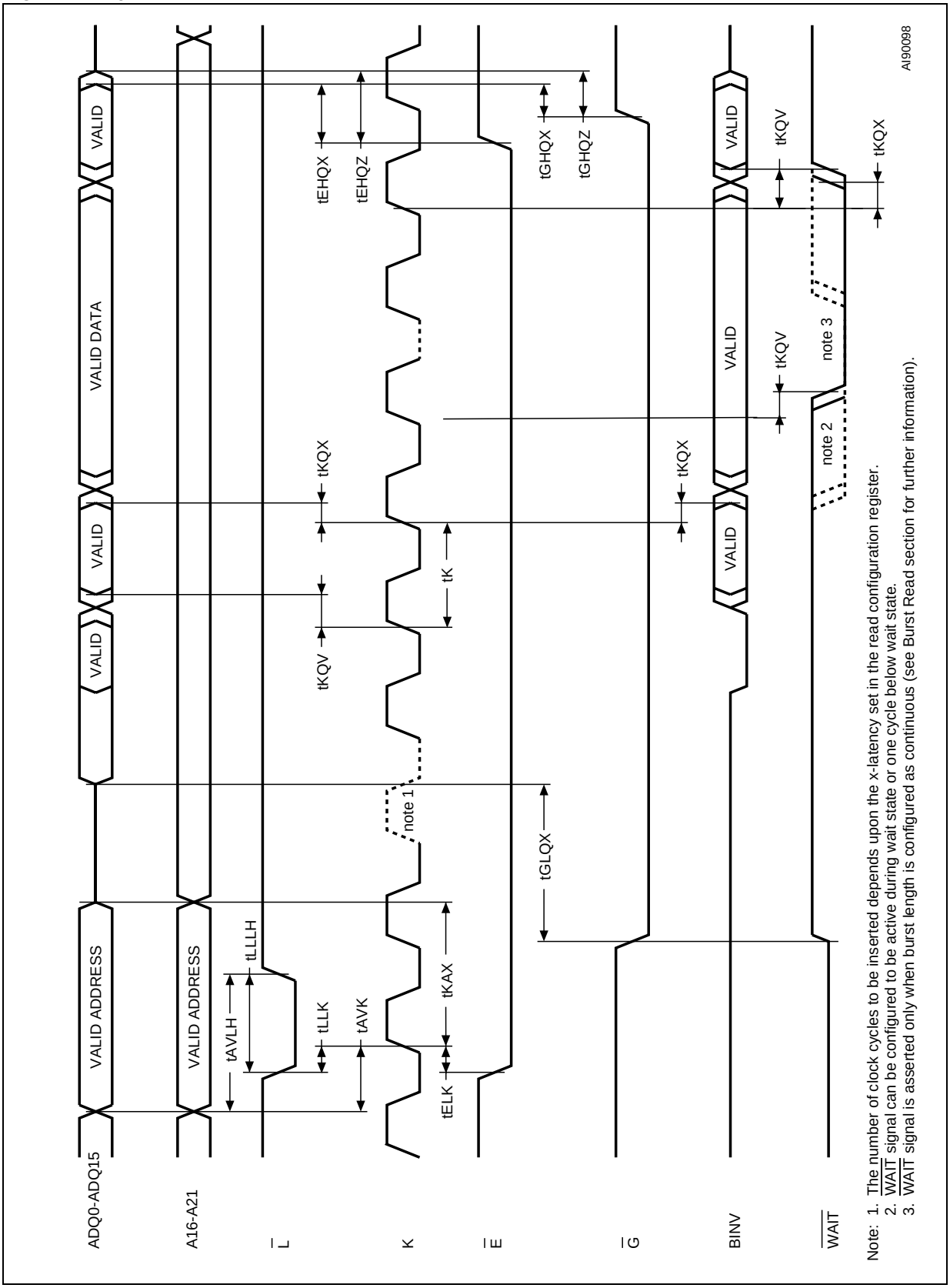


Table 28. Synchronous Burst Read AC Characteristics
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	Test Condition	M58MR064				Unit
				100		120		
				Min	Max	Min	Max	
t_{AVK}	t_{AVCLKH}	Address Valid to Clock		7		7		ns
t_{ELK}	$t_{CELCLKH}$	Chip Enable Low to Clock		7		7		ns
t_K	t_{CLK}	Clock Period		18		25		ns
t_{KAX}	t_{CLKHAX}	Clock to Address Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	10		10		ns
t_{KHKL}	$t_{CLKHCLKL}$	Clock High		5		5		ns
t_{KLKH}	$t_{CLKLCLKH}$	Clock Low		5		5		ns
t_{KQV}	t_{CLKHQV}	Clock to Data Valid Clock to BINV Valid Clock to WAIT Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		14		18	ns
t_{KQX}	t_{CLKHQX}	Clock to Output Transition Clock to BINV Transition Clock to WAIT Transition	$\overline{E}$ = V_{IL}	4		4		ns
t_{LLK}	$t_{AVDLCLKH}$	Latch Enable Low to Clock		7		7		ns

Figure 12. Synchronous Burst Read



Note: 1. The number of clock cycles to be inserted depends upon the x-latency set in the read configuration register.
2. WAIT signal can be configured to be active during wait state or one cycle below wait state.
3. WAIT signal is asserted only when burst length is configured as continuous (see Burst Read section for further information).

Table 29. Write AC Characteristics, Write Enable Controlled
(T_A = –40 to 85 °C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	M58MR064				Unit
			100		120		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVLH}		Address Valid to Latch Enable High	10		10		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		ns
t_{ELLH}		Chip Enable Low to Latch Enable High	10		10		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{GHLL}		Output Enable High to Latch Enable Low	20		20		ns
t_{GHWL}		Output Enable High to Write Enable Low	20		20		ns
t_{LHAX}		Latch Enable High to Address Transition	10		10		ns
t_{LHWH}		Latch Enable High to Write Enable High	10		10		ns
t_{LLLH}		Latch Enable Pulse Width	10		10		ns
t_{VDHEL}	t_{VCS}	V_{DD} High to Chip Enable Low	50		50		µs
t_{VPPHWH}		V_{PP} High to Write Enable High	200		200		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{WHLL}		Write Enable High to Latch Enable Low	0		0		ns
t_{WHVPPL}		Write Enable High to V_{PP} Low	200		200		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		ns
t_{WHWPV}		Write Enable High to Write Protect Valid	200		200		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{WPVWH}		Write Protect Valid to Write Enable High	200		200		ns

Figure 13. Write AC Waveforms, $\overline{W}$ Controlled

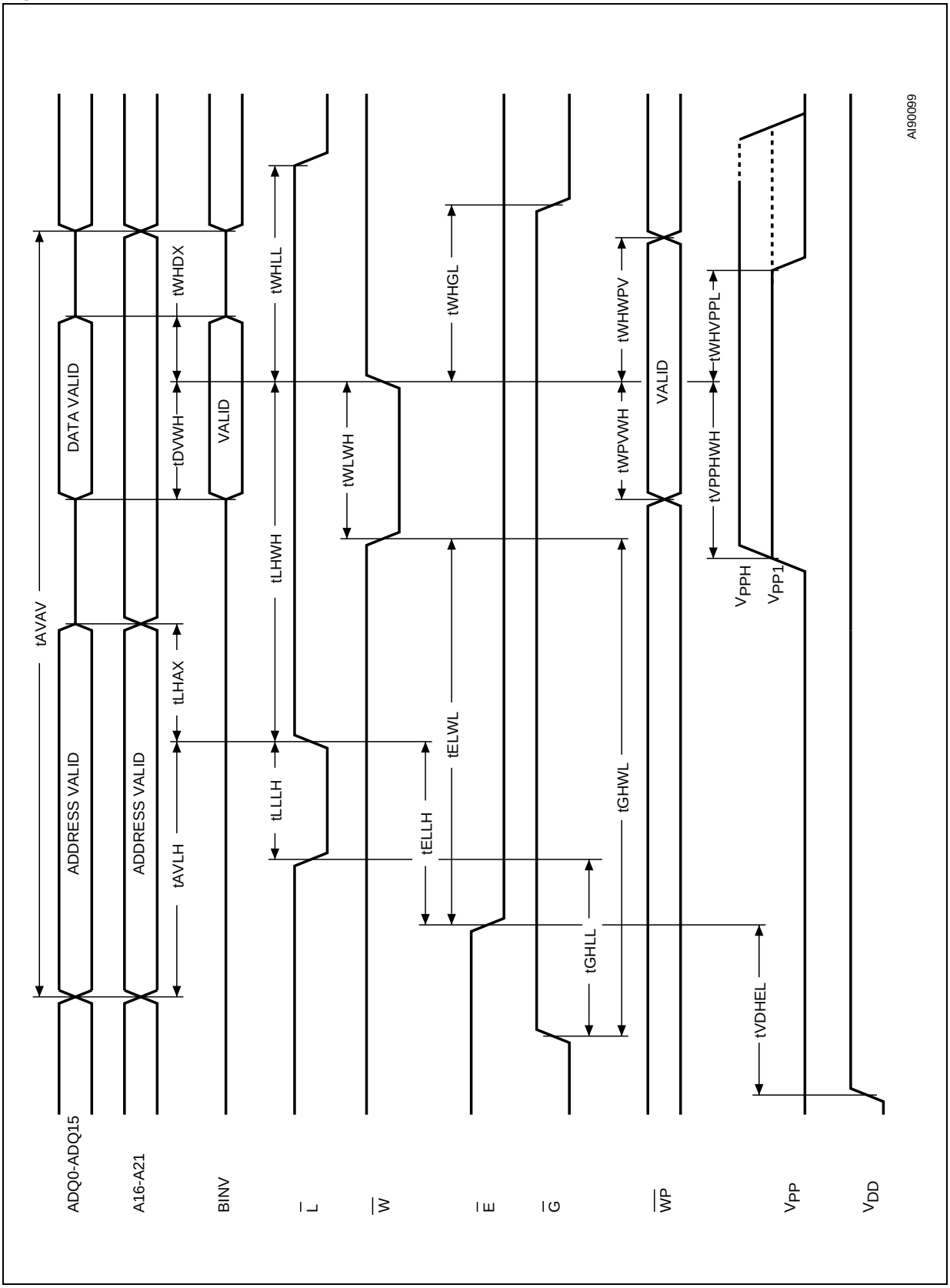


Table 30. Write AC Characteristics, Chip Enable Controlled
(T_A = –40 to 85 °C; V_{DD} = V_{DDQ} = 1.65V to 2.0V)

Symbol	Alt	Parameter	M58MR064				Unit
			100		120		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		ns
t_{AVLH}		Address Valid to Latch Enable High	10		10		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40		40		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	30		30		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	60		60		ns
t_{ELLH}		Chip Enable Low to Latch Enable High	10		10		ns
t_{GHLL}		Output Enable High to Latch Enable Low	20		20		ns
t_{LHAX}		Latch Enable High to Address Transition	10		10		ns
t_{LHEH}		Latch Enable High to Chip Enable High	10		10		ns
t_{LLLH}		Latch Enable Pulse Width	10		10		ns
t_{VDHEL}	t_{VCS}	V_{DD} High to Chip Enable Low	50		50		µs
t_{VPPHEH}		V_{PP} High to Chip Enable High	200		200		ns
t_{EHVPPL}		Chip Enable High to V_{PP} Low	200		200		ns
t_{EHWPV}		Chip Enable High to Write Protect Valid	200		200		ns
t_{WLEL}	t_{WS}	Chip Enable Low to Chip Enable Low	0		0		ns
t_{WPVEH}		Write Protect Valid to Chip Enable High	200		200		ns

Figure 14. Write AC Waveforms, $\overline{E}$ Controlled

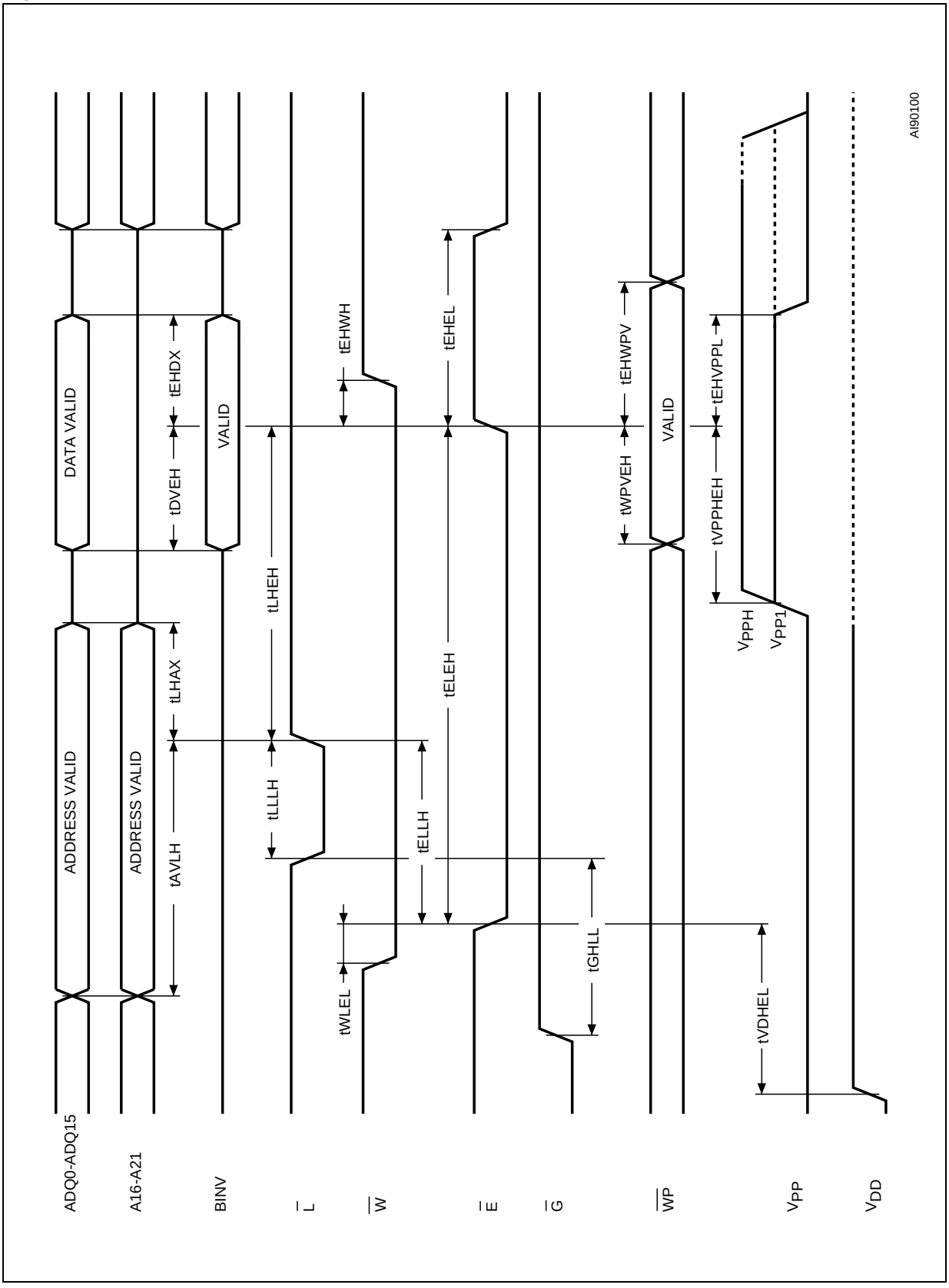


Figure 15. Reset and Power-up AC Waveforms

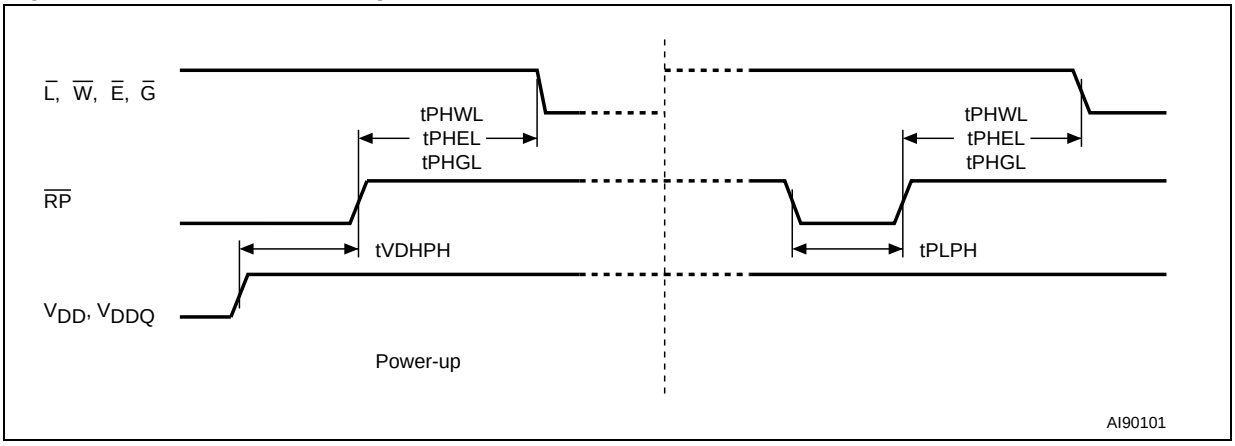


Table 31. Reset and Power-up AC Characteristics

Symbol	Parameter	Test Condition	Min	Unit
t_{PLPH} (1,2)	$\overline{RP}$ Pulse Width		100	ns
t_{PHEL} t_{PHLL} t_{PHWL}	Reset High to Device Enabled	During Program and Erase	50	µs
		Other Conditions	30	ns
t_{VDHPH} (3)	Supply Valid to Reset High		50	µs

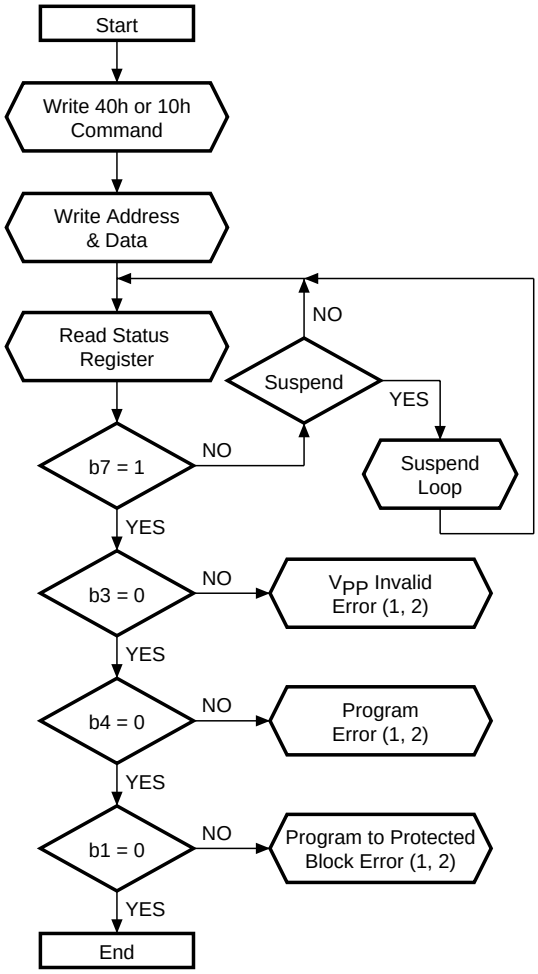
Note: 1. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
2. Sampled only, not 100% tested.
3. It is important to assert $\overline{RP}$ in order to allow proper CPU initialization during Power-up or System reset.

Table 32. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = –40 to 85°C; V_{DD} = V_{DDQ} = 1.65V to 2.0V, V_{PP} = V_{DD} unless otherwise specified)

Parameter	Min	Max (1)	Typ	Typical after 100k W/E Cycles	Unit
Parameter Block (4 K-Word) Erase (Preprogrammed)		2.5	0.5	1	sec
Main Block (32 K-Word) Erase (Preprogrammed)		10	1	3	sec
Bank Erase (Preprogrammed, Bank A)			4		sec
Bank Erase (Preprogrammed, Bank B)			15		sec
Chip Program (2)			40		sec
Chip Program (DPG, V_{PP} = 12V) (2)			20		sec
Word Program (3)		200	10	10	µs
Double Word Program		200	10	10	µs
Tetra Word Program		200	10	10	µs
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. Max values refer to the maximum time allowed by the internal algorithm before error bit is set. Worst case conditions program or erase should perform significantly better.
2. Excludes the time needed to execute the sequence for program instruction.
3. Same timing value if V_{PP} = 12V.

Figure 16. Program Flowchart and Pseudo Code (1)



Program instruction:
– write 40h or 10h command
– write Address & Data
(memory enters read status state after the Program instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled) if PES instruction given execute suspend program loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4 = 1, Program error:
– error handler

If b1 = 1, Program to protected block error:
– error handler

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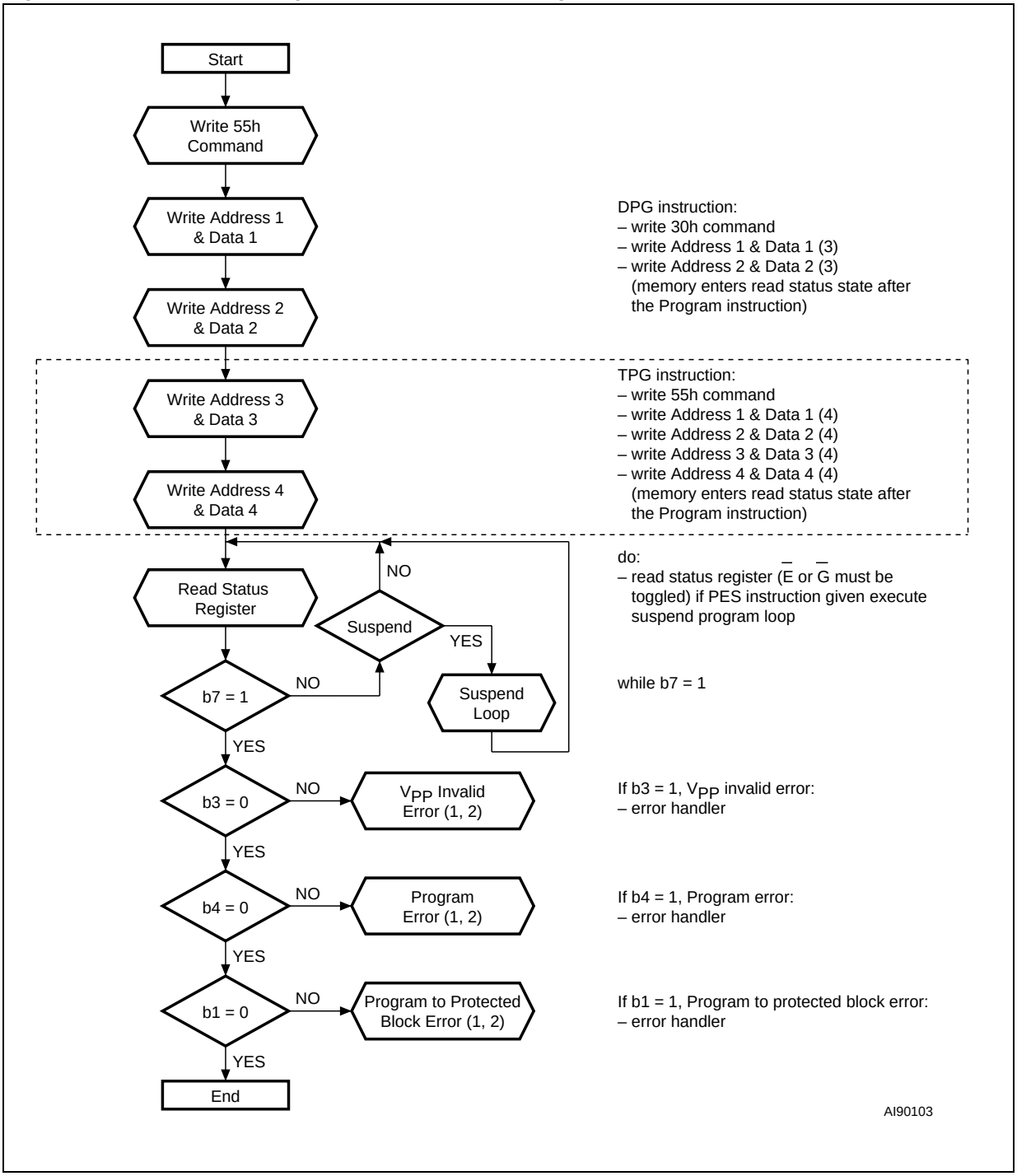
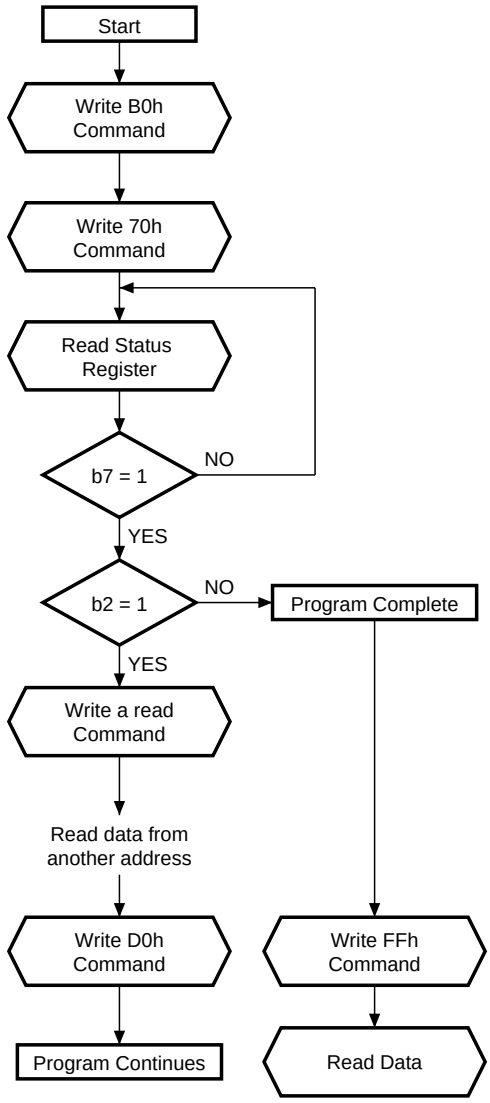
Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a program sequence.
2. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 17. Double Word Program and Tetra Word Program Flowchart and Pseudo code (1)



Note: 1. Status check of b1 (Protected Block), b3 (VPP Invalid) and b4 (Program Error) can be made after each program operation or after a program sequence.
2. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.
3. Address 1 and address 2 must be consecutive addresses differing only for address bit A0.
4. Address, address 2, address 3 and address 4 must be consecutive addresses differing only for address bit A1-A0.

Figure 18. Program Suspend & Resume Flowchart and Pseudo Code



PES instruction:
– write B0h command
do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b2 = 0 Program completed

PER instruction:
– write D0h command to resume the program
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

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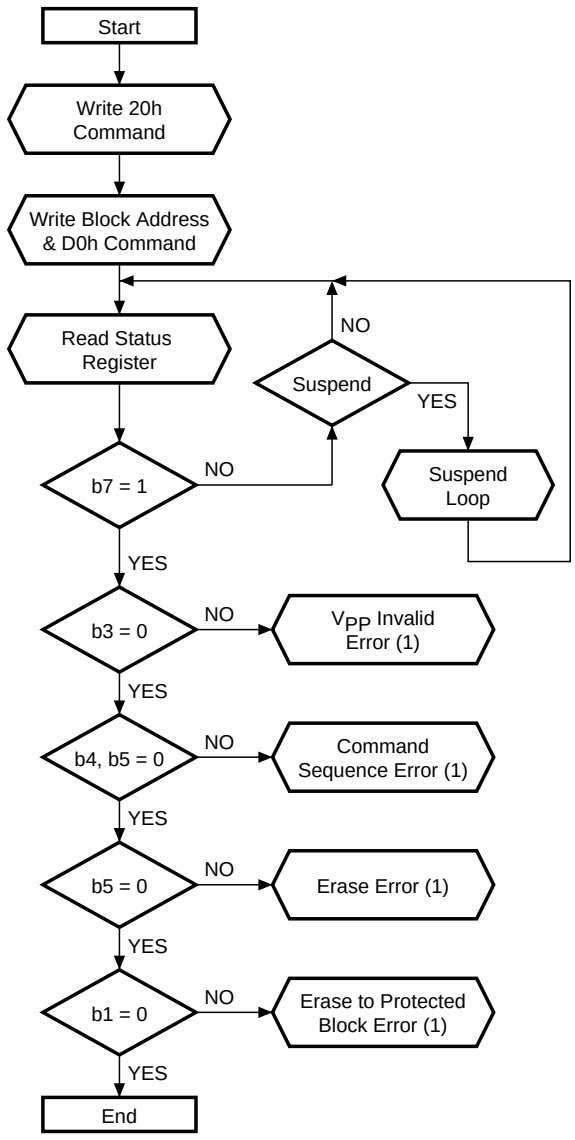
Figure 19. Block Erase Flowchart and Pseudo Code



EE instruction:
– write 20h command
– write Block Address (A12-A21) & command D0h
(memory enters read status state after the EE instruction)

do:
– read status register ($\overline{E}$ or $\overline{G}$ must be toggled) if PES instruction given execute suspend erase loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4, b5 = 1, Command sequence error:
– error handler

If b5 = 1, Erase error:
– error handler

If b1 = 1, Erase to protected block error:
– error handler

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Figure 20. Erase Suspend & Resume Flowchart and Pseudo Code

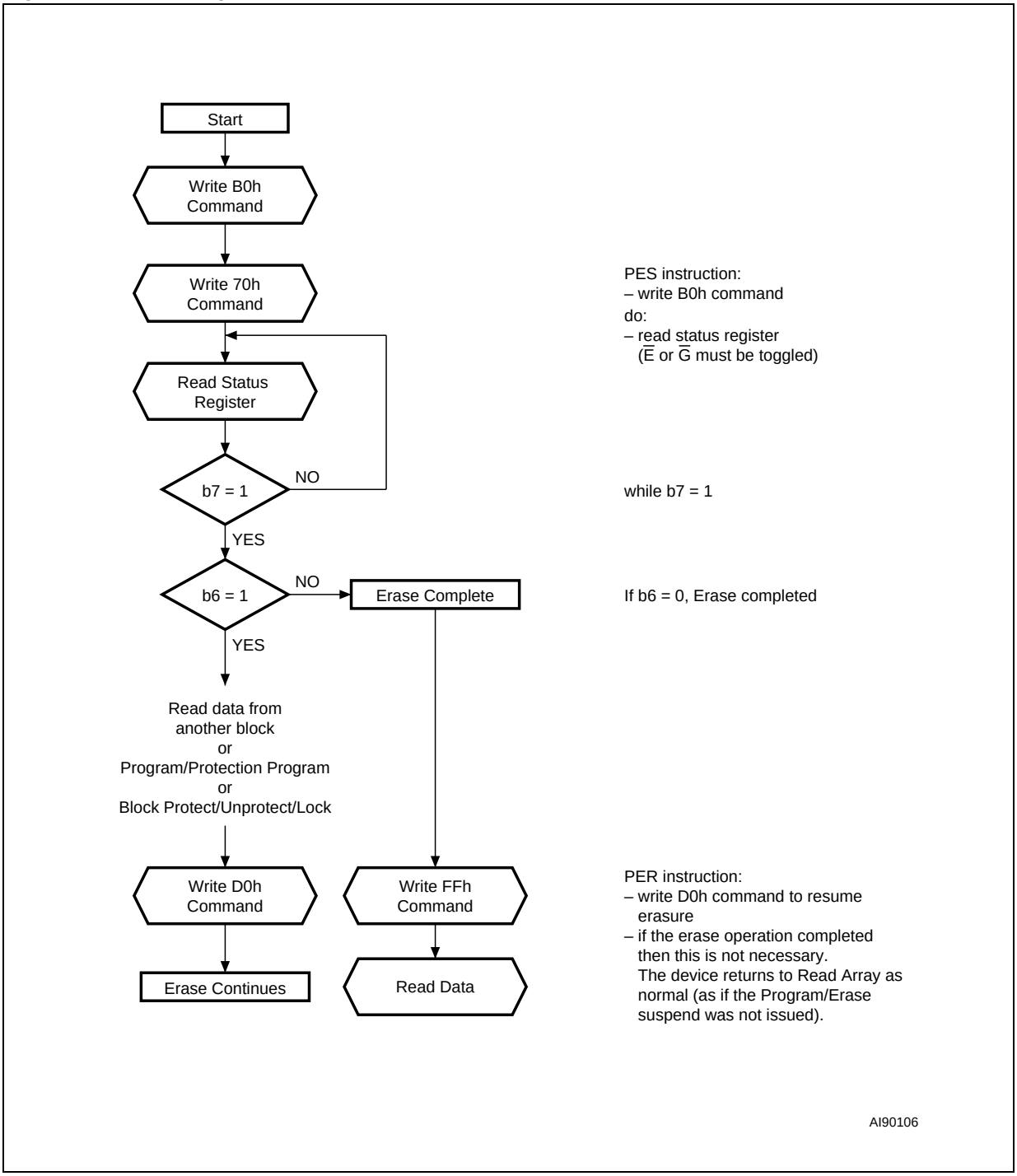


Table 33. Command Interface States - Lock table

Current State of the Other Partition	Current State of the Current Partition		Command Input to the Current Partition (and Next State of the Current Partition)										
	Mode	State	Others	Read Memory Array (FFH)	Erase Confirm P/E Resume BU Confirm (D0h)	Read Status Register (70h)	Clear Status Register (50h)	Read elect. sign. (90h)	Read CFI (98h)	Block Protect-Unprotect-Lock setup write RCR setup (60h)	Block Protect Confirm (01h)	Block Lock Confirm (2Fh)	Write RCR Confirm (03h)
Any State	Read	Array CFI Electronic Signature Status	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block Protect-Unprotect-LockSetup Write RCR Setup	Read Array	Read Array	Read Array
Any State	Protect Unprotect Lock RCR	Setup	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockBlock	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockError Write RCR Error	Block Protect-Unprotect-LockBlock	Block Protect-Unprotect-LockBlock	Set RCR
		Error Protect-Unprotect-LockBlock Set RCR	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block Protect-Unprotect-LockSetup Write RCR Setup	Read Array	Read Array	Read Array
Any State	Protection Register	Done	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block Protect-Unprotect-LockSetup Write RCR Setup	Read Array	Read Array	Read Array
Any State	Program-Multiple Program	Done	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block Protect-Unprotect-LockSetup Write RCR Setup	Read Array	Read Array	Read Array
Setup Idle Erase Suspend	Program Suspend	Read Array, CFI, Elect. Sign., Status	SEE MODIFY TABLE	PS Read Array	Program (Busy)	PS Read Status Register	PS Read Array	PS Read Elect. Sign.	PS Read CFI	PS Read Array	PS Read Array	PS Read Array	PS Read Array
Idle	Block-Bank Erase	Setup	Erase Error	Erase Error	Erase (Busy)	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error
Any State		Error Done	SEE MODIFY TABLE	Read Array	Read Array	Read Status Register	Read Array	Read Elect. Sign.	Read CFI	Block Protect-Unprotect-LockSetup Write RCR Setup	Read Array	Read Array	Read Array
Setup Busy Idle Program Suspend	Erase Suspend	Read Array, CFI, Elect. Sign., Status	SEE MADIFY TABLE	ES Read Array	Erase (Busy) ES Read Array Erase (Busy) ES Read Array	ES Read Status Register	ES Read Array	ES Read Elect. Sign.	ES Read CFI	Block Protect-Unprotect-LockSetup Write RCR Setup	ES Read Array	ES Read Array	ES Read Array

Table 34. Command Interface States - Modify table

Current State of the Other Partition	Current State of the Current Partition		Command Input to the Current Partition (and Next State of the Current Partition)						
	Mode	State	Others	Program Setup (10h/40h)	Block Erase Setup (20h)	Program-Erase Suspend (B0h)	OTP Setup (C0h)	Multiple Program Setup (30h/55h)	Bank Erase Setup (80h)
Setup	Read	Array, CFI, Electronic Signature, Status Register	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Busy									
Idle				Program setup	Block Erase Setup		OTP Setup	Multiple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Setup	Protect Unprotect-Lock/ RCR	Error, Protect-Unprotect-LockBlock, Set RCR	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Busy									
Idle				Program setup	Block Erase Setup		OTP Setup	Multiple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Idle	Protection Register	Setup	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)	Protection Register (Busy)
Setup		Busy							
Busy		Done	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Idle				Program Setup	Block Erase Setup		OTP Setup	Multiple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Any State	Program-Multiple Program	Setup	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)	Program (Busy)
Idle		Busy				PS Read Status Register			
Setup		Done	SEE LOCK TABLE	Read Array	Read Array	Read Array	Read Array	Read Array	Read Array
Busy									
Idle				Program Setup	Block Erase Setup		OTP Setup	Multiple Program Setup	Bank Erase Setup
Erase Suspend					Read Array		Read Array		Read Array
Program Suspend				Read Array				Read Array	
Setup	Program Suspend	Read Array, CFI, Elect. Sign., Status Register	SEE LOCK TABLE	PS Read Array	PS Read Array	PS Read Array	PS Read Array	PS Read Array	PS Read Array
Idle									
Erase Suspend									
Idle	Block-Bank Erase	Setup	SEE LOCK TABLE	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error	Erase Error
		Busy	Erase (Busy)	Erase (Busy)	Erase (Busy)	ES Read Status Register	Erase (Busy)	Erase (Busy)	Erase (Busy)
Setup	Erase Suspend	Read Array, CFI, Elect. Sign., Status Register	SEE LOCK TABLE	ES Read Array	ES Read Array	ES Read Array	ES Read Array	ES Read Array	ES Read Array
Busy									
Idle				Program Setup				Multiple Program Setup	
Program Suspend				ES Read Array				ES Read Array	

Table 35. Ordering Information Scheme

Example: M58MR064C 100 ZC 6 T

Device Type
M58

Architecture
M = Multiplexed Address/Data, Dual Bank, Burst Mode

Operating Voltage
R = 1.8V

Device Function
064C = 64 Mbit (x16), Dual Bank: 1/4-3/4 partitioning, Top Boot
064D = 64 Mbit (x16), Dual Bank: 1/4-3/4 partitioning, Bottom Boot

Speed
100 = 100 ns
120 = 120 ns

Package
ZC = TFBGA48: 0.5 mm pitch

Temperature Range
6 = –40 to 85°C

Option
T = Tape & Reel packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

Table 36. Daisy Chain Ordering Scheme

Example: M58MR064 -ZC T

Device Type
M58MR064

Daisy Chain
-ZC = TFBGA48: 0.5 mm pitch

Option
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

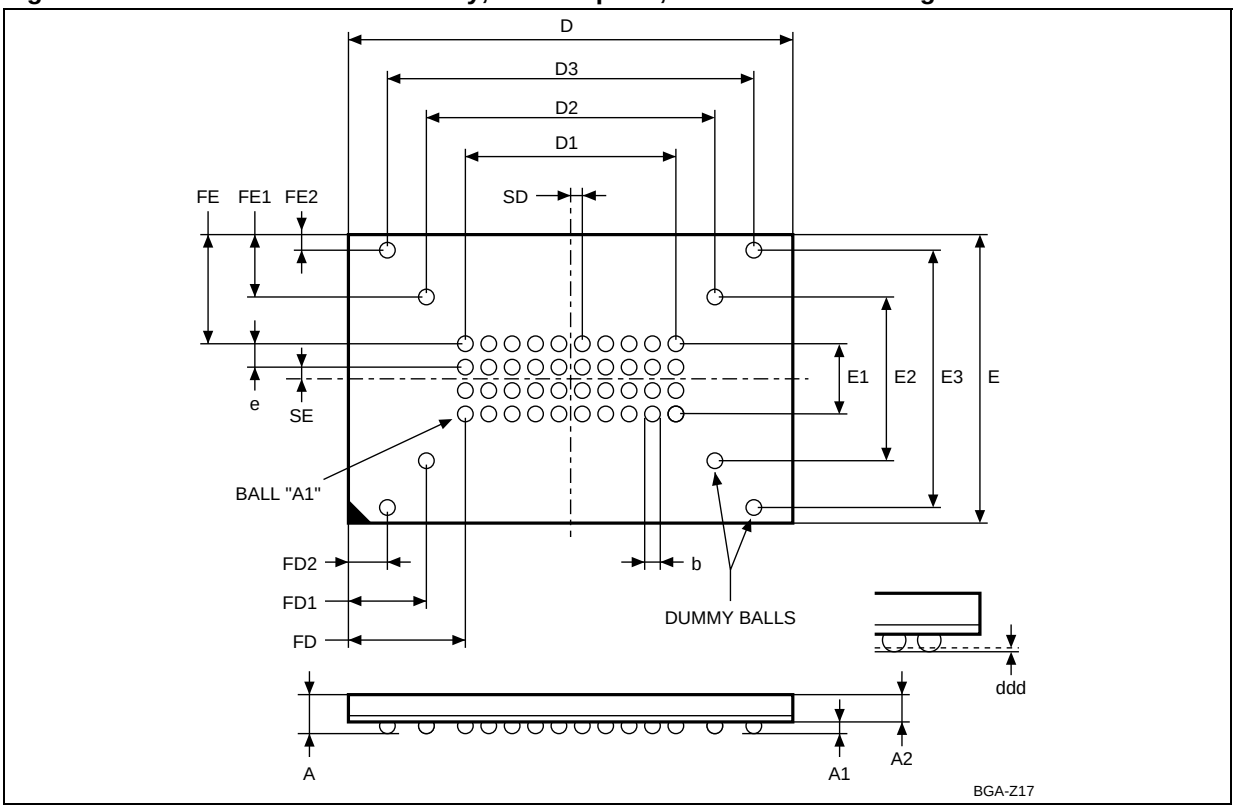
Table 37. Document Revision History

Date	Version	Revision Details
April 2001	-01	First Issue
07-Mar-2002	-02	Document Status changed to Datasheet, CFI information clarified: Table 18,data modified at Offset 13h. Table 19, data modified at Offsets 23h and 24h. Table 22, Offset addresses modified.

Table 38. TFBGA48 - 10 x 4 ball array, 0.5 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		0.950	1.200		0.0374	0.0472
A1		0.200	0.300		0.0079	0.0118
A2	0.790			0.0311		
b	0.300	0.250	0.350	0.0118	0.0098	0.0138
D	10.530	10.480	10.580	0.4146	0.4126	0.4165
D1	4.500	–	–	0.1772	–	–
D2	6.500	–	–	0.2559	–	–
D3	8.500	–	–	0.3346	–	–
ddd			0.080			0.0031
E	6.290	6.240	6.340	0.2476	0.2457	0.2496
E1	1.500	–	–	0.0591	–	–
E2	3.500	–	–	0.1378	–	–
E3	5.500	–	–	0.2165	–	–
e	0.500	–	–	0.0197	–	–
FD	3.015	–	–	0.1187	–	–
FD1	2.015	–	–	0.0793	–	–
FD2	1.015	–	–	0.0400	–	–
FE	2.395	–	–	0.0943	–	–
FE1	1.395	–	–	0.0549	–	–
FE2	0.395	–	–	0.0156	–	–
SD	0.250	–	–	0.0098	–	–
SE	0.250	–	–	0.0098	–	–

Figure 21. TFBGA48 - 10 x 4 ball array, 0.5 mm pitch, Bottom View Package Outline



Drawing is not to scale.

Figure 22. TFBGA48 Daisy Chain - Package Connections (Top view through package)

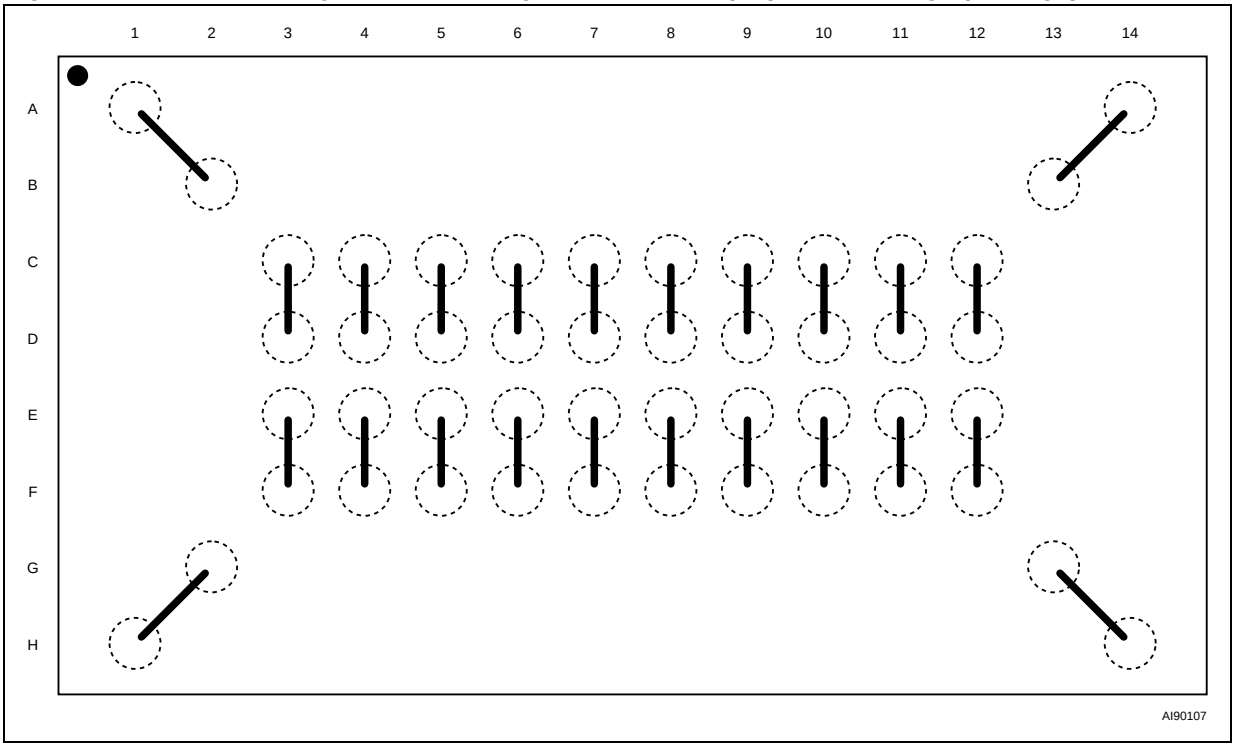


Figure 23. TFBGA48 Daisy Chain - PCB Connections proposal (Top view through package)