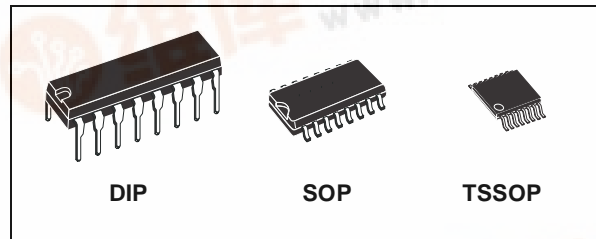




74AC138

3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED: $t_{PD} = 4.5ns$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu A$ (MAX.) at $T_A = 25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24mA$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 138
- IMPROVED LATCH-UP IMMUNITY



ORDER CODES

PACKAGE	TUBE	T & R
DIP	74AC138B	
SOP	74AC138M	74AC138MTR
TSSOP		74AC138TTR

DESCRIPTION

The 74AC138 is an advanced high-speed CMOS 3 TO 8 LINE DECODER (INVERTING) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

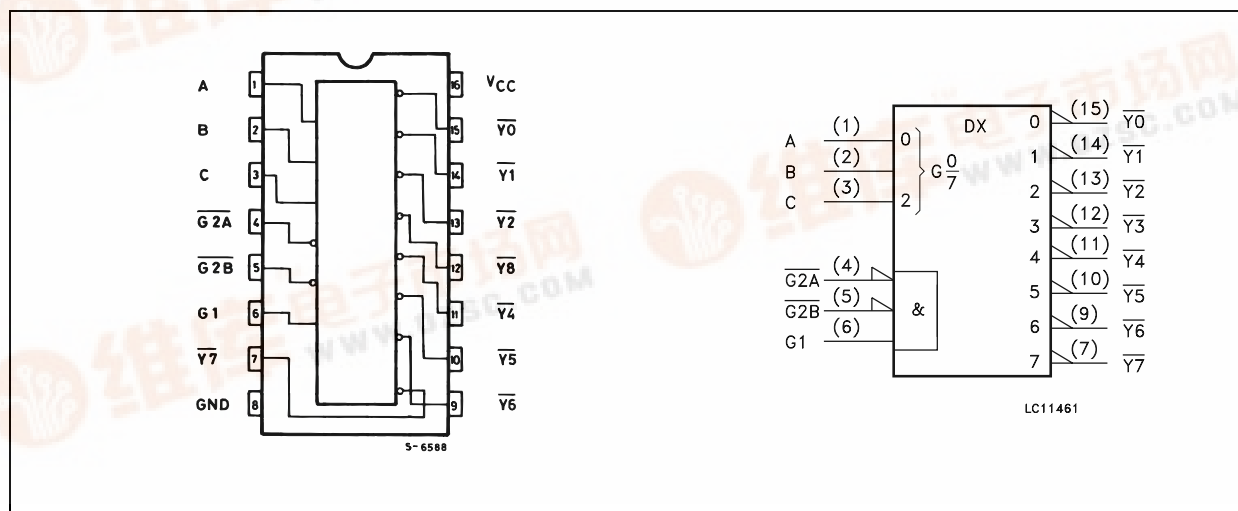
If the device is enabled, 3 binary select inputs (A, B, and C) determine which one of the outputs will go low. If enable input G1 is held low or either G2A

or G2B is held high, the decoding function is inhibited and all the 8 outputs go to high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

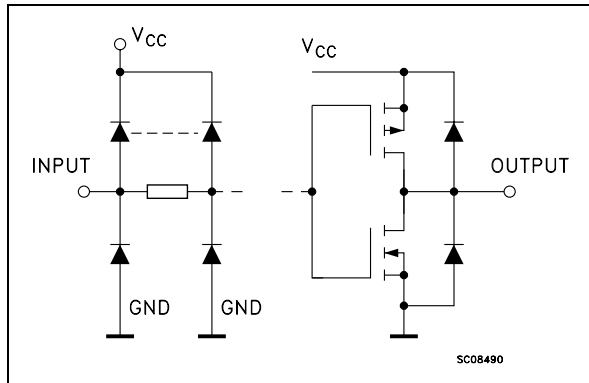
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



74AC138

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

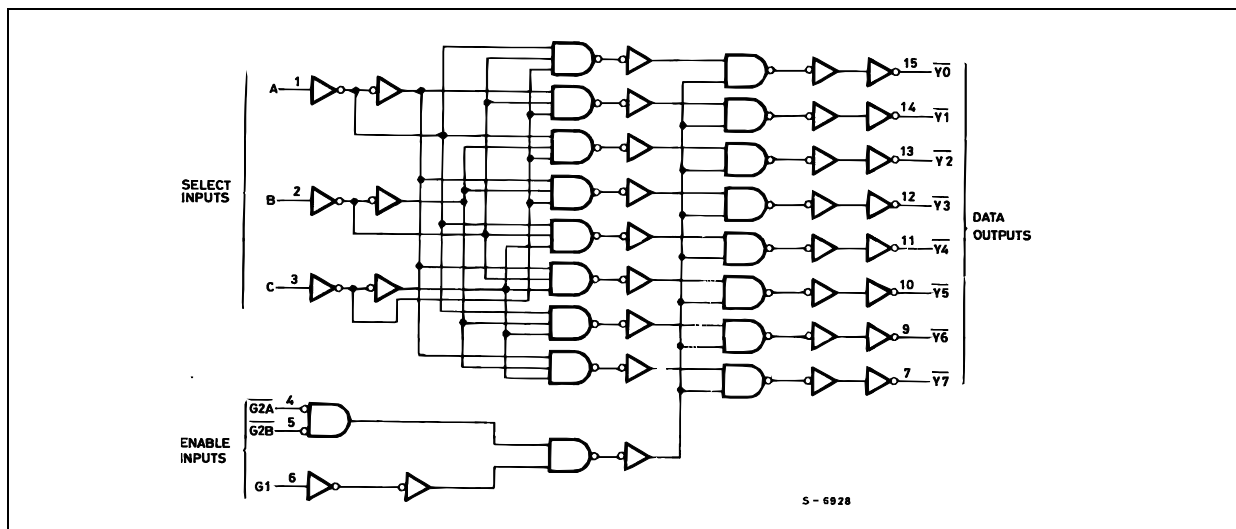
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$, $\overline{G2B}$	Enable Inputs
6	$\overline{G1}$	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	Y0 to Y7	Outputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or $5.5V$ (note 1)	8	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} -0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V _{IL}	Low Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} -0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V _{OH}	High Level Output Voltage	3.0	I _O =-50 μA	2.9	2.99		2.9		2.9		V
		4.5	I _O =-50 μA	4.4	4.49		4.4		4.4		
		5.5	I _O =-50 μA	5.4	5.49		5.4		5.4		
		3.0	I _O =-12 mA	2.56			2.46		2.4		
		4.5	I _O =-24 mA	3.86			3.76		3.7		
		5.5	I _O =-24 mA	4.86			4.76		4.7		
V _{OL}	Low Level Output Voltage	3.0	I _O =50 μA		0.002	0.1		0.1		0.1	V
		4.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		5.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		3.0	I _O =12 mA			0.36		0.44		0.5	
		4.5	I _O =24 mA			0.36		0.44		0.5	
		5.5	I _O =24 mA			0.36		0.44		0.5	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		80	μA
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75		50	mA
I _{OHD}			V _{OHD} = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

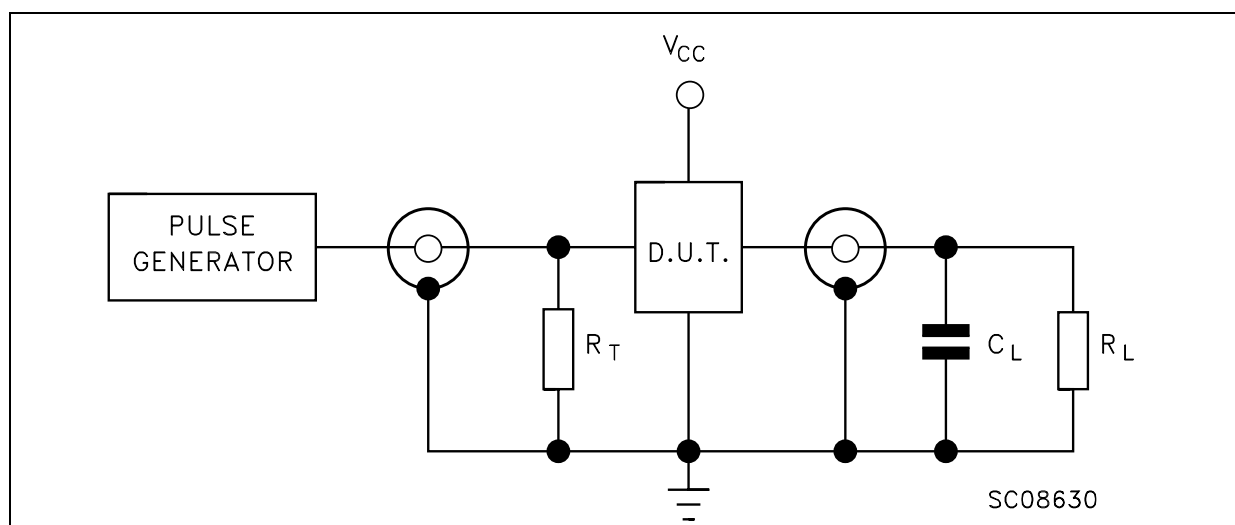
2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{PLH} t_{PHL}	Propagation Delay Time A, B, C to Y	3.3(*)		1.5	5.5	10.5	1.5	14.0	1.5	15.4	ns
		5.0(**)		1.5	4.5	9.0	1.5	10.0	1.5	11.0	
t_{PLH} t_{PHL}	Propagation Delay Time G1 to Y	3.3(*)		1.5	6.0	10.5	1.5	14.0	1.5	15.4	ns
		5.0(**)		1.5	4.5	11.0	1.5	10.0	1.5	11.0	
t_{PLH} t_{PHL}	Propagation Delay Time G2A or G2B to Y	3.3(*)		1.5	5.5	10.5	1.5	12.7	1.5	14.0	ns
		5.0(**)		1.5	4.5	9.0	1.5	10.0	1.5	10.0	

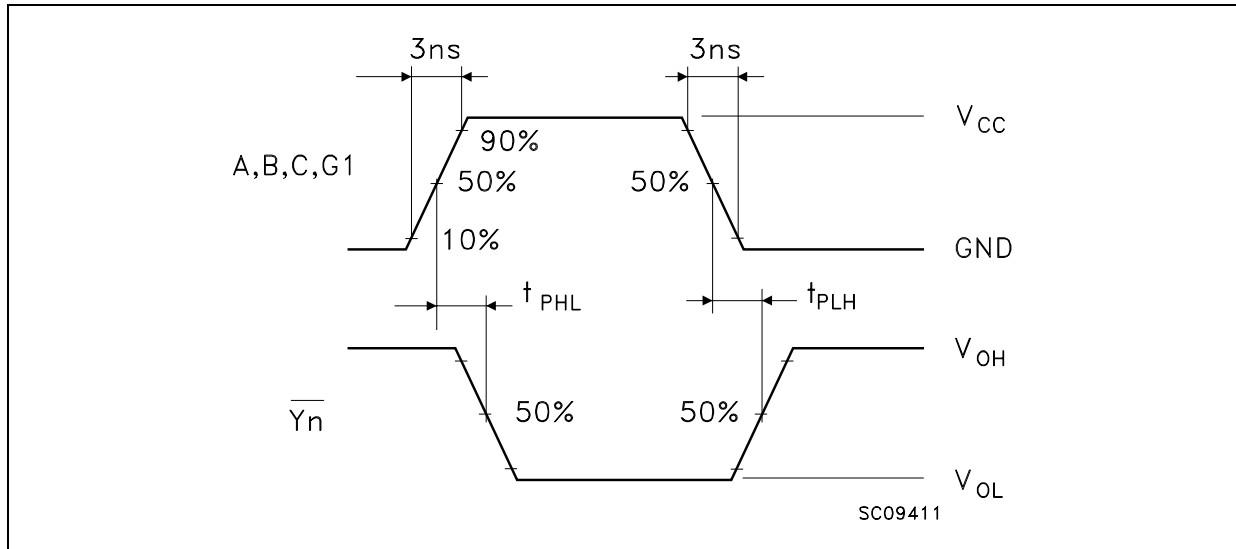
(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$ (**) Voltage range is $5.0\text{V} \pm 0.5\text{V}$ **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	5.0			4						pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0	$f_{IN} = 10\text{MHz}$		60						pF

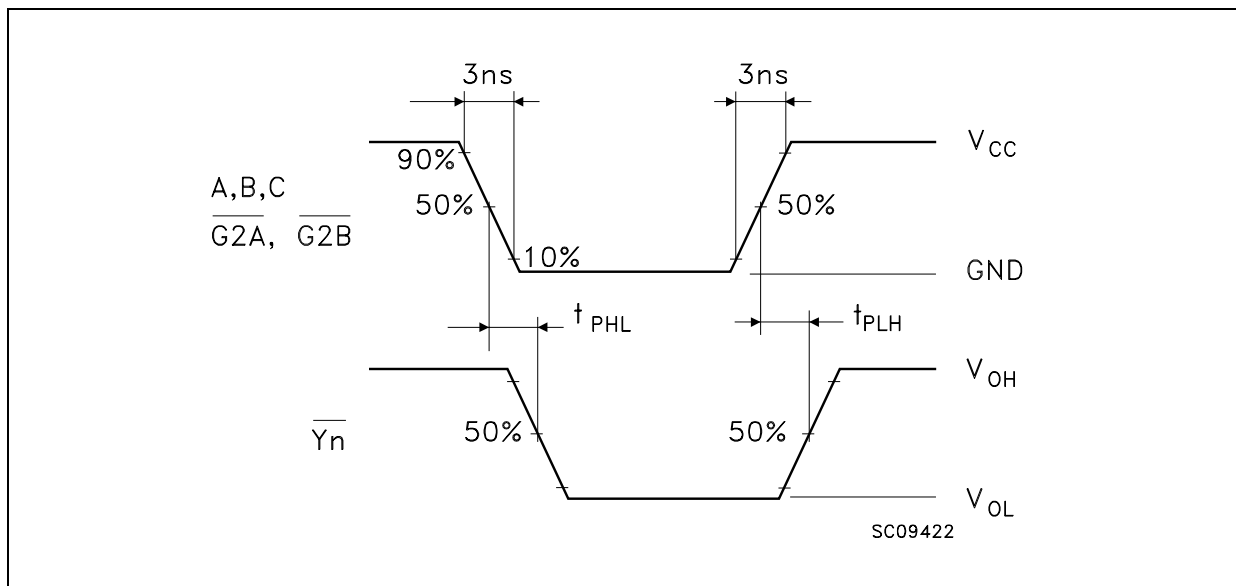
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)**TEST CIRCUIT** $C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance) $R_L = R_1 = 500\Omega$ or equivalent $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

74AC138

WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS ($f=1\text{MHz}$; 50% duty cycle)

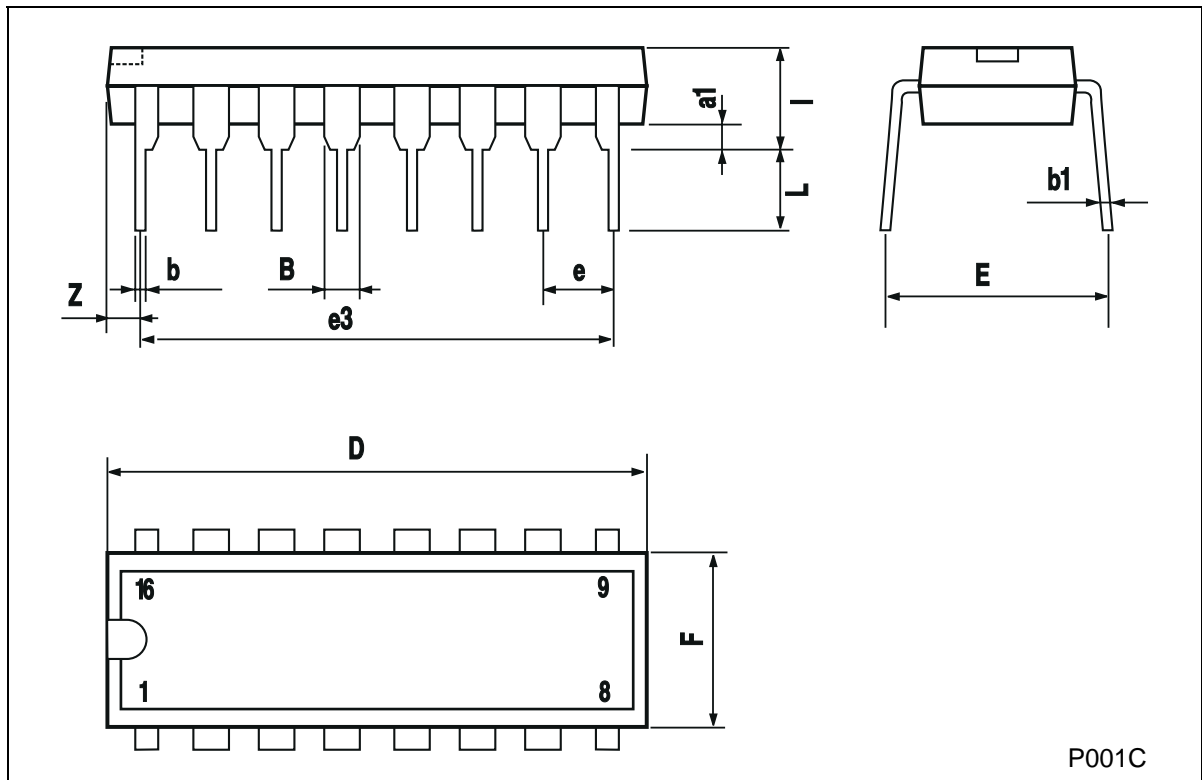


WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS ($f=1\text{MHz}$; 50% duty cycle)



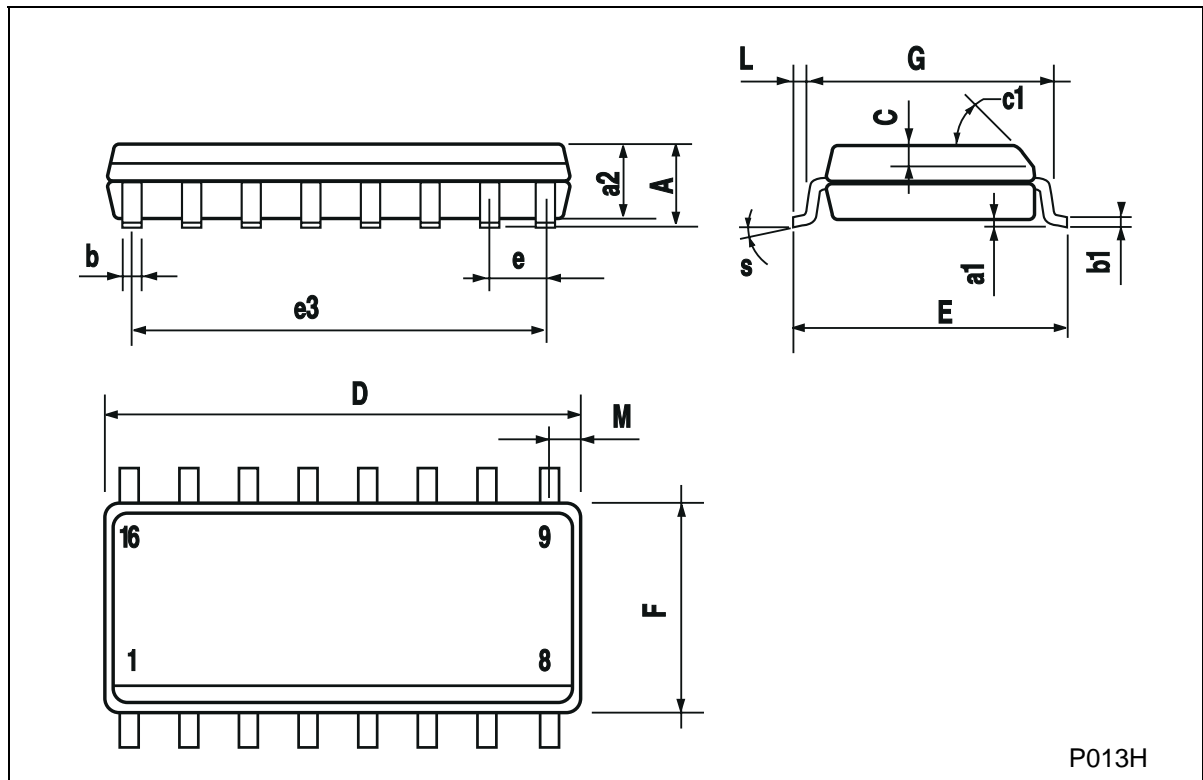
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



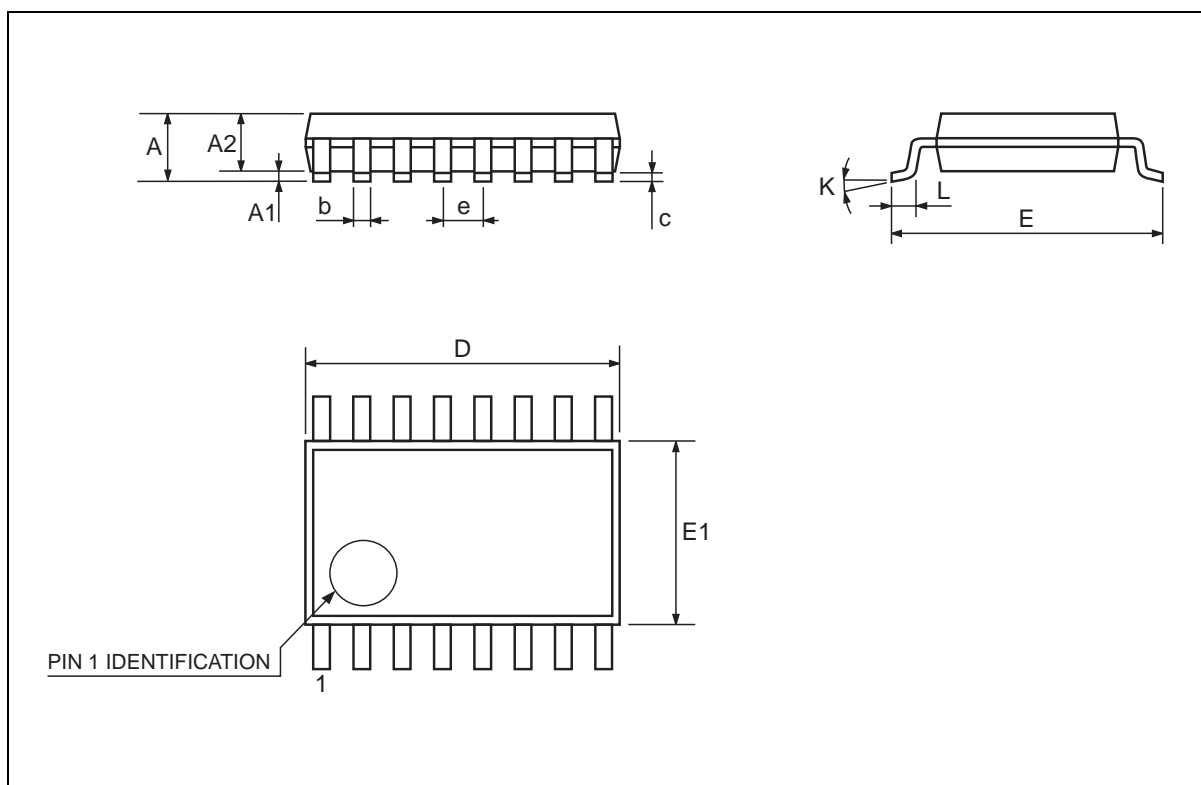
SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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