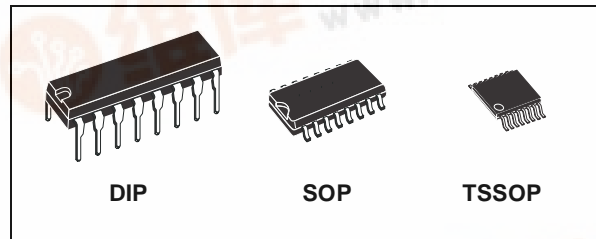




# 74ACT138

## 3 TO 8 LINE DECODER (INVERTING)

- HIGH SPEED:  $t_{PD} = 5ns$  (TYP.) at  $V_{CC} = 5V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu A$  (MAX.) at  $T_A = 25^\circ C$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2V$  (MIN.),  $V_{IL} = 0.8V$  (MAX.)
- $50\Omega$  TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24mA$  (MIN)
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC}$  (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 138
- IMPROVED LATCH-UP IMMUNITY



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	74ACT138B	
SOP	74ACT138M	74ACT138MTR
TSSOP		74ACT138TTR

### DESCRIPTION

The 74ACT138 is an advanced high-speed CMOS 3 TO 8 LINE DECODER (INVERTING) fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

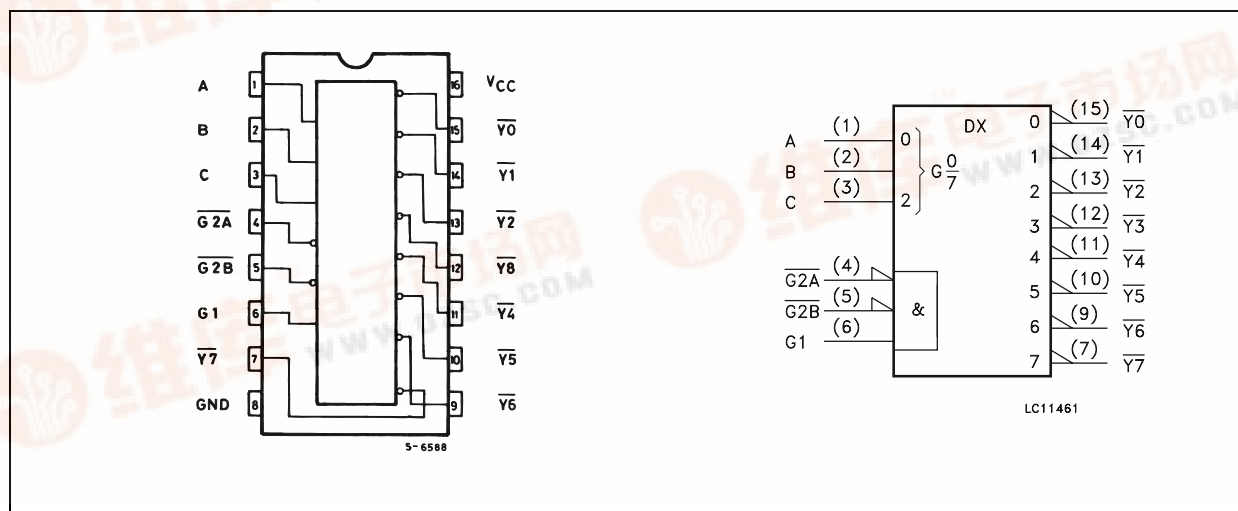
If the device is enabled, 3 binary select inputs (A, B, and C) determine which one of the outputs will go low. If enable input G1 is held low or either G2A or G2B is held high, the decoding function is inhibited and all the 8 outputs go to high.

Three enable inputs are provided to ease cascade connection and application of address decoders for memory systems.

The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels.

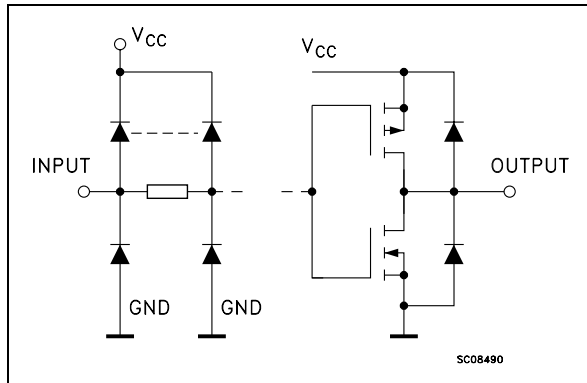
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



# 74ACT138

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

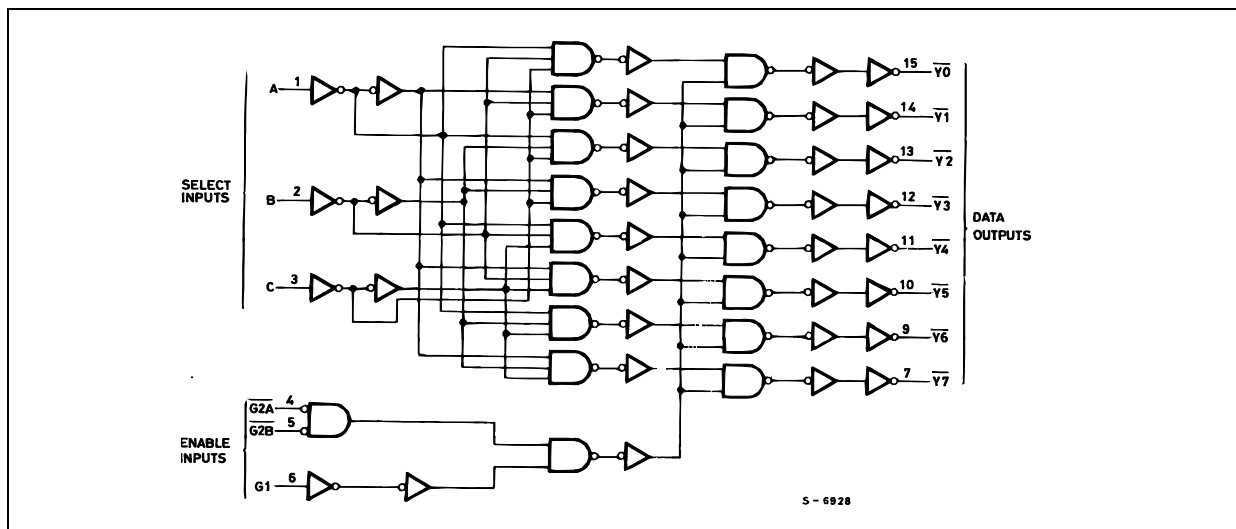
PIN No	SYMBOL	NAME AND FUNCTION
1, 2, 3	A, B, C	Address Inputs
4, 5	$\overline{G2A}$ , $\overline{G2B}$	Enable Inputs
6	$\overline{G1}$	Enable Input
15, 14, 13, 12, 11, 10, 9, 7	Y0 to Y7	Outputs
8	GND	Ground (0V)
16	V <sub>CC</sub>	Positive Supply Voltage

## TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	X	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

X : Don't Care

## LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to $5.5V$ (note 1)	8	ns/V

1)  $V_{IN}$  from 0.8V to 2.0V

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
V <sub>IL</sub>	Low Level Input Voltage	4.5	V <sub>O</sub> = 0.1 V or V <sub>CC</sub> -0.1V		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.49		4.4		4.4		V
		5.5	I <sub>O</sub> =-50 μA	5.4	5.49		5.4		5.4		
		4.5	I <sub>O</sub> =-24 mA	3.86			3.76		3.7		
		5.5	I <sub>O</sub> =-24 mA	4.86			4.76		4.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	V
		5.5	I <sub>O</sub> =50 μA		0.001	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
		5.5	I <sub>O</sub> =24 mA			0.36		0.44		0.5	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>CCCT</sub>	Max I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V		0.6			1.5		1.6	mA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA
I <sub>OLD</sub>	Dynamic Output Current (note 1, 2)	5.5	V <sub>OLD</sub> = 1.65 V max					75		50	mA
I <sub>OHD</sub>			V <sub>OHD</sub> = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω, Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time A, B, C to Y	5.0(*)			5.0	9.0		10.0		10.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time G1 to Y	5.0(*)			5.0	8.0		9.0		9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time G2A or G2B to Y	5.0(*)			5.5	8.5		10.0		10.5	ns

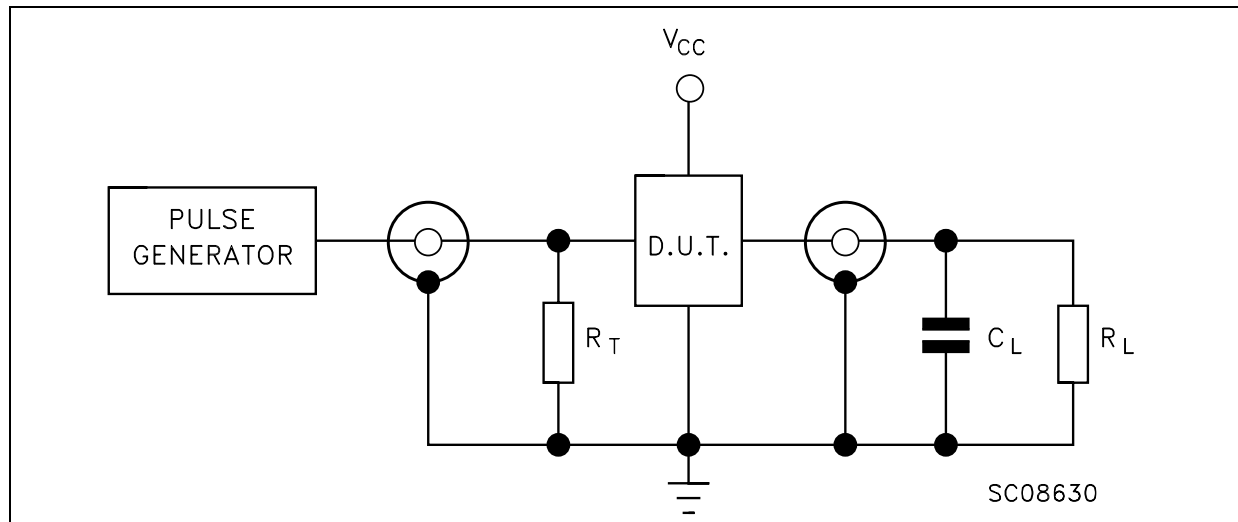
(\*) Voltage range is 5.0V ± 0.5V

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	5.0			4						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0	f <sub>IN</sub> = 10MHz		60						pF

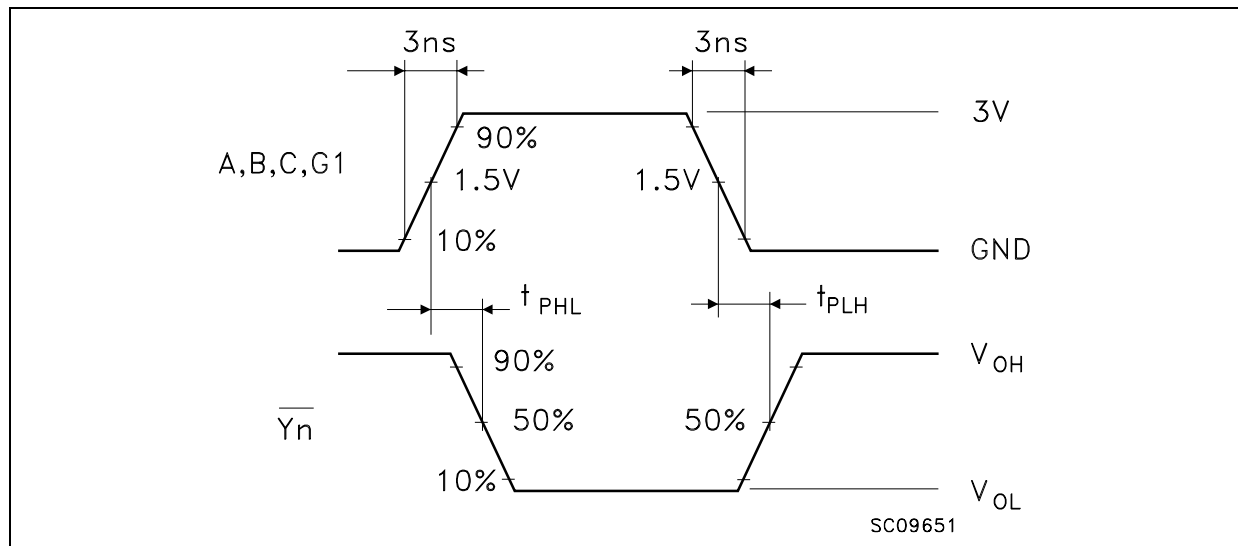
1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(OPR)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC/n</sub> (per circuit)

**TEST CIRCUIT**



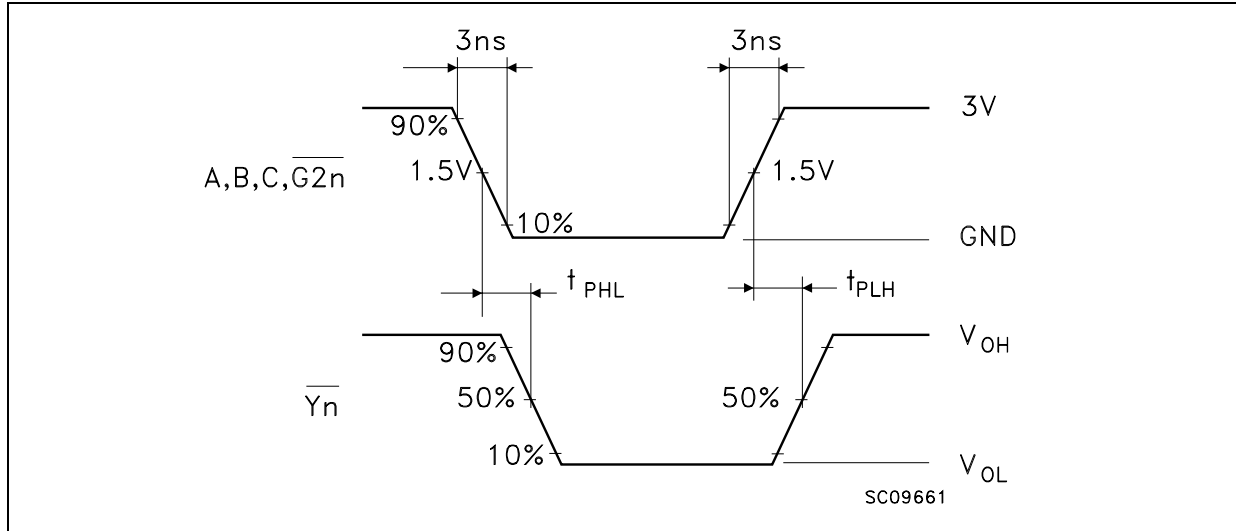
C<sub>L</sub> = 50pF or equivalent (includes jig and probe capacitance)  
 R<sub>L</sub> = R<sub>1</sub> = 500Ω or equivalent  
 R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

**WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS (f=1MHz; 50% duty cycle)**



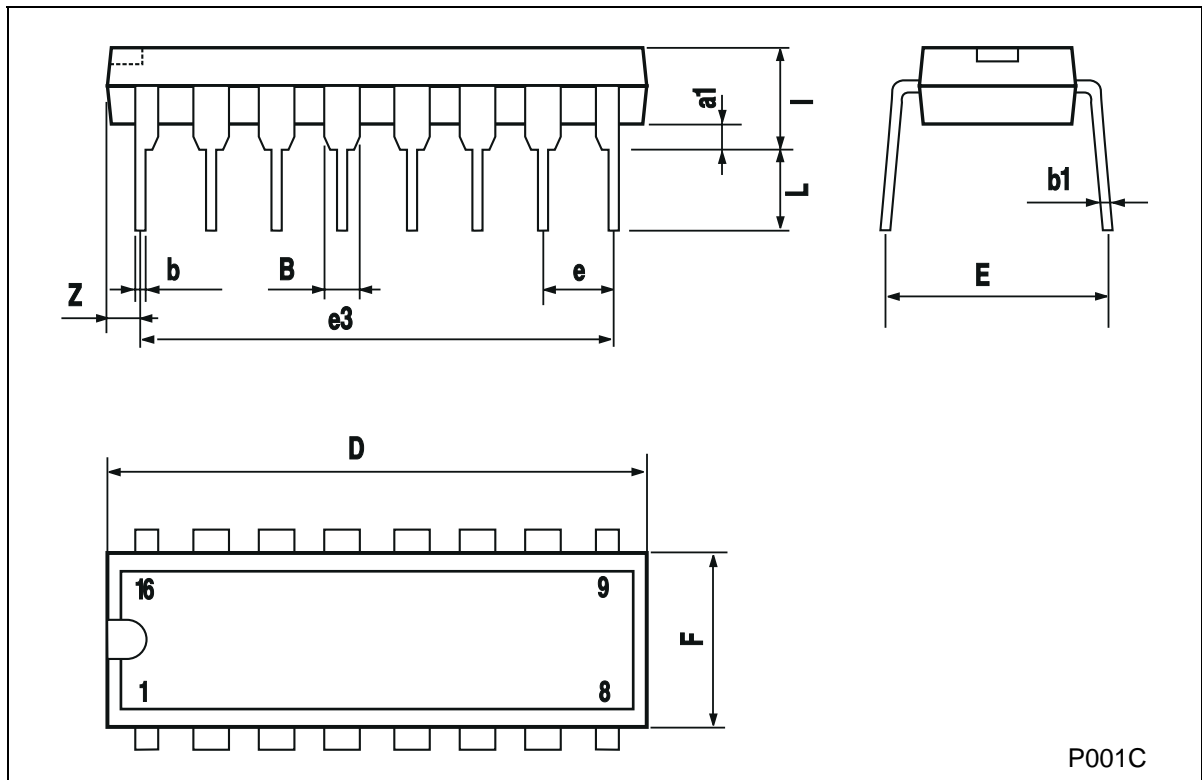
# 74ACT138

**WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS** ( $f=1\text{MHz}$ ; 50% duty cycle)



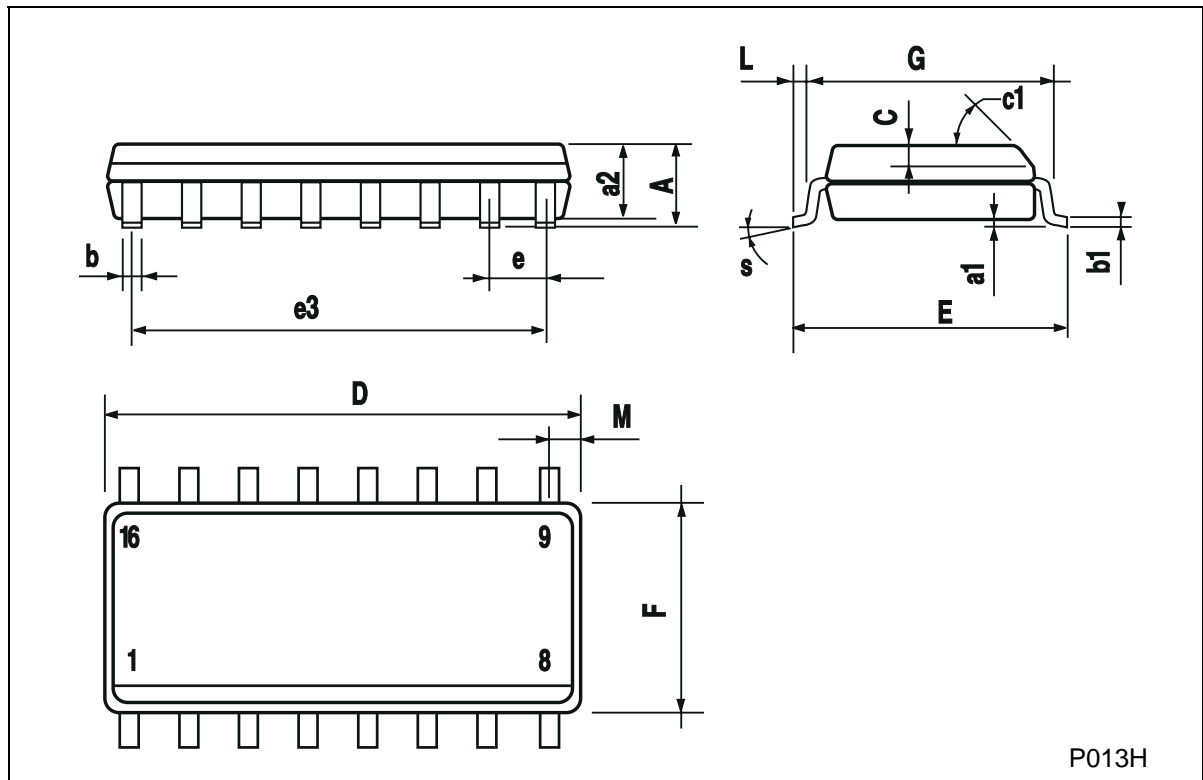
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



## SO-16 MECHANICAL DATA

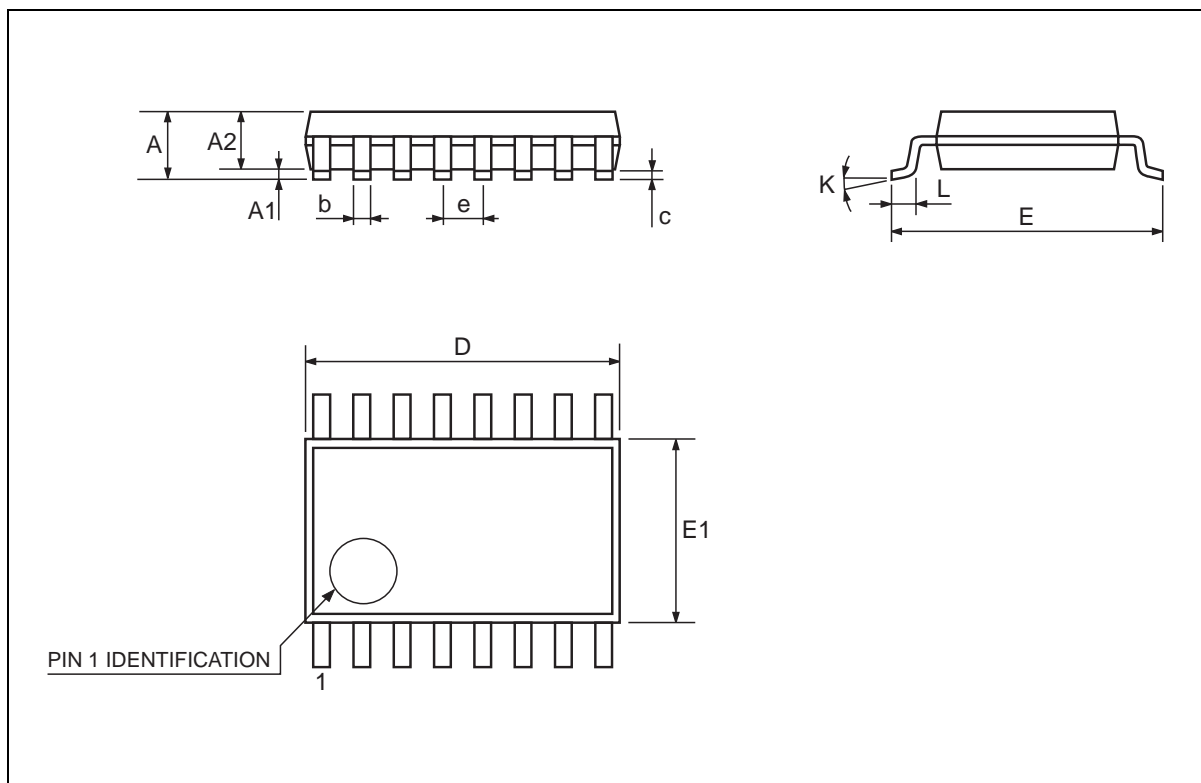
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					





## TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2001 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>