# CMOS 8–Bit Microcontrollers

# TMP90C041N/TMP90C041F

## 1. Outline and Characteristics

The TMP90C041 is a high-speed advanced 8-bit microcontroller applicable to a variety of equipment.

With its 8-bit CPU, A/D converter, multi-function timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90C041 allows the expansion of external memories for programs (up to 64K byte) and data (1M byte).

The TMP90C041N is a 64-pin shrink DIP product. (SDIP64-P750)

The TMP90C041F is a 64-pin flat package product. (QFP64-P1420A)

The characteristics of the TMP90C041 include:

(1) Powerful instructions: 163 basic instructions, including Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions

(2) Minimum instruction executing time:
320ns (at 12.5MHz oscillation frequency)

(3) Memory expansion
External program memory: 64K byte
External data memory: 1M byte

(4) 8-bit A/D converter (6 channels)

(5) General-purpose serial interface (1 Channel)
Asynchronous mode, I/O interface mode

(6) Multi-function 16-bit timer/event counter (1 channel)

(7) 8-bit timers (4 channels)

(8) Stepping motor control port (2 channels)

(9) Input/Output ports (28 pins)

(10) Interrupt function: 10 internal interrupts and 4 external interrupts

(11) Micro Direct Memory Access (μDMA) function (11 channels)

(12) Watchdog timer

(13) Standby function (4 HALT modes)

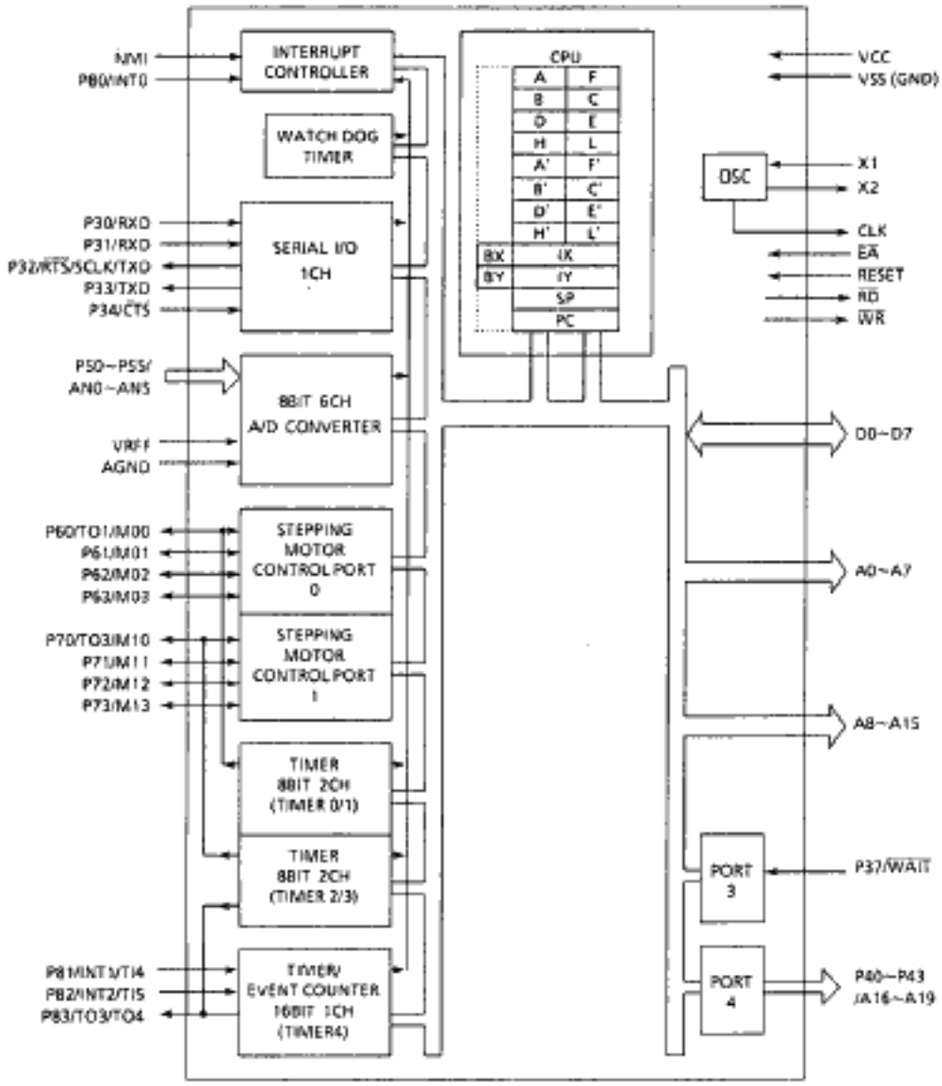



**Figure 1. TMP90C041 Block Diagram**

## 2. Pin Assignment and Functions

The assignment of input/output pins, their names and functions are described below.

### 2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP90C041N.

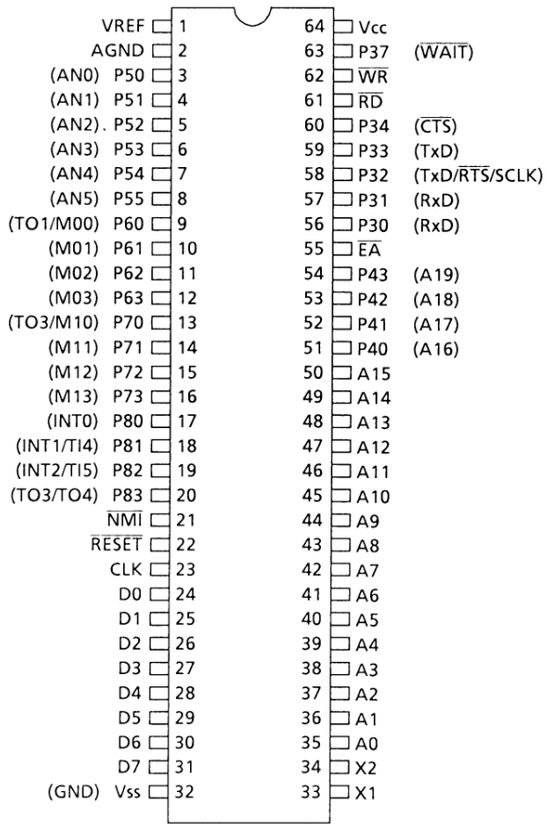



**Figure 2.1-(1). Pin Assignment (Shrink Dual Inline Package)**

Figure 2.1 (2) shows pin assignment of the TMP90C041F.

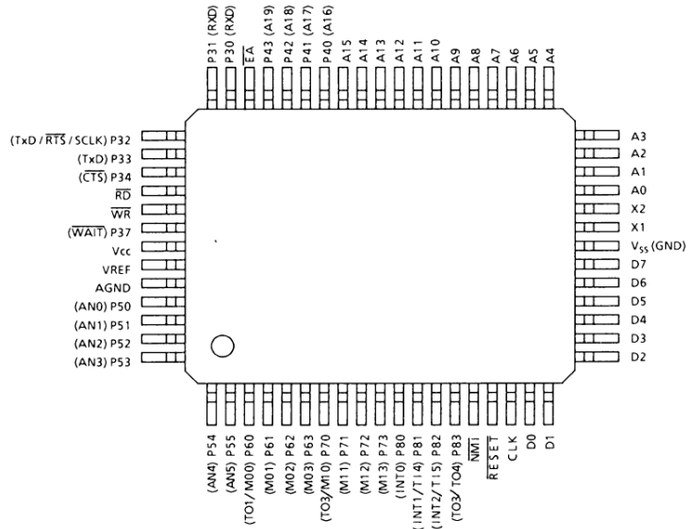



**Figure 2.1 (2). Pin Assignment (Flat Package)**

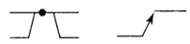
## 2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

**Table 2.2 Pin Names and Functions (1/2)**

| Pin Name | No. of pins | I/O 3 states | Function |
|---|---|---|---|
| D0 ~ D7 | 8 | 3 states | Data bus: Also functions as 8-bit bidirectional data bus for external memory |
| A0 ~ A7 | 8 | Output | Address bus: The lower 8 bits address bus for external memory |
| A8 ~ A15 | 8 | Output | Address bus: The upper 8 bits address bus for external memory |
| P30<br>/RxD | 1 | Input | Port 30: 1-bit input port<br>Receiver Serial Data |
| P31<br>/RxD | 1 | Input | Port 31: 1-bit input port<br>Receiver Serial Data |
| P32<br>/TxD<br>/$\overline{\text{RTS}}$<br>/SCLK | 1 | Output | Port 32: 1-bit input port<br>Transmitter Serial Data<br>Request to send Serial Data<br>Serial clock output |
| P33<br>/TxD | 1 | Output | Port 33: 1-bit output port<br>Transmitter Serial Data |
| P34<br>/$\overline{\text{CTS}}$ | 1 | Input | Port 34: 1-bit input port<br>Clear to send Serial Data |
| $\overline{\text{RD}}$ | 1 | Output | Read: Generates strobe signal for reading external memory |
| $\overline{\text{WR}}$ | 1 | Output | Write: Generates strobe signal for writing into external memory |
| P37<br>/$\overline{\text{WAIT}}$ | 1 | Input | Port 37: 1-bit input port<br>Wait: Input pin for connecting slow speed memory or peripheral LSI |

**Table 2.2 Pin Names and Functions (2/2)**

| Pin Name | No. of Pins | I/O 3 states | Function |
|---|---|---|---|
| P40 ~ P43<br>/A16 ~ A19 | 4 | Output | Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis |
| | | | Address bus: Also functions as address bus for external memory (4 bits of bank address) |
| P50 ~ P55<br>/AN0 ~ AN5 | 6 | Input | Port 5: 6-bit input port |
| | | | Analog input: 6 analog input to A/D converter |
| VREF | 1 | – | Input of reference voltage to A/D converter |
| AGND | 1 | – | Ground pin for A/D converter |
| P60 ~ P63<br>/M00 ~ M03<br>/TO1 | 4 | I/O | Port 6: 4-bit I/O port that allows I/O selection on bit basis |
| | | Output | Stepping motor control port 0 |
| | | Output | Timer output 1: Output of Timer 0 or 1 |
| P70 ~ P73<br>/M10 ~ M13<br>/TO3 | 4 | I/O | Port 7: 4-bit I/O port that allows I/O selection on bit basis |
| | | Output | Stepping motor control port 1 |
| | | Output | Timer output 3: Output of Timer 2 or 3 |
| P80<br>/INT0 | 1 | Input | Port 80: 1-bit input port |
| | | | Interrupt request pin 0: Interrupt request pin (Level/rising edge is programmable)  |
| P81<br>/INT1<br>/TI4 | 1 | Input | Port 81: 1-bit input port |
| | | | Interrupt request pin 1: Interrupt request pin (Rising/falling edge is programmable)  |
| | | | Timer input 4: Counter/capture trigger signal for Timer 4 |
| P82<br>/INT2<br>/TI5 | 1 | Input | Port 82: 1-bit input port |
| | | | Interrupt request pin 2: rising edge interrupt request pin |
| | | | Timer input 5: capture trigger signal for Timer 4 |
| P83<br>/TO3/T04 | 1 | Output | Port 83: 1-bit output port |
| | | | Timer output 3/4: Output of Timer 2, 3 or 4 |
| $\overline{\text{NMI}}$ | 1 | Input | Non-maskable interrupt request pin: Falling edge interrupt request pin  |
| CLK | 1 | Output | Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting. |
| $\overline{\text{EA}}$ | 1 | Input | External access: Connects with GND pin in the TMP90C041 with no internal ROM. |
| $\overline{\text{RESET}}$ | 1 | Input | Reset: Initializes the TMP90C041. (Built-in pull-up resistor) |
| X1/X2 | 2 | Input/<br>Output | Pin for quartz crystal or ceramic resonator |
| $V_{CC}$ | 1 | – | Power supply (+5V) |
| $V_{SS}$ (GND) | 1 | – | Ground (0V) |

# 3. Operation

The following explains the TMP90C041 functions and basic operations.

The CPU functions and internal I/O functions of the TMP90C041 are the same as the TMP90C840A.

Refer to the "TMP90C840A" section concerning functions which are not explained in the following.

## 3.1 CPU

The TMP90C041 has an internal high-performance 8-bit CPU.

Refer to the book TLCS Series CPU Core Architecture concerning CPU operation.

## 3.2 Memory Map

The TMP90C041 supports a program memory of up to 64K bytes and a data memory of maximum 1M bytes.

The program memory may be assigned to the address space from 00000H to 0FFFFH, while the data memory can be allocated to any address from 00000H to FFFFFH.

(1) Internal I/O

The TMP90C041 provides a 48-byte address space as an internal I/O area, whose addresses range from FFC0H to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3.1 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.

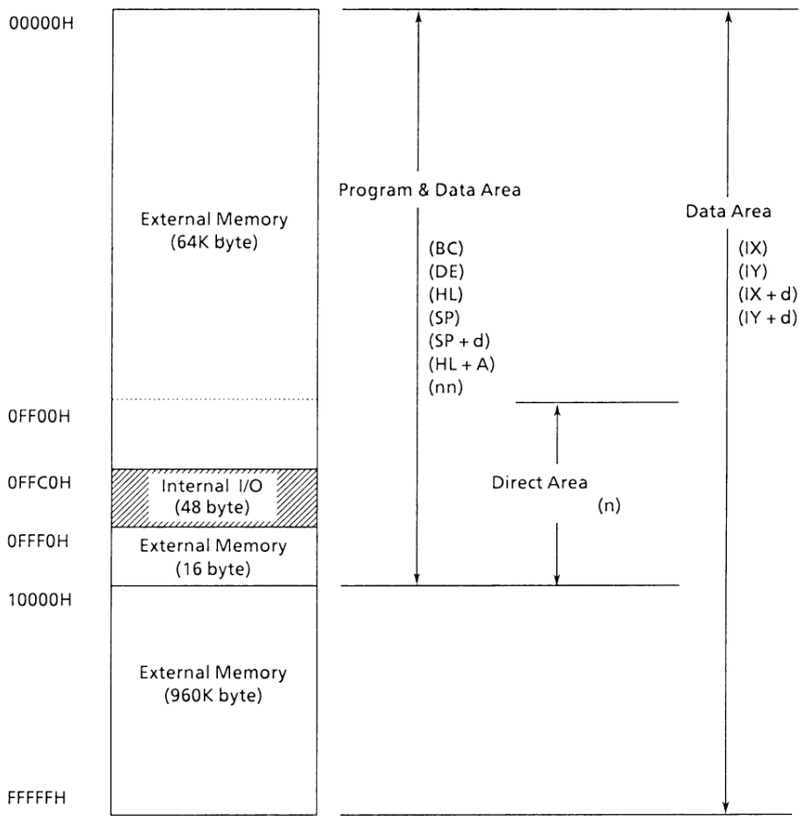


**Figure 3.2. Memory Map**

# 4. Electrical Characteristics

TMP90C041N/TMP90C041F

## 4.1 Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | -0.5 ~ + 7 | V |
| $V_{IN}$ | Input voltage | -0.5 ~ $V_{CC}$ + 0.5 | V |
| $P_D$ | Power dissipation (Ta = 70°C) | F 500 | mW |
| | | N 600 | |
| $T_{SOLDER}$ | Soldering temperature (10s) | 260 | °C |
| $T_{STG}$ | Storage temperature | -65 ~ 150 | °C |
| $T_{OPR}$ | Operating temperature | -20 ~ 70 | °C |

## 4.2 DC Characteristics

**TA = -20 ~ 70°C $V_{CC}$ = 5V ± 10%**
**Typical Values are for TA = 25°C and $V_{CC}$ = 5V.**

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (D0 ~ D7) | -0.3 | 0.2$V_{CC}$ - 0.1 | V | – |
| $V_{IL1}$ | P3, P5, P6, P7, P8 | -0.3 | 0.3$V_{CC}$ | V | – |
| $V_{IL2}$ | $\overline{RESET}$, INT0, $\overline{NMI}$ | -0.3 | 0.25$V_{CC}$ | V | – |
| $V_{IL4}$ | X1 | -0.3 | 0.2$V_{CC}$ | V | – |
| $V_{IH}$ | Input Low Voltage (D0 ~ D7) | 0.2$V_{CC}$ + 1.1 | $V_{CC}$ + 0.3 | V | – |
| $V_{IH1}$ | P3, P5, P6, P7, P8 | 0.7$V_{CC}$ | $V_{CC}$ + 0.3 | V | – |
| $V_{IH2}$ | $\overline{RESET}$, INT0, NMI | 0.75$V_{CC}$ | $V_{CC}$ + 0.3 | V | – |
| $V_{IH4}$ | X1 | 0.8$V_{CC}$ | $V_{CC}$ + 0.3 | V | – |
| $V_{OL}$ | Output Low Voltage | – | 0.45 | V | $I_{OL}$ = 1.6mA |
| $V_{OH}$<br>$V_{OH1}$<br>$V_{OH2}$ | Output High Voltage | 2.4<br>0.75$V_{CC}$<br>0.9$V_{CC}$ | – | V<br>V<br>V | $I_{OH}$ = -400µA<br>$I_{OH}$ = -100µA<br>$I_{OH}$ = -20µA |
| $I_{DAR}$ | Darlington Drive Current<br>(8 I/O pins) | -1.0 | -3.5 | mA | $V_{EXT}$ = 1.5V<br>$R_{EXT}$ = 1.1kΩ |
| $I_{LI}$ | Input Leakage Current | 0.02 (Typ) | ±5 | µA | 0.0 ≤ Vin ≤ $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | 0.05 (Typ) | ±10 | µA | 0.2 ≤ Vin ≤ $V_{CC}$ - 0.2 |
| $I_{CC}$ | Operating Current (RUN)<br>Idle 1<br>Idle 2 | 20 (Typ)<br>1.5 (Typ)<br>9 (Typ) | 40<br>5<br>15 | mA<br>mA<br>mA | tosc = 12.5MHz |
| | STOP (TA = -20 ~ 70°C)<br>STOP (TA = 0 ~ 50°C) | 0.2 (Typ) | 50<br>10 | µA<br>µA | 0.2 ≤ Vin ≤ $V_{CC}$ - 0.2 |
| $R_{RST}$ | $\overline{RESET}$ Pull Up Register | 50 | 150 | KΩ | – |
| CIO | Pin Capacitance | – | 10 | pF | testfreq = 1MHz |
| $V_{TH}$ | Schmitt width $\overline{RESET}$, $\overline{NMI}$, INT0 | 0.4 | 1.0 (Typ) | V | – |

Note: $I_{DAR}$ is guaranteed for a total of up to 8 optional ports.

### 4.3 AC Characteristics

**TA = -20 ~ 70°C $V_{CC}$ = 5V ± 10%**
**CL = 50pF**

| Symbol | Parameter | Variable | | 10MHz Clock | | 12.5MHz Clock | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{OSC}$ | OSC. Period = x | 80 | 1000 | 100 | - | 80 | – | ns |
| $t_{CYC}$ | CLK Period | 4x | 4x | 400 | – | 320 | – | ns |
| $t_{WL}$ | CLK Low width | 2x - 40 | – | 160 | – | 120 | – | ns |
| $t_{WH}$ | CLK High width | 2x - 40 | – | 160 | – | 120 | – | ns |
| $t_{AC}$ | Address Setup to $\overline{RD}$, $\overline{WR}$ | x - 45 | – | 55 | – | 35 | – | ns |
| $t_{RR}$ | $\overline{RD}$ Low width | 2.5x - 40 | – | 210 | – | 160 | – | ns |
| $t_{CA}$ | Address Hold Time After $\overline{RD}$, $\overline{WR}$ | 0.5x - 30 | – | 20 | – | 10 | – | ns |
| $t_{AD}$ | Address to Valid Data In | - | 3.5x - 95 | – | 255 | – | 185 | ns |
| $t_{RD}$ | $\overline{RD}$ to Valid Data In | - | 2.5x - 80 | – | 170 | – | 120 | ns |
| $t_{HR}$ | Input Data Hold After $\overline{RD}$ | 0 | – | 0 | – | 0 | – | ns |
| $t_{WW}$ | $\overline{WR}$ Low width | 2.5x - 40 | – | 210 | – | 160 | – | ns |
| $t_{DW}$ | Data Setup to $\overline{WR}$ | 2x - 50 | – | 150 | – | 110 | – | ns |
| $t_{WD}$ | Data Hold After $\overline{WR}$ | 30 | 90 | 30 | 90 | 30 | 90 | ns |
| $t_{CWA}$ | $\overline{RD}$, $\overline{WR}$ to Valid $\overline{WAIT}$ | – | 1.5x - 100 | – | 50 | – | 20 | ns |
| $t_{AWA}$ | Address to Valid $\overline{WAIT}$ | – | 2.5x - 130 | – | 120 | – | 70 | ns |
| $t_{WAS}$ | $\overline{WAIT}$ Setup to CLK | 70 | – | 70 | – | 70 | – | ns |
| $t_{WAH}$ | $\overline{WAIT}$ Hold After CLK | 0 | – | 0 | – | 0 | – | ns |
| $t_{RV}$ | $\overline{RD}$/$\overline{WR}$ Recovery Time | 1.5x - 35 | – | 115 | – | 85 | – | ns |
| $t_{CPW}$ | CLK to Port Data Output | – | x + 200 | – | 300 | – | 280 | ns |
| $t_{PRC}$ | Port Data Setup to CLK | 200 | – | 200 | – | 200 | – | ns |
| $t_{CPR}$ | Port Data Hold After CLK | 100 | – | 100 | – | 100 | – | ns |
| $t_{CHCL}$ | $\overline{RD}$/$\overline{WR}$ Hold After CLK | x-60 | – | 40 | – | 20 | – | ns |
| $t_{CLC}$ | $\overline{RD}$/$\overline{WR}$ Setup to CLK | 1.5x - 25 | – | 100 | – | 70 | – | ns |
| $t_{CLHA}$ | Address Hold After CLK | 1.5x - 80 | – | 70 | – | 40 | – | ns |
| $t_{ACL}$ | Address Setup to CLK | 2.5x - 80 | – | 170 | – | 120 | – | ns |
| $t_{CLD}$ | Data Setup to CLK | x - 50 | – | 50 | – | 30 | – | ns |

- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 – D7)
  High $0.8V_{CC}$/Low $0.2V_{CC}$ (excluding D0 – D7)

### 4.4 A/D Conversion Characteristics

**TA = -20 ~ 70°C $V_{CC}$ = 5V ± 10%**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{REF}$ | Analog reference voltage | $V_{CC}$ - 1.5 | $V_{CC}$ | $V_{CC}$ | V |
| $A_{GND}$ | Analog reference voltage | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | |
| $V_{AIN}$ | Allowable analog input voltage | $V_{SS}$ | – | $V_{CC}$ | |
| $I_{REF}$ | Supply current for analog reference voltage | – | 0.5 | 1.0 | mA |
| Error | Total error (TA = 25°C, $V_{CC}$ = $V_{REF}$ = 5.0V) | – | – | 1.0 | LSB |
| | Total error | – | – | 2.5 | |

### 4.5 Zero-Cross Characteristics

**TA = -20 ~ 70°C $V_{CC}$ = 5V ± 10%**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{ZX}$ | Zero-cross detection input | AC coupling C = 0.1μF | 1 | 1.8 | VAC p - p |
| $A_{ZX}$ | Zero-cross accuracy | 50/60Hz sine wave | – | 135 | mV |
| $F_{ZX}$ | Zero-cross detection input frequency | – | 0.04 | 1 | kHz |

### 4.6 Serial Channel Timing-I/O Interface Mode

**TA = –20 ~ 70°C $V_{CC}$ = 5V ± 10%**
**CL = 50pF**

| Symbol | Parameter | Variable | | 10MHz Clock | | 12.5MHz Clock | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{SCY}$ | Serial Port Clock Cycle Time | 8x | – | 800 | – | 640 | – | ns |
| $t_{OSS}$ | Output Data Setup SCLK Rising Edge | 6x - 150 | – | 450 | – | 330 | – | ns |
| $t_{OHS}$ | Output Data Hold After SCLK Rising Edge | 2x - 120 | – | 80 | – | 40 | – | ns |
| $t_{HSR}$ | Input Data Hold After SCLK Rising Edge | 0 | – | 0 | – | 0 | – | ns |
| $t_{SRD}$ | SCLK Rising Edge to Input DATA Valid | – | 6x - 150 | – | 450 | – | 330 | ns |

### 4.7 16-bit Event Counter

**TA = –20 ~ 70°C $V_{CC}$ = 5V ± 10%**

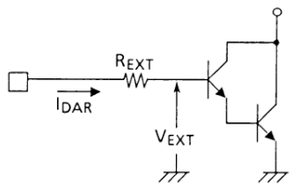
| Symbol | Parameter | Variable | | 10MHz Clock | | 12.5MHz Clock | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{VCK}$ | TI4 clock cycle | 8x + 100 | – | 900 | – | 740 | – | ns |
| $t_{VCKL}$ | TI4 Low clock pulse width | 4x + 40 | – | 440 | – | 360 | – | ns |
| $t_{VCKH}$ | TI4 High clock pulse width | 4x + 40 | – | 440 | – | 360 | – | ns |

### 4.8 Interrupt Operation

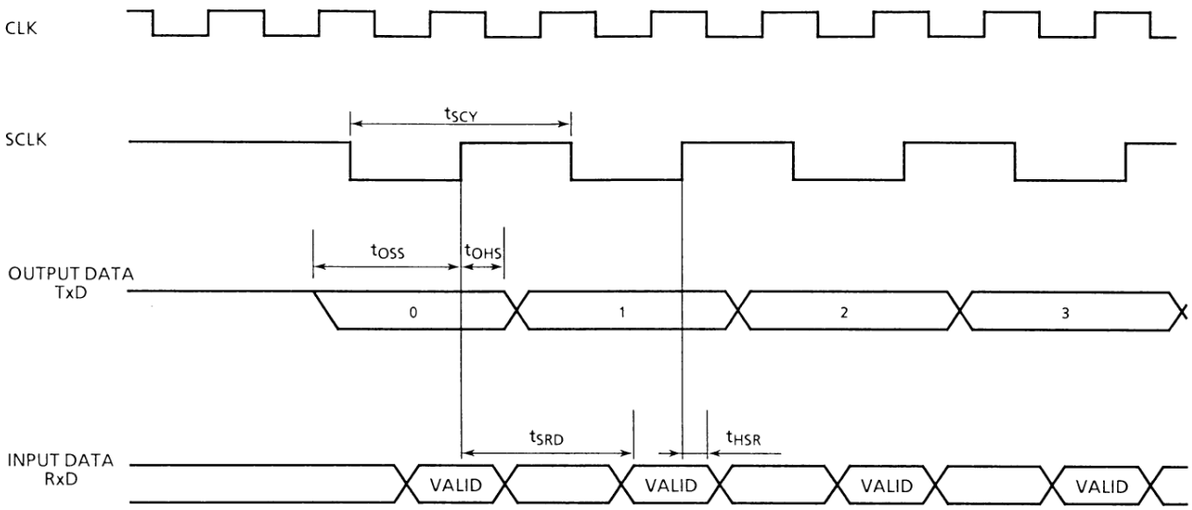
**TA = -20 ~ 70°C $V_{CC}$ = 5V ± 10%**

| Symbol | Parameter | Variable | | 10MHz Clock | | 12.5MHz Clock | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{INTAL}$ | $\overline{NMI}$, INT0 Low level pulse width | 4x | – | 400 | – | 320 | – | ns |
| $t_{INTAH}$ | $\overline{NMI}$, INT0 High level pulse width | 4x | – | 400 | – | 320 | – | ns |
| $t_{INTBL}$ | INT1, INT2 Low level pulse width | 8x + 100 | – | 900 | – | 740 | – | ns |
| $t_{INTBH}$ | INT1, INT2 High level pulse width | 8x + 100 | – | 900 | – | 740 | – | ns |

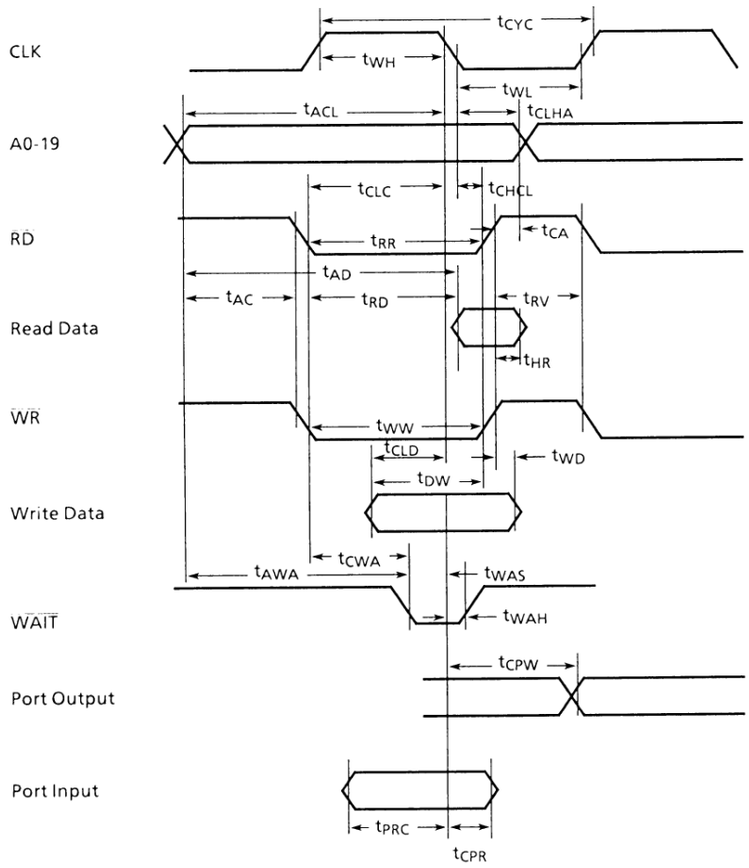
**(Reference) Definition of $I_{DAR}$**




### 4.9 I/O Interface Mode Timing Chart



### 4.10 Timing Chart



## 5. Differences Between TMP90C841A and TMP90C041

Specifications of TMP90C841A and TMP90C041 are the same except below.

TMP90C841A system, not using internal RAM and internal I/O functions as shown below, can be substituted by TMP90C041 system. To substitute the TMP90C841A system using the internal RAM by the TMP90C041 system, it is necessary to attach the external RAM to the address corresponded to the internal address.

| Name | TMP90C841A | TMP90C041 |
|---|---|---|
| RAM | 256 bytes of internal RAM are provided. (0FEC0H ~ 0FFBFH) | External memory area. |
| A0 ~ A15 | High-Impedance state during reset | Driving state during reset. |
| P0 (0FFC1H)<br>P1 (0FFC1H)<br>P2 (0FFC4H) | Provided<br>(same chip as TMP90C840A) | R/W function is not provided. |
| P01CR (0FFC2H) | Provided | EXT, P1C, P0C is not provided. |
| P2CR (0FFC5H) | Provided | P2XC register is not provided |

* Note: Connect $\overline{EA}$ pin with GND pin.