TEXAS INSTRUMENTS

CY29FCT520T

SCCS011A - May 1994 - Revised April 2000

Multi-Level Pipeline Register

Features

- **Function, pinout, and drive compatible with FCT, F Logic, and AM29520**
- **FCT-C speed at 6.0 ns max. (Com'l), FCT-B speed at 7.5 ns max. (Com'l), FCT-A speed at 14.0 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-Off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Sink current 64 mA (Com'l), 32 mA (Mil)**
  Source current 32 mA (Com'l), 12 mA (Mil)
- **Single and dual pipeline operation modes**
- **Multiplexed data inputs and outputs**

Functional Description

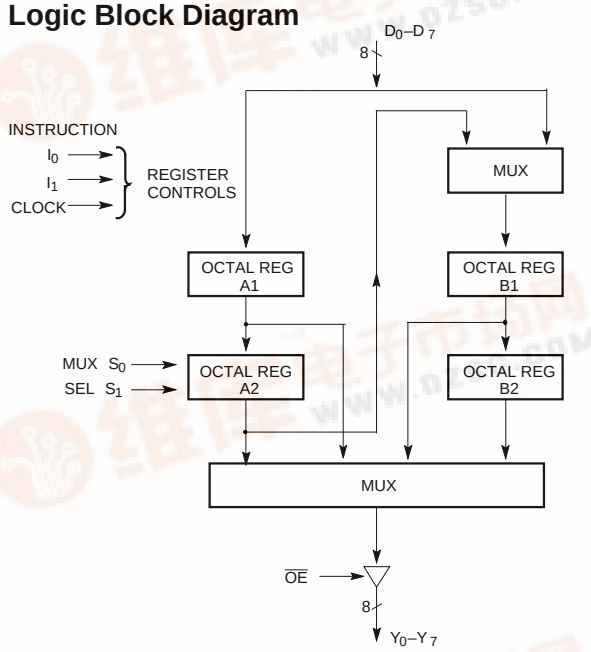
The CY29FCT520T devices are multilevel 8-bit-wide pipeline registers. The devices consist of four registers, A1, A2, B1, and B2, which are configured by the instruction inputs I_0, I_1 as a single 4-level pipeline or as two two-level pipelines. The contents of any register may be read at the multiplexed output at any time by using the mux-selection controls S_0 and S_1.

The pipeline registers are positive edge triggered and data is shifted by the rising edge of the clock input. Instruction I=0 selects the four-level pipeline mode. Instruction I=1 selects the two-level B pipeline while I=2 selects the two-level A pipeline. I=3 is the HOLD instruction; no shifting is performed by the clock in this mode.

In the two-level operation mode, data is shifted from level 1 to level 2 and new data is loaded into level 1.

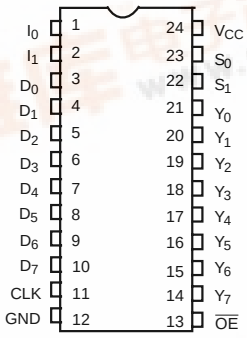
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

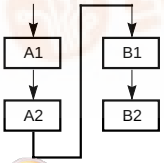
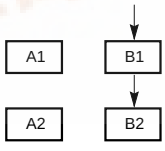
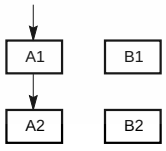
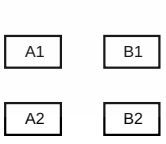


Pin Configurations

DIP, SOIC, QSOP, CDIP
Top View



Pipeline Instruction Table

I = 0		I = 1		I = 2		I = 3	
I_1 = 0	I_0 = 0	I_1 = 0	I_0 = 1	I_1 = 1	I_0 = 0	I_1 = 1	I_0 = 1
							
Single four-level		Dual two-level				Hold	

Output Selection Mux Table

Inputs.		
S_1	S_0	Output
1	1	A1
1	0	A2
0	1	B1
0	0	B2

Maximum Ratings[1, 2]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–65°C to +135°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

DC Output Voltage..... –0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....120 mA

Power Dissipation 0.5W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature[3]	V_{CC}
Commercial	–40°C to +85°C	5V ± 5%
Military	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[4]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=–15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=–12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[5]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	$V_{CC=}$Max., V_{OUT}=2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC}=Max., V_{OUT} = 0.5V				–10	µA
I_{OS}	Output Short Circuit Current[6]	V_{CC}=Max., V_{OUT}=0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Capacitance[5]

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		9	12	pF

Notes:

1. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. T_A is the "instant on" case temperature.
4. Typical values are at V_{CC}=5.0V, T_A=+25˚C ambient.
5. This parameter is specified but not tested.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[4]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V, f_1=0, Outputs Open [7]	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[8]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[9]	V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.7	1.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, Eight Bits Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	2.8	5.6[10]	mA
		V_{CC}=Max., 50% Duty Cycle, Outputs Open, f_0=10 MHz, Eight Bits Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	5.1	14.3[10]	mA

Notes:

7. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC}+\Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
   D_H = Duty Cycle for TTL inputs HIGH
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
   f_0 = Clock frequency for registered devices, otherwise zero
   f_1 = Input signal frequency
   N_1 = Number of inputs changing at f_1
   All currents are in milliamps and all frequencies are in megahertz.
10. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[11]

Parameter	Description	CY29FCT520AT				CY29FCT520BT				Unit	Fig. No.[12]
		Military		Commercial		Military		Commercial			
		Min	Max.	Min	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Data Output	2.0	16.0	2.0	14.0	2.0	8.0	2.0	7.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Data Output	2.0	15.0	2.0	13.0	2.0	8.0	2.0	7.5	ns	1, 5
t_S	Set-Up Time Input Data to Clock	6.0		5.0		2.8		2.5		ns	4
t_H	Hold Time Input Data to Clock	2.0		2.0		2.0		2.0		ns	4
t_S	Set-Up Time Instruction (Reg. Enable) to Clock	6.0		5.0		4.5		4.0		ns	4
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0		2.0		2.0		2.0		ns	4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	13.0	1.5	12.0	1.5	7.5	1.5	7.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time	1.5	16.0	1.5	15.0	1.5	8.0	1.5	7.5	ns	1, 7, 8
t_W	Clock Pulse Width,[5] HIGH or LOW	8.0		7.0		6.0		5.5		ns	5

Parameter	Description	CY29FCT520CT		Unit	Fig. No.[12]
		Commercial			
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Data Output	2.0	6.0	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Data Output	2.0	6.0	ns	1, 5
t_S	Set-Up Time Input Data to Clock	2.5		ns	4
t_H	Hold Time Input Data to Clock	2.0		ns	4
t_S	Set-Up Time Instruction (Reg. Enable) to Clock	4.0		ns	4
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0		ns	4
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	6.0	ns	1, 7, 8
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.0	ns	1, 7, 8
t_W	Clock Pulse Width,[5] HIGH or LOW	5.5		ns	5

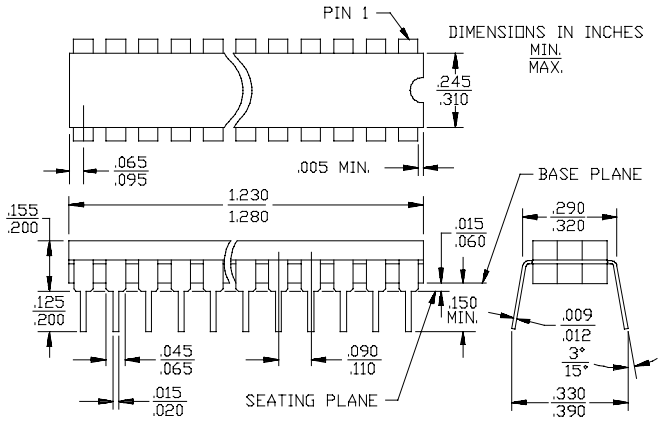
Notes:
11. Minimum limits are specified but not tested on Propagation Delays.
12. See “Parameter Measurement Information” in the General Information section.

Ordering Information

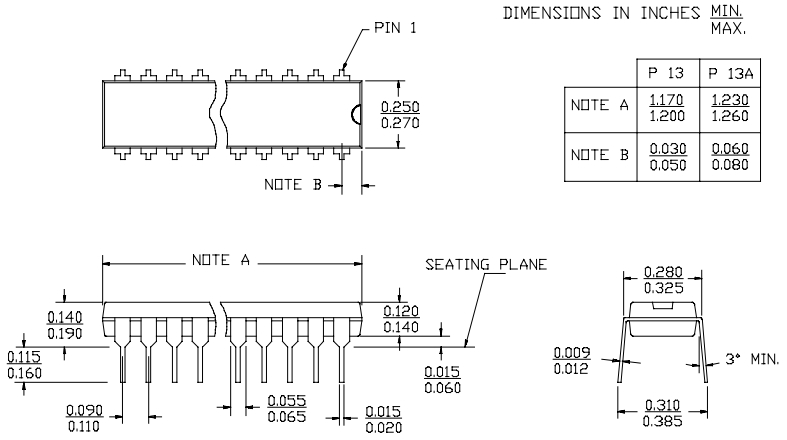
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY29FCT520CTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	Commercial
7.5	CY29FCT520BTSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	Commercial
8.0	5962-9220504MLA (CY29FCT520BTDMB)	D14	24-Lead (300-Mil) CDIP	Military
14.0	CY29FCT520ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY29FCT520ATSOC/SOCT	S13	24-Lead (300-Mil) Molded SOIC	
16.0	5962-9220502MLA (CY29FCT520ATDMB)	D14	24-Lead (300-Mil) CDIP	Military

Package Diagrams

24-Lead (300-Mil) CDIP D14
MIL-STD-1835 D- 9 Config.A



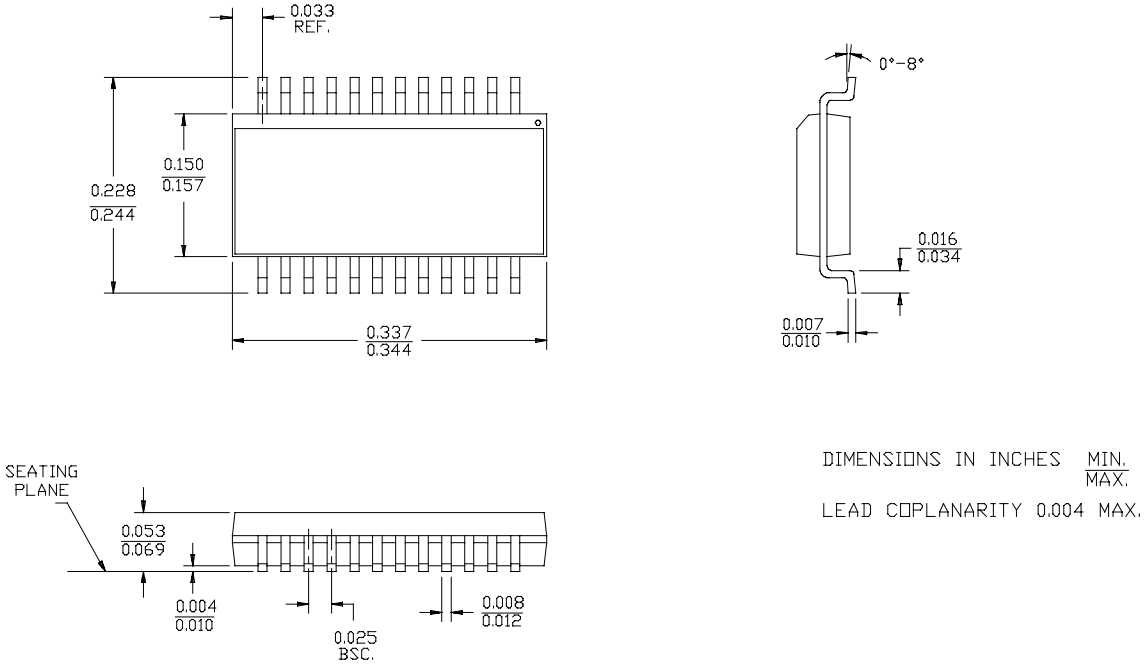
24-Lead (300-Mil) Molded DIP P13/P13A



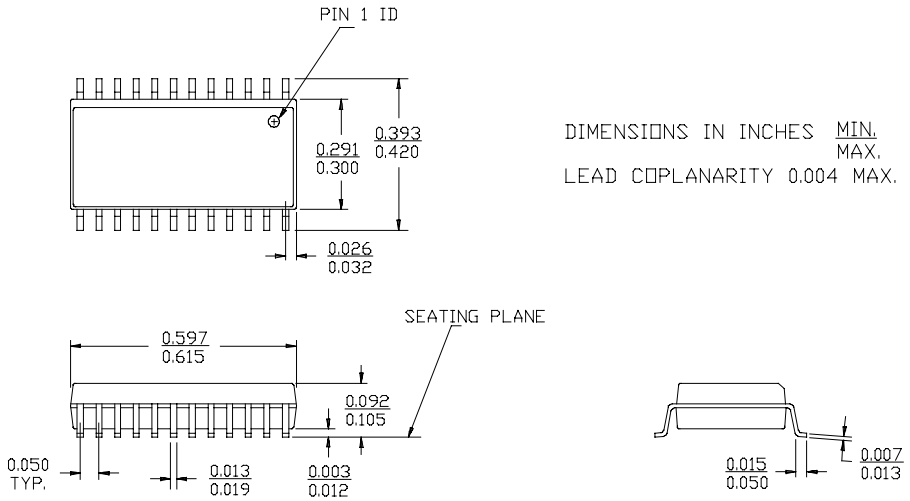
	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

Package Diagrams (continued)

24-Lead Quarter Size Outline Q13



24-Lead (300-Mil) Molded SOIC S13



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