

RT9222 Data Sheet



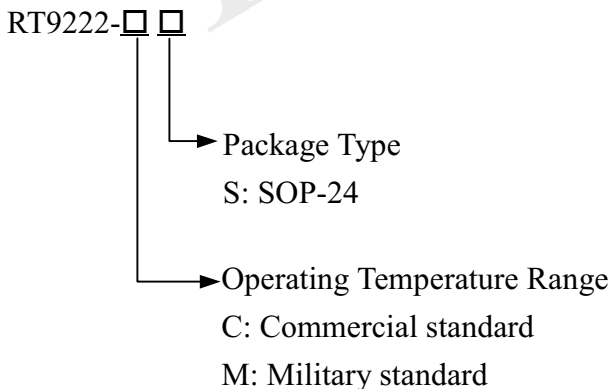
Programmable Synchronous PWM Buck Converter with Dual Adjustable Low Dropout Linear Regulator Controller

General Description

The RT9222 integrates a PWM controller and two low-dropout linear regulators into a single chip. The PWM controller provides the CPU core voltage controlled by a 5-bit DAC and the linear section regulates power for GTL bus, clock driver or other circuits on motherboards. The PWM controller provides an adjustable Intel-compatible 1.3V~3.5V output voltage. The synchronous N-MOSFET driver with 200 KHz switching frequency optimizes the efficiency, device size, and cost built-in over-voltage and current-limiting protection prevent the CPU from damage. Power-good signal is sent when the core voltage is within $\pm 10\%$ of the setting point.

The linear section is a low dropout regulator which drives low cost NPN transistors. The output level is user-adjustable and can be programmed by two external resistors and the internal 1.265V reference.

Ordering Information



Features

- Provides 3 Regulated Voltages
- N-MOSFET Driver for High Efficiency Switching Section
- Power-good, Over-voltage, and Current-limiting Protection for Switching Section
- Adjustable Output Voltage for Linear Section
- Linear Section Uses Low Cost NPN Transistor as Power Device
- TTL-compatible 5-bit DAC Core Output Voltage

Applications

- Power Supply for Pentium, Pentium Pro™, Pentium II™, PowerPC™, K6™, 6x86™, and Alpha™ Microprocessors
- High-power 5V to 3.xV DC-DC Regulators
- Low-voltage Distributed Power Supplies
- Programmable Power Supplies

Pin Configurations

Part Number	Pin Configurations			
RT9222CS	GND	1	24	GATE2
	GATE1	2	23	LDOV
	LDOS1	3	22	VID0
	LDOS2	4	21	VID1
	VCC	5	20	VID2
	OVP	6	19	VID3
	PGOOD	7	18	VID4
	CSN	8	17	VSEN
	CSP	9	16	SHDN
	PGNDH	10	15	BSTH
	DH	11	14	BSTL
	PGNDL	12	13	DL

Absolute Maximum Ratings

- VCC to GND (V_{IN}) ----- -0.3 to +5.5V
- PGND to GND ----- $\pm 0.3V$
- BSTH and BSTL to GND ----- -0.3 to +14V
- Ambient Temperature Range (T_A) ----- 0 to +70°C
- Junction Temperature Range (T_J) ----- 0 to +125°C
- Storage Temperature Range (T_{STG}) ----- -65 to +150°C
- Lead Temperature (Soldering) 10 seconds (T_L) ----- 300°C
- Thermal Impedance Junction to Ambient (θ_{JA}) ----- 80°C/W
- Thermal Impedance Junction to Case (θ_{JC}) ----- 25°C/W

Electrical Characteristics

VCC = 5V; GND = 0V; PGNDH = PGNDL = 0V; VSEN = VOUT; 0mV < ($V_{CSP} - V_{CSN}$) < 60mV; $T_A = 25^\circ C$

Parameter	Test Conditions	Min	Typ	Max	Units
Switching Section					
Output Voltage	$I_O = 2A$		(1)		
Supply Voltage	VCC	4.5	-	5.5	V
Supply Current		-	3	6	mA
Load Regulation	$I_O = 0.8A$ to 15A	-	1	-	%
Line Regulation	VCC = 4.75V to 5.25V	-	0.5	-	%
Power On Reset Trip Point	VCC Rising	-	4.2	-	V
Current Limit Voltage	$V_{CSP} - V_{CSN}$	65	75	85	mV
Oscillator Frequency		170	200	230	KHz
Oscillator Max Duty Cycle		90	95	-	%
DH Source	$V_{BSTH} - V_{DH} = 1V$	-	3.5	-	Ω
DH Sink	$V_{DH} - V_{PGNDH} = 1V$	-	3.5	-	Ω
DL Source	$V_{BSTL} - V_{DL} = 3V$	-	2	-	Ω
DL Sink	$V_{DL} - V_{PGNDL} = 1V$	-	2	-	Ω
OVP Threshold Voltage		-	120	-	%
OVP Source Current	$V_{OVP} = 3.0V$	10	-	-	mA
Power Good Threshold Voltage	VSEN Rising	92	-	108	%
Linear Sections					
Quiescent Current	LDOV = 12V	-	-	5	mA
Reference Voltage		1.240	1.265	1.290	V
Gain (A_{OL})	LDOS1/2 to GATE1/2	-	65	-	dB
Load Regulation	$I_O = 0$ to 5A	-	1	-	%
Line Regulation	LDOV = 11.4V to 12.6V	-	1	-	%

Note: (1) See output voltage table.

Pin Description

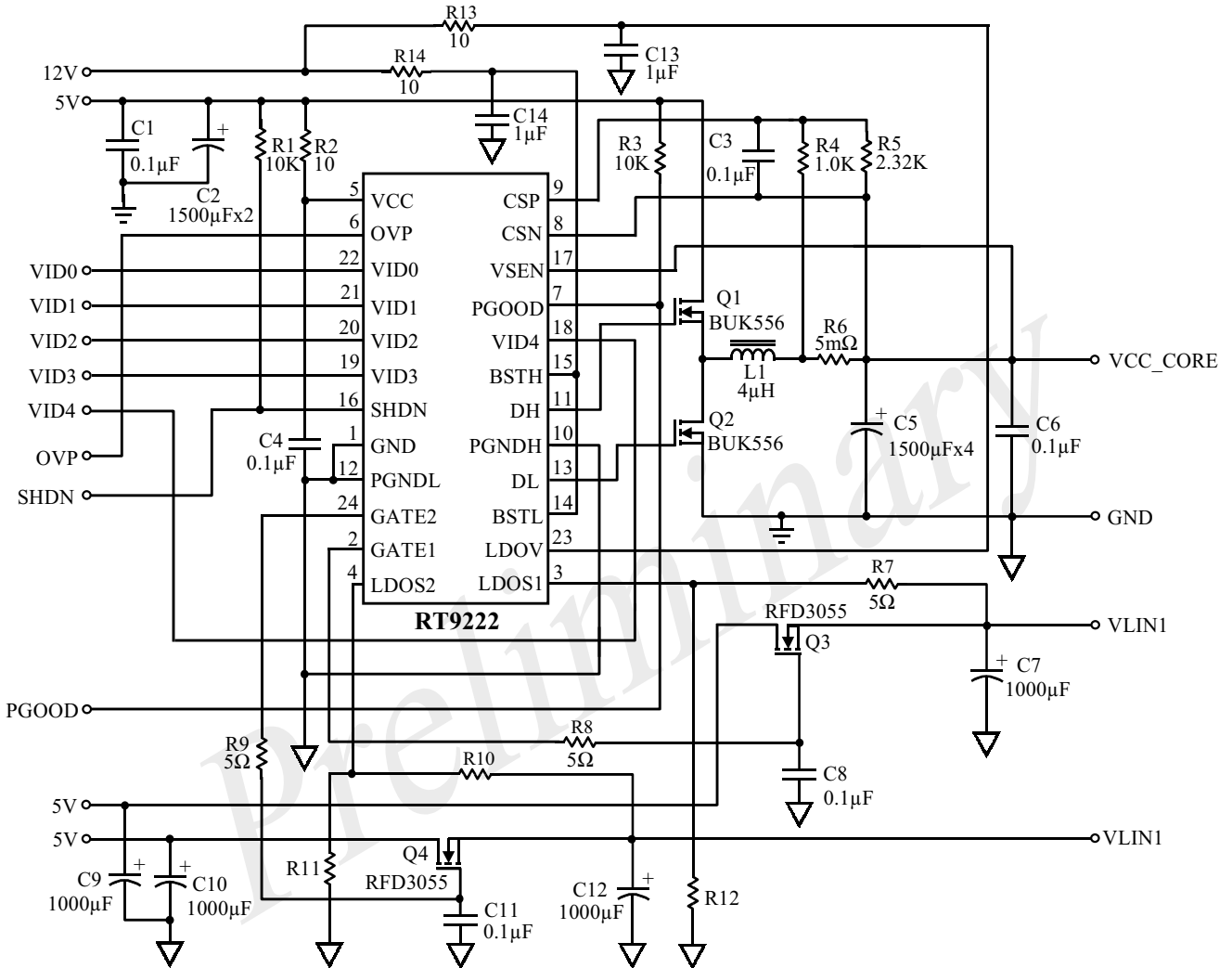
Pin No.	Pin Name	Pin Function
1	GND	Small signal analog and digital ground
2	GATE1	LDO1 gate drive output
3	LDOS1	LDO1 sense input
4	LDOS2	LDO2 sense input
5	VCC	Input voltage
6	OVP	High signal out if $V_o > \text{setpoint} + 20\%$
7	PGOOD ⁽¹⁾	Open collector logic output; High if V_o within 10% of setpoint
8	CSN	Current sense input (Negative)
9	CSP	Current sense input (Positive)
10	PGNDH	Power ground for high side switch
11	DH	High side driver output
12	PGNDL	Power ground for low side switch
13	DL	Low side driver output
14	BSTL	Supply for low side driver
15	BSTH	Supply for high side driver
16	SHDN ⁽¹⁾	Logic low shutdown the converter
17	VSEN	Top end of internal feedback chain
18	VID4 ⁽¹⁾	Programming input (MSB)
19	VID3 ⁽¹⁾	Programming input
20	VID2 ⁽¹⁾	Programming input
21	VID1 ⁽¹⁾	Programming input
22	VID0 ⁽¹⁾	Programming input (LSB)
23	LDOV	+12V for LDO section
24	GATE2	LDO2 gate drive output

Note: (1) All logic level inputs and outputs are TTL compatible.

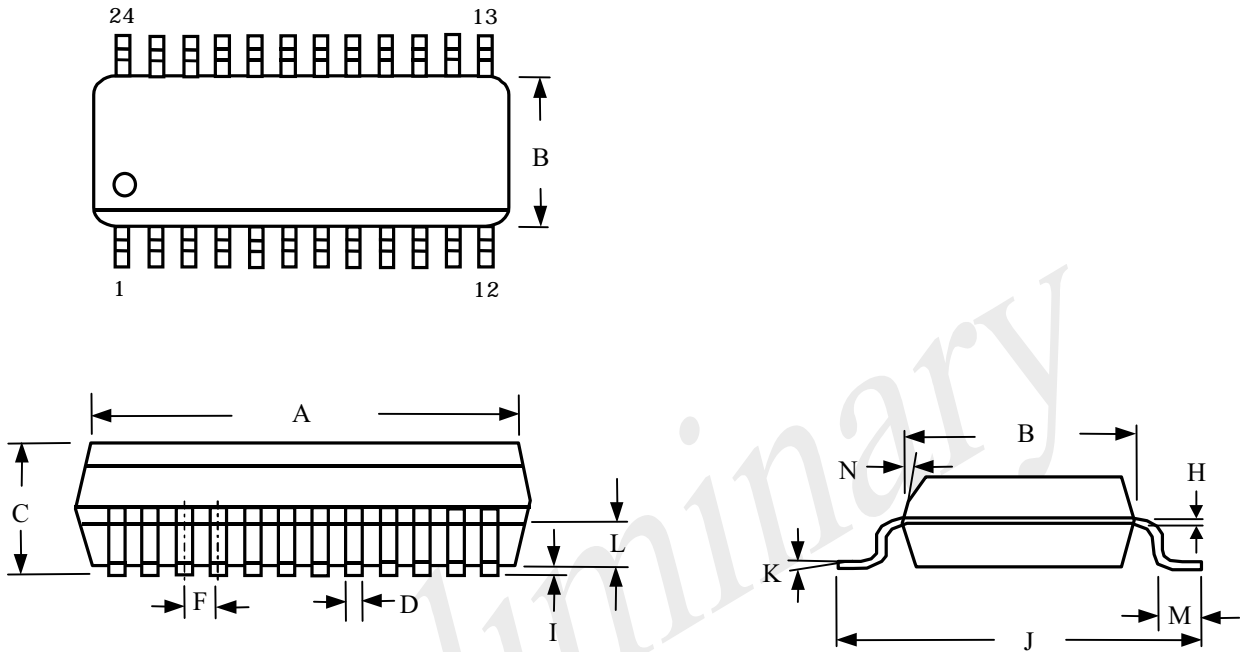
Output Voltage

Test	Conditions	VID 43210	Min	Typ	Max	Units
Output Voltage	$I_o = 2A$ in application circuit	01111	1.274	1.300	1.326	V
		01110	1.323	1.350	1.377	
		01101	1.372	1.400	1.428	
		01100	1.421	1.450	1.479	
		01011	1.478	1.500	1.523	
		01010	1.527	1.550	1.573	
		01001	1.576	1.600	1.624	
		01000	1.625	1.650	1.675	
		00111	1.675	1.700	1.726	
		00110	1.724	1.750	1.776	
		00101	1.773	1.800	1.827	
		00100	1.822	1.850	1.878	
		00011	1.872	1.900	1.929	
		00010	1.921	1.950	1.979	
		00001	1.970	2.000	2.030	
		00000	2.019	2.050	2.081	
		11111	1.940	2.000	2.060	
		11110	2.058	2.100	2.142	
		11101	2.156	2.200	2.244	
		11100	2.254	2.300	2.346	
		11011	2.352	2.400	2.448	
		11010	2.450	2.500	2.550	
		11001	2.548	2.600	2.652	
		11000	2.646	2.700	2.754	
		10111	2.744	2.800	2.856	
		10110	2.813	2.900	2.987	
		10101	2.910	3.000	3.090	
		10100	3.007	3.100	3.193	
		10011	3.104	3.200	3.296	
		10010	3.201	3.300	3.399	
10001	3.298	3.400	3.502			
10000	3.395	3.500	3.605			

Typical Application Circuit



Package Information



Symbols	Dimensions In Inches			Dimensions In Millimeter		
	Min	Norm	Max	Min	Norm	Max
A	0.606	0.608	0.610	15.392	15.443	15.494
B	0.298	0.300	0.302	7.569	7.620	7.671
C	0.098	0.100	0.102	2.489	2.540	2.591
D	--	0.016	--	--	0.406	--
F	--	0.050	--	--	1.270	--
H	--	0.010	--	--	0.254	--
I	0.006	--	--	0.152	--	--
J	0.406	0.410	0.414	10.312	10.414	10.516
K	--	5°	--	--	5°	--
L	0.039	0.041	0.043	0.991	1.041	1.092
M	0.030	0.032	0.034	0.762	0.813	0.864
N	--	7°	--	--	7°	--