Integrated Circuit Systems, Inc.

ICS9250-29

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

Solano type chipset.

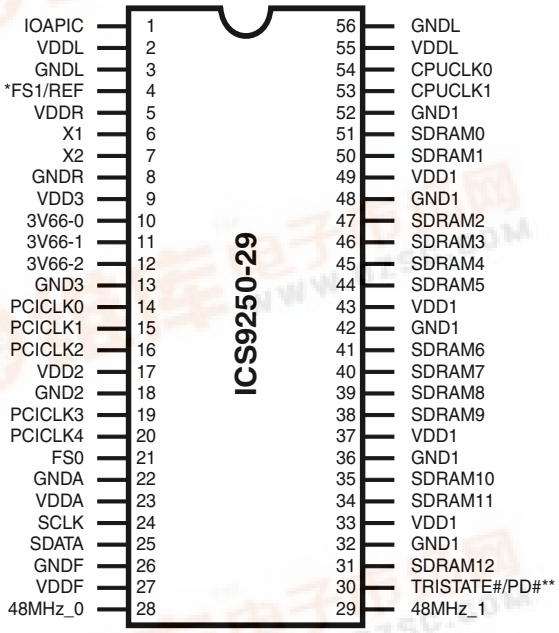
Output Features:

- 2 CPU (2.5V) (up to 133MHz achievable through I^2C)
- 13 SDRAM (3.3V) (up to 133MHz achievable through I^2C)
- 5 PCI (3.3 V) @33.3MHz
- 1 IOAPIC (2.5V) @ 33.3 MHz
- 3 Hublink clocks (3.3 V) @ 66.6 MHz
- 2 (3.3V) @ 48 MHz (Non spread spectrum)
- 1 REF (3.3V) @ 14.318 MHz

Features:

- Supports spread spectrum modulation, 0 to -0.5% down spread.
- I^2C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal
- Alternate frequency selections available through I^2C control.

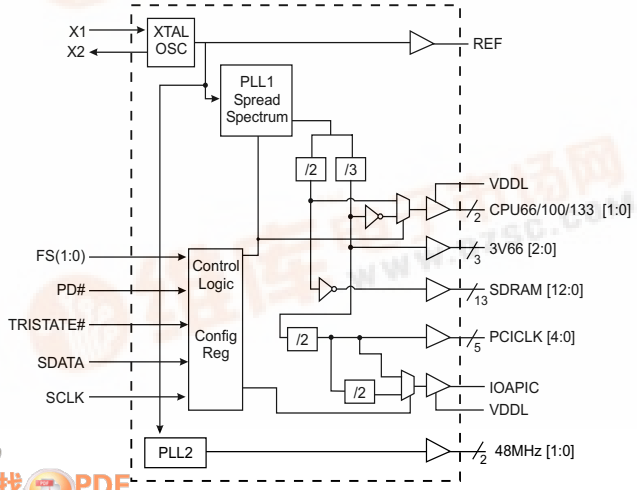
Pin Configuration



56-Pin 300mil SSOP

* This input has a 50KΩ pull-down to GND.
** This input has a 50KΩ pull-up to VDD

Block Diagram



Functionality

Tristate#	FS0	FS1	CPU MHz	SDRAM MHz
0	0	X	Tristate	Tristate
0	1	X	Test	Test
1	0	0	66MHz	100MHz
1	1	0	100MHz	100MHz
1	0	1	133MHz	133MHz
1	1	1	133MHz	100MHz

Power Groups

VDDA, GNDA = CPU, PLL (analog)
VDDF, GNDF = Fixed PLL, 48M (analog/digital)
VDDR, GNDR = REF, X1, X2 (analog/digital)
VDD3, GND3 = 3V66 (digital)
VDD2, GND2 = PCI (digital)
VDD1, GND1 = SDRAM (digital)
VDDL, GNDL = IOAPIC, CPU (digital)

ICS9250-29

General Description

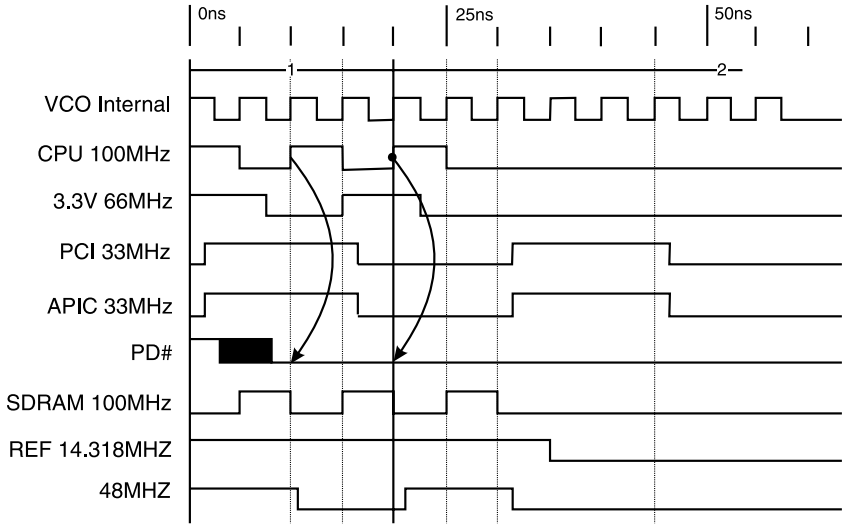
The **ICS9250-29** is a single chip clock solution for Solano type chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-29 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	IOAPIC	OUT	2.5V clock output running at 33.3MHz.
2, 55	VDDL	PWR	2.5V power supply for CPU & IOAPIC
3, 56	GNDL	PWR	Ground for 2.5V power supply for CPU & IOAPIC
4	FS1	IN	Function Select pin. Determines CPU frequency, all output functionality
	REF	OUT	3.3V, 14.318MHz reference clock output.
5, 9, 17, 23, 27, 33, 37, 43, 49	VDDx	PWR	3.3V power supply
6	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
7	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
8, 13, 18, 22, 26, 32, 36, 42, 48, 52	GNDx	PWR	Ground pins for 3.3V supply
12, 11, 10	3V66 (2:0)	OUT	3.3V Fixed 66MHz clock outputs for HUB
21	FS0	IN	Function Select pin. Determines CPU frequency, all output functionality.
20, 19, 16, 15, 14	PCICLK (4:0)	OUT	3.3V PCI clock outputs
30	TRISTATE#	IN	At power up the TRISTATE#/PD# pin defaults to the TRISTATE# input function to enable the TRISTATE# and TEST modes. (see Shared Pin Operation for full description).
	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
24	SCLK	IN	Clock input of I^2C input
25	SDATA	IN	Data input for I^2C serial input.
29, 28	48MHz (1:0)	OUT	3.3V Fixed 48MHz clock outputs.
31, 34, 35, 38, 39, 40, 41, 44, 45, 46, 47, 50, 51	SDRAM [12:0]	OUT	3.3V output running 100MHz and 133MHz. All SDRAM outputs can be turned off through I^2C
53, 54	CPUCLK (1:0)	OUT	2.5V Host bus clock output. 66MHz, 100MHz or 133MHz depending on FS pins.

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

Maximum Allowed Current

Solano Condition	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or GND	Max 3.3V supply consumption Max discrete cap loads, Vddq3 = 3.465V All static inputs = Vddq3 or GND
Powerdown Mode (PWRDWN# = 0)	2mA	2mA
Full Active 66MHz FS(1:0) = 00	35mA	440mA
Full Active 100MHz FS(1:0) = 01	50mA	430mA
Full Active 133MHz FS(1:0) = 11	60mA	440mA
Full Active 133MHz FS(1:0) = 10	60mA	500mA

Clock Enable Configuration

PD#	CPUCLK	SDRAM	IOAPIC	3V66	PCICLK	REF, 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

Note: This clock does not support Read Back. Doing a read back will lock up the PIIX-4 system.

Notes:

1. The ICS clock generator is a slave/receiver, I²C (SMB) component. It is only a "write" mode SMB device, no readback on this part. **Read-Back will lock up the PIIX-4 due to the Byte count of 00_H.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Truth Table

Tristate	FS0	FS1	CPU	SDRAM	3V66	PCI	48MHz	REF	IOAPIC
0	0	X	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
0	1	X	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6
1	0	0	66.6 MHz	100 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz
1	1	0	100 MHz	100 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz
1	0	1	133 MHz	133 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz
1	1	1	133 MHz	100 MHz	66.6 MHz	33.3 MHz	48 MHz	14.318 MHz	33.3 MHz

Byte 0: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	(Reserved ID)	0	(Active / Inactive)
Bit 6	-	(Reserved ID)	0	(Active / Inactive)
Bit 5	-	(Reserved ID)	0	(Active / Inactive)
Bit 4	-	(Reserved ID)	1	(Active / Inactive)
Bit 3	-	Spread Spectrum	0	(1=On / 0=Off)
Bit 2	29	48MHz_1	1	(Active / Inactive)
Bit 1	28	48MHz_0	1	(Active / Inactive)
Bit 0	-	(Reserved ID)	0	(Active / Inactive)

Note:
Reserved ID bits must be written with "0"

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	40	SDRAM7	1	(Active / Inactive)
Bit 6	41	SDRAM6	1	(Active / Inactive)
Bit 5	44	SDRAM5	1	(Active / Inactive)
Bit 4	45	SDRAM4	1	(Active / Inactive)
Bit 3	46	SDRAM3	1	(Active / Inactive)
Bit 2	47	SDRAM2	1	(Active / Inactive)
Bit 1	50	SDRAM1	1	(Active / Inactive)
Bit 0	51	SDRAM0	1	(Active / Inactive)

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	12	3V66_2 (AGP)	1	(Active / Inactive)
Bit 6	31	SDRAM12	1	(Active / Inactive)
Bit 5	34	SDRAM11	1	(Active / Inactive)
Bit 4	35	SDRAM10	1	(Active / Inactive)
Bit 3	38	SDRAM9	1	(Active / Inactive)
Bit 2	39	SDRAM8	1	(Active / Inactive)
Bit 1	15	PCICLK1	1	(Active / Inactive)
Bit 0	-	Undefined bit	0	(Active / Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default
3. Undefined bits can be written with either "1" or "0"

Byte 3: ICS Reserved Functionality and frequency select register (Default as noted in PWD)

Bit	Description								PWD
Bit 7	ICS Reserved bit (Note 2)								0
Bit 6	ICS Reserved bit (Note 2)								0
Bit 5	ICS Reserved bit (Note 2)								0
Bit 4	ICS Reserved bit (Note 2)								0
Bit 3	5% overclock mode (1 = 5% / 0= normal)								0
Bit 2	Undefined bit (note 3)								1
Bit 1	Tristate#/PWRDN# (1 = PWRDN# / 0 = Tristate#) see pin description								1
Bit 0	Bit 0	FS1	FS0	CPUCLK MHz	SDRAM MHz	3V66 MHz	PCICLK MHz	IOAPIC MHz	0 Note 1
	0	0	0	66.66	100.0	66.66	33.33	33.33	
	0	0	1	100.0	100.0	66.66	33.33	33.33	
	0	1	0	133.32	133.32	66.66	33.33	33.33	
	0	1	1	133.32	100.0	66.66	33.33	33.33	
	1	0	0	66.66	100.0	66.66	33.33	33.33	
	1	0	1	100.0	100.0	66.66	33.33	33.33	
	1	1	0	133.32	133.32	66.66	33.33	33.33	
	1	1	1	133.32	133.32	66.66	33.33	33.33	

Note 1: For system operation, the BSEL lines of the CPU will program FS0, FS1 for the appropriate CPU speed, always with SDRAM = 100MHz. After BIOS verifies the SDRAM is PC133 speed, then bit 0 can be written from the default 0 to 1 to change the SDRAM output frequency from 100MHz to 133MHz. This will only change if the CPU is at the 133MHz FSB speed as shown in this table. The CPU, 3V66, PCI and IOAPIC clocks will be glitch free during this transition, and only SDRAM will change.

Note 2: Must be written with "0"

Note 3: Undefined bits can be written with either "1" or "0"

Byte 4: Reserved Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	(Reserved)	0	(Active / Inactive)
Bit 6	-	(Reserved)	0	(Active / Inactive)
Bit 5	-	(Reserved)	0	(Active / Inactive)
Bit 4	-	(Reserved)	0	(Active / Inactive)
Bit 3	-	(Reserved)	0	(Active / Inactive)
Bit 2	20	PCICLK4	1	(Active / Inactive)
Bit 1	19	PCICLK3	1	(Active / Inactive)
Bit 0	16	PCICLK2	1	(Active / Inactive)

Byte 5: Reserved Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	(Reserved)	0	(Active / Inactive)
Bit 6	-	(Reserved)	0	(Active / Inactive)
Bit 5	-	(Reserved)	0	(Active / Inactive)
Bit 4	-	(Reserved)	0	(Active / Inactive)
Bit 3	-	(Reserved)	0	(Active / Inactive)
Bit 2	-	(Reserved)	0	(Active / Inactive)
Bit 1	-	(Reserved)	0	(Active / Inactive)
Bit 0	-	(Reserved)	0	(Active / Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table[1]

Group	CPU 66MHz SDRAM 100MHz		CPU 100MHz SDRAM 100MHz		CPU 133MHz SDRAM 100MHz		CPU 133MHz SDRAM 133MHz	
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM	-2.5ns	500ps	5.0ns	500ps	0.0ns	500ps	3.75ns	500ps
CPU to 3V66	7.5ns	500ps	5.0ns	500ps	0.0ns	500ps	0.0ns	500ps
SDRAM to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps	-3.75ns	500ps
3V66 to PCI	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5-3.5ns	500ps	1.5 -3.5ns	500ps
PCI to IOAPIC	0.0ns	1ns	0.0ns	1ns	0.0ns	1ns	0.0ns	1ns
USB & DOT	Asynch	N/A	Asynch	N/A	Asynch	N/A	Asynch	N/A

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND			600	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance[1]	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	13.5		22.5	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Delay[1]	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	ms
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	ms

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DD}=3,3V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.10	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.26	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	53.6	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5%;C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.46	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.47	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50.2	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	9		30	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH@\ min}$ = 1.0 V, $V_{OH@\ MAX}$ = 2.375 V	-27		-27	mA
Output Low Current	I_{OL4B}	$V_{OL@\ MIN}$ = 1.2 V, $V_{OL@\ MAX=}$ 0.3V	27		30	mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.09	1.6	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.22	1.6	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	45	50.2	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%, C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH\ @MIN}$= 2.0 V, $V_{OH@\ MAX}$=3.135 V	-54		-46	mA
Output Low Current	I_{OL3}	$V_{OL@\ MIN}$= 1.0 V, $V_{OL@\ MAX}$=0.4 V	49		53	mA
Rise Time	t_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.19	1.6	ns
Fall Time	t_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.43	1.6	ns
Duty Cycle	d_{t3}[1]	V_T = 1.5 V	45	54.9	55	%
Skew	t_{sk3}[1]	V_T = 1.5 V			250	ps
Jitter	$t_j$cyc-cyc[1]	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.43	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.63	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.9	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz_0

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, VDDL = 2.5 V +/-5%, C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = 1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = -1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH@MIN}$=1 V, $V_{OH@MAX}$= 3.135 V	-29		-23	mA
Output Low Current	I_{OL5}	$V_{OL@MIN}$=1.95 V, $V_{OL@MIN}$=0.4 V	29		27	mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.53	4	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.76	4	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45	53.6	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Fixed Clocks			500	ps
	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Ref Clocks			1000	ps

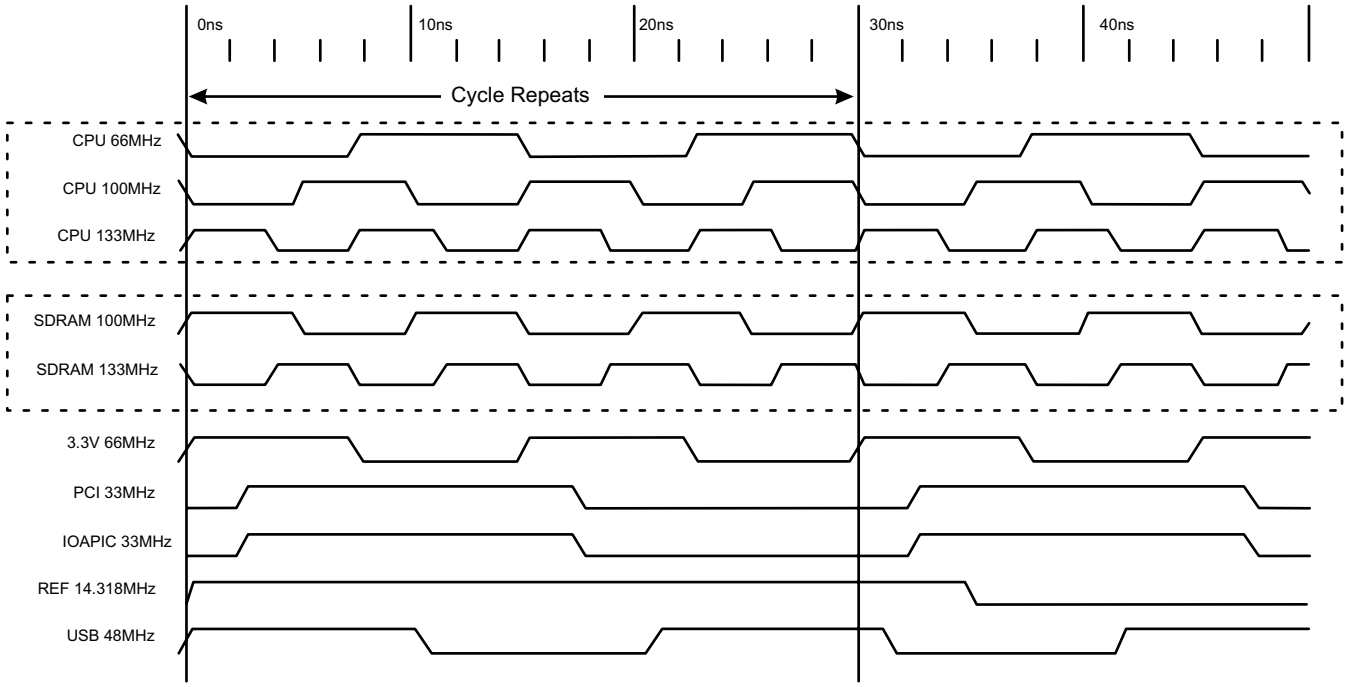
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz_1

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 15 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN3}[1]	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH@MIN}$ = 2.0 V, $V_{OH@MAX}$=3.135 V	-33		-33	mA
Output Low Current	I_{OL3}	$V_{OL@MIN}$ = 1.0 V, $V_{OL@MAX}$=0.4 V	30		38	mA
Rise Time	t_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.81	2.0	ns
Fall Time	t_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	0.95	2.0	ns
Duty Cycle	d_{t3}[1]	V_T = 1.5 V	45	53.1	55	%
Jitter	$t_j$cyc-cyc[1]	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.



Group Offset Waveforms

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9250-29 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

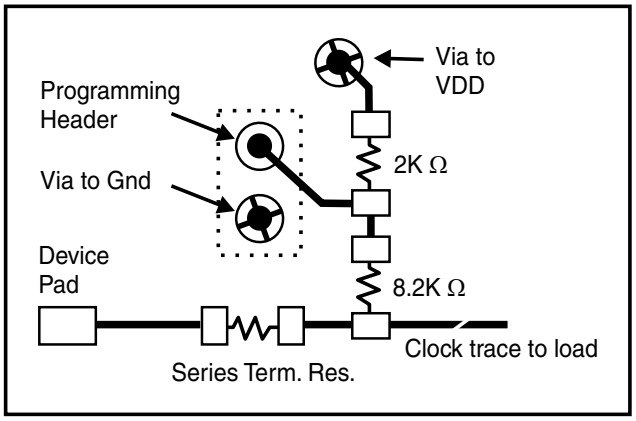


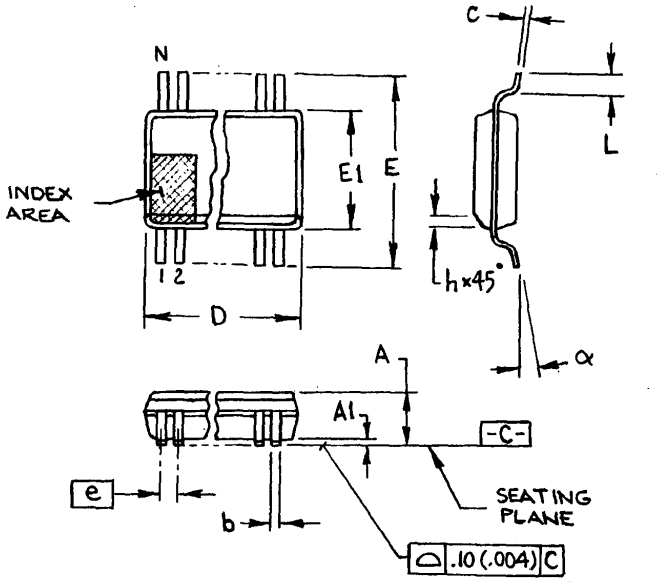
Fig. 1

TRISTATE#/PD# pin description:

The TRISTATE#/PD# pin provides the capability of invoking Tristate mode during board level testing.

At power up the TRISTATE#/PD# pin defaults to the TRISTATE# input function to enable the TRESTATE# and TEST modes.

Approximately 1.5ms to 3ms after power on, the TRISTATE#/PD# changes to the PD# input function and the TRISTATE# functionality is disabled (if TRISTATE# is not active).



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.288	18.542	.720	.730

JEDEC MO-118 6/1/00
DOC# 10-0034 REV B

Ordering Information

ICS9250yF-29-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device