

Features

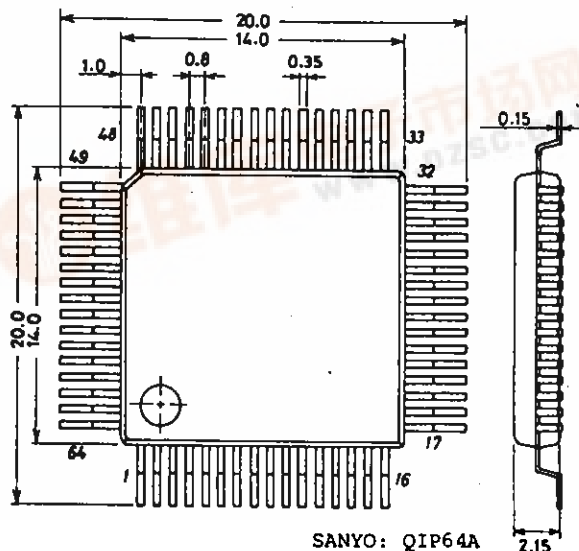
- High-speed, high-voltage silicon gate CMOS device
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock (CLOCK).
- 32-bit latch data is changed on the negative transition of the LATCH pad and is held on the positive transition.
- The STROBE pad, BEO pad can be used to exercise on/off control of the output driver.
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads)
- Maximum ratings of driver output : $V_O = 28V$, $I_{OL} = 30mA$
- Logic unit operating voltage : $V_{DD} = 4.5$ to $5.5V$

Absolute Maximum Ratings at $T_a = 25^\circ C$

			unit
Maximum Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_I	-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{O(1)}$	S_{OUT} output	-0.3 to $V_{DD} + 0.3$ V
	$V_{O(2)}$	D1 to D32 output, output Tr off	28 V
Output Current	I_O	D1 to D32 output, per output	30 mA
Allowable Power Dissipation	$P_d \max$	$T_a = 70^\circ C$	450 mW
Operating Temperature	T_{opr}	-10 to +70	$^\circ C$
Storage Temperature	T_{stg}	-35 to +125	$^\circ C$

Package Dimensions 3057

(unit: mm)



SANYO: QIP64A

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Allowable Operating Conditions at Ta = -10 to +70°C

		Pin Name	min	typ	max	unit
Supply Voltage	V _{DD}	V _{DD}	4.5		5.5	V
'H'-Level Input Voltage	V _{IH}	S _{IN} , C _{LOCK} , L _{ATCH} , B _{EO} , S _{TROBE}	0.8V _{DD}		V _{DD}	V
'L'-Level Input Voltage	V _{IL}	S _{IN} , C _{LOCK} , L _{ATCH} , B _{EO} , S _{TROBE}	V _{SS(L)}	0.2V _{DD}		V
Clock Frequency	f _{CLK}	C _{LOCK} Duty: 50%			5.0	MHz
Clock Pulse Width	t _{wφ}	C _{LOCK}	75			ns
Clock Rise/Fall Time	t _r , t _f	C _{LOCK}			200	ns
Data Setup Time	t _{DS}	S _{IN} , C _{LOCK}	100			ns
Data Hold Time	t _{DH}	S _{IN} , C _{LOCK}	50			ns
Latch Pulse Width	t _{WL}	L _{ATCH}	100			ns

Electrical Characteristics at Ta = 25°C

		Pin Name	min	typ	max	unit
'H'-Level Input Current	I _{IH(1)}	S _{IN} , C _{LOCK} , L _{ATCH}			10	μA
		B _{EO}	12		72	μA
'L'-Level Input Current	I _{IL(1)}	S _{IN} , C _{LOCK} , L _{ATCH}	-10			μA
		I _{IL(2)}	-72		-12	μA
'H'-Level Output Voltage	V _{OH}	S _{OUT} V _{DD} =5V, I _{OH} =-0.5mA	V _{DD} -0.5			V
'L'-Level Output Voltage	V _{OL(1)}	S _{OUT} V _{DD} =5V, I _{OL} =0.5mA			0.5	V
		V _{OL(2)} D1 to D32 V _{DD} =5V, I _{OL} =30mA			0.5	V
Output OFF-State Leakage Current	I _{OFF}	D1 to D32 V _O =24V			20	μA
Input Capacitance	C _{IN}	C _{LOCK}		5.0		pF
Operating Current Dissipation	I _{DD}	V _{DD} V _{DD} =5V, f _{CLK} =5MHz, all outputs: no load			5	mA

Switching Characteristics at Ta = 25°C

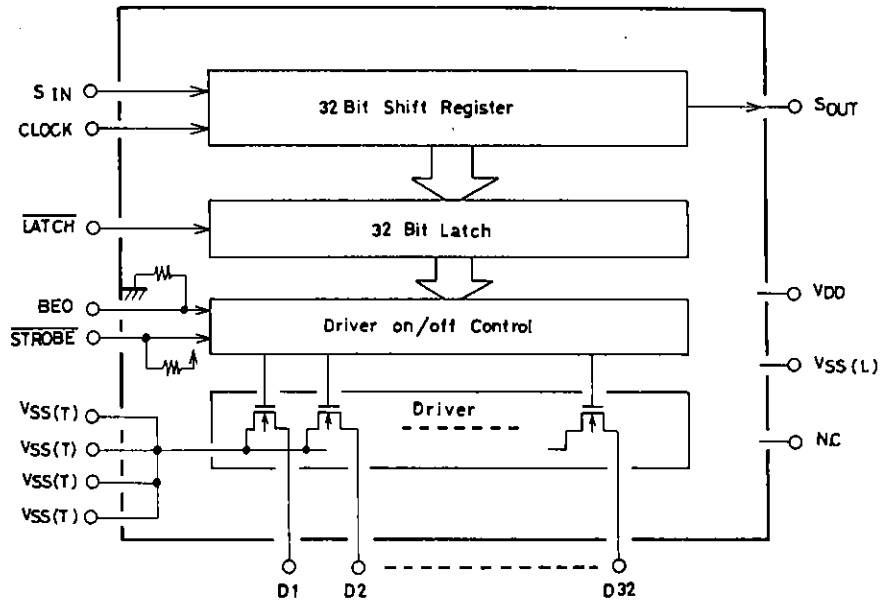
		Pin Name	min	typ	max	unit
Clock Latch Delay Width	t _{CL}	C _{LOCK} , L _{ATCH} V _{DD} =5V	100			ns
Latch Clock Delay Width	t _{LC}	C _{LOCK} , L _{ATCH} V _{DD} =5V	0			ns
'H'-Level Output Propagation Delay Time	t _{PLH(1)}	L _{ATCH} , D1 to D32 V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			400	ns
		B _{EO} , S _{TROBE} V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			300	ns
		C _{LOCK} , S _{OUT} V _{DD} =5V, S _{OUT} : C _L =15pF			200	ns
'L'-Level Output Propagation Delay Time	t _{PHL(1)}	L _{ATCH} , D1 to D32 V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			200	ns
		B _{EO} , S _{TROBE} D1 to D32 V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			100	ns
		C _{LOCK} , S _{OUT} V _{DD} =5V, S _{OUT} : C _L =15pF			200	ns

Driver ON/OFF Truth Table

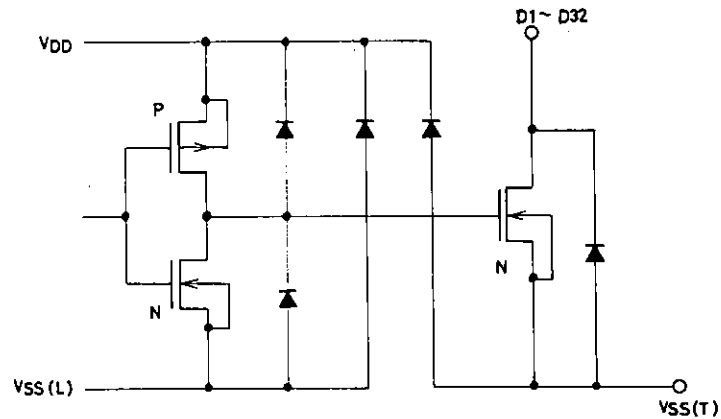
Latch Data (Q)	BEO	STROBE	Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Driver on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

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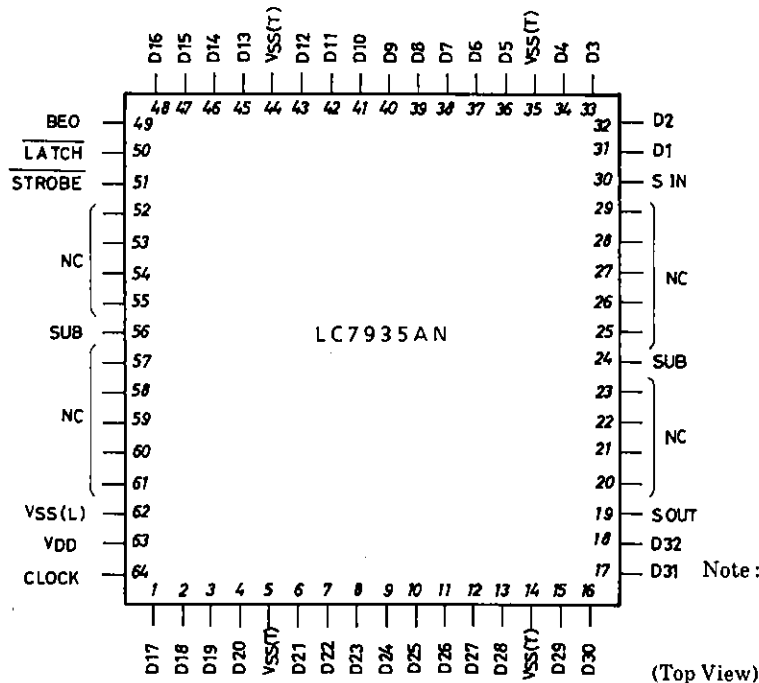
Equivalent Circuit Block Diagram



Output Driver Section Equivalent Circuit



Pin Assignment

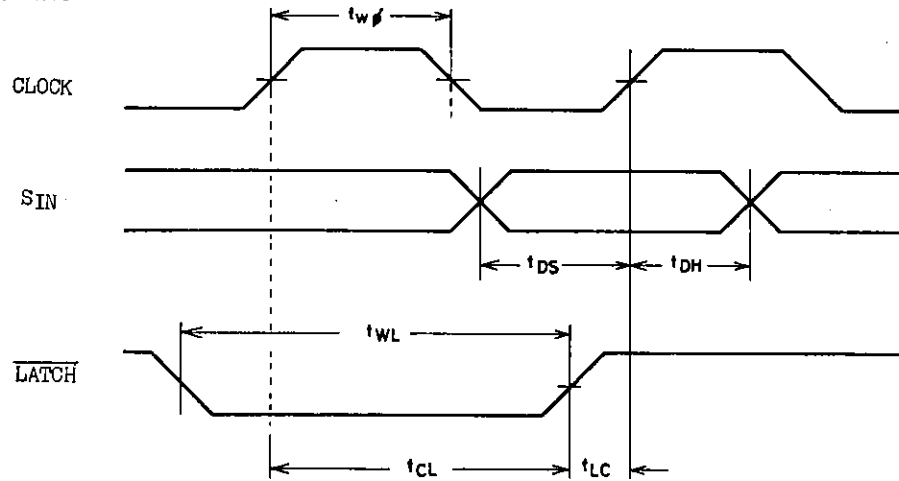


Note: SUB pin and NC pin must be kept open. [SUB pin is connected to the substrate (V_{DD}).]

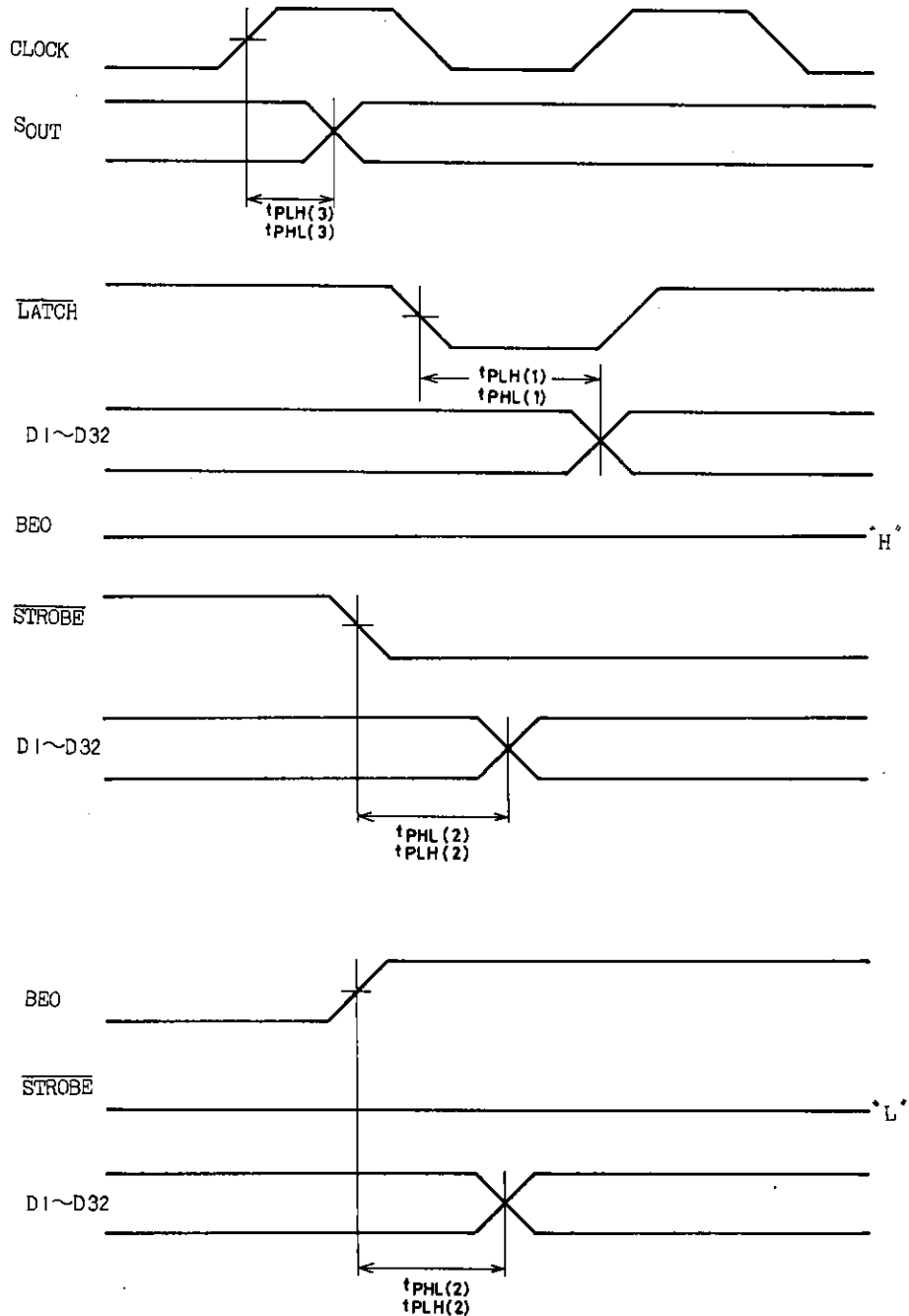
(Top View)

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Input Data Timing Chart



Output Data Timing Chart



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