

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4938B

**Dual precision monostable
multivibrator**

Preliminary specification
File under Integrated Circuits, IC04

January 1995

Dual precision monostable multivibrator

HEF4938B

FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- I_{CC} category: MSI

DESCRIPTION

The HEF4938B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW trigger/retrigger input (\bar{I}_0), an active HIGH trigger/retrigger input (I_1), an overriding active LOW direct reset input (\bar{C}_D), an output (O) and its complement (\bar{O}), and two pins (C_{TC} and $R_{C_{TC}}$) for connecting the external timing components C_t and R_t . Typical pulse width variation over temperature range is $\pm 0.2\%$.

The HEF4938B may be triggered by either the positive or the negative edges of the input pulse and will produce an accurate output pulse with a pulse width range of 10 μ s to infinity. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t . The output pulse width (T) is equal to $R_t \times C_t$. The linear design techniques in LOC MOS guarantee precise control of the output pulse width. A LOW level at \bar{C}_D terminates the output pulse immediately. Schmitt-trigger action in the inputs makes the circuit highly tolerant for slower rise and fall times.

FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{I}_0	I_1	\bar{C}_D	O	\bar{O}
\uparrow	L	H	\nearrow	\searrow
H	\uparrow	H	\nearrow	\searrow
X	X	L	L	H

Notes

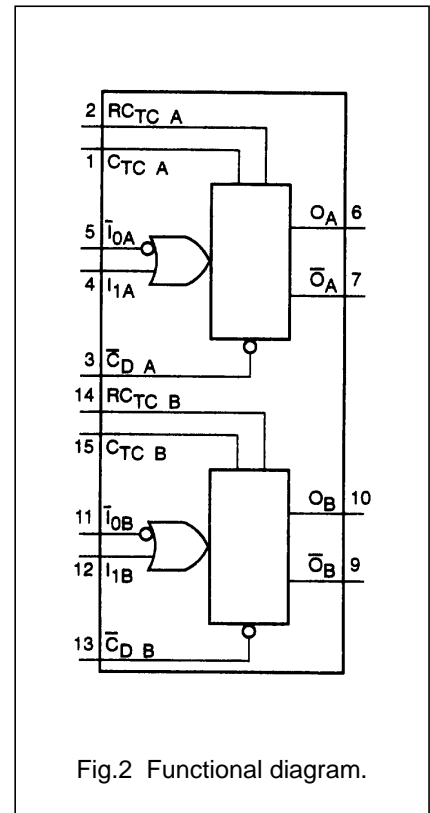
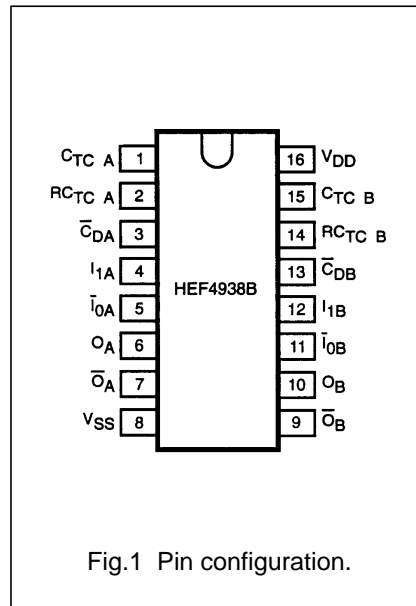
1. H = HIGH voltage level
2. L = LOW voltage level

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
HEF4938B	16	DIL	plastic	SOT38Z

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$C_{TC A}, C_{TC B}$	external capacitor connections
2, 14	$R_{C_{TC A}}, R_{C_{TC B}}$	external capacitor/resistor connections
3, 13	$\bar{C}_{DA}, \bar{C}_{DB}$	direct reset input (active LOW)
4, 12	I_{1A}, I_{1B}	input (LOW-to-HIGH triggered)
5, 11	$\bar{I}_{0A}, \bar{I}_{0B}$	input (HIGH-to-LOW triggered)
6, 10	O_A, O_B	output
7, 9	\bar{O}_A, \bar{O}_B	complementary output (active LOW)
8	V_{SS}	ground (0 V)
16	V_{DD}	positive supply voltage



3. X = state is immaterial
4. \uparrow = positive-going transition
5. \downarrow = negative-going transition
6. \nearrow = positive output pulse
7. \searrow = negative output pulse

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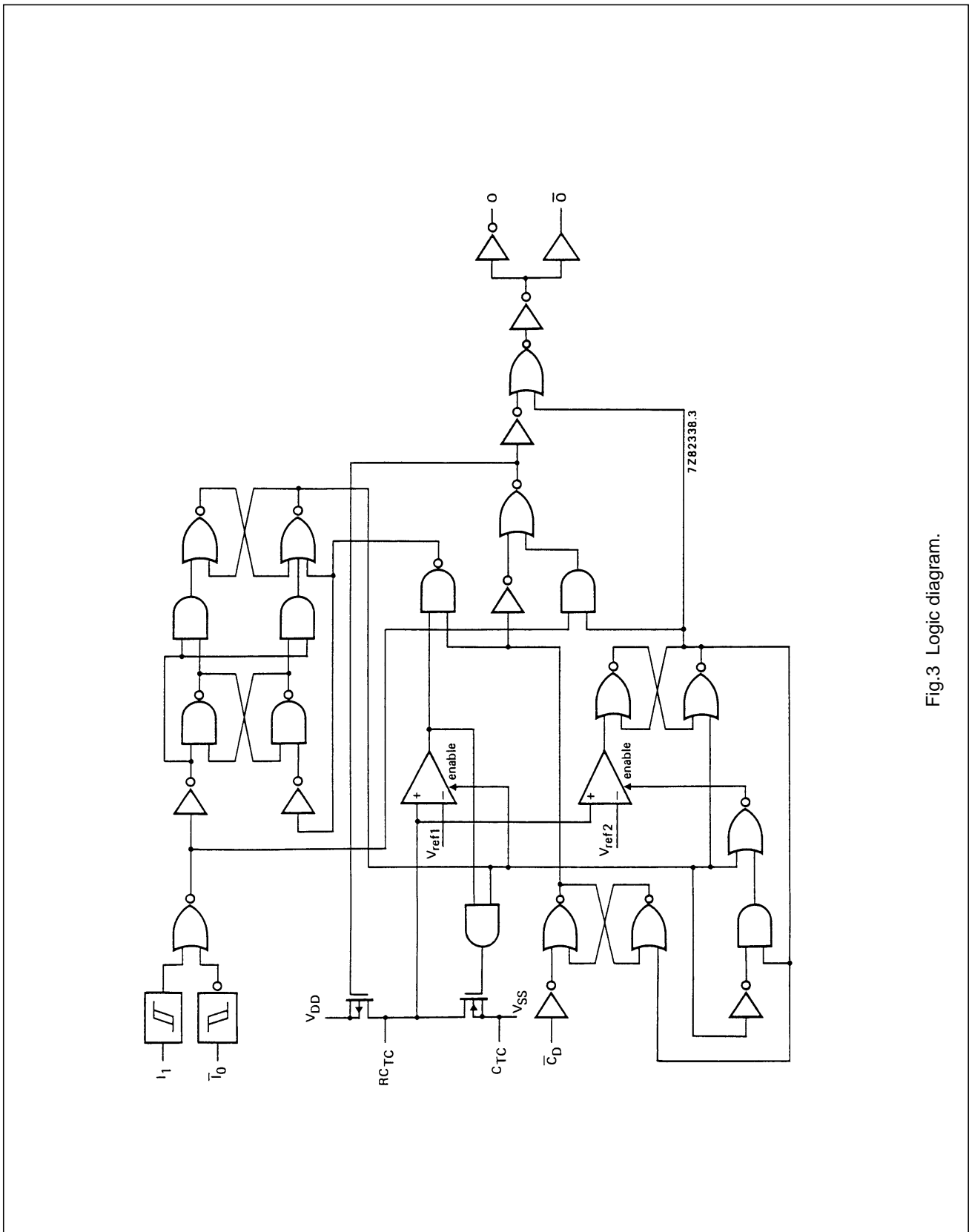








Fig.3 Logic diagram.





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FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{I}_0	I_1	\bar{C}_D	O	\bar{O}
	L	H		
H		H		
X	X	L	L	H

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4.  = positive-going transition
5.  = negative-going transition
6.  = positive output pulse
7.  = negative output pulse

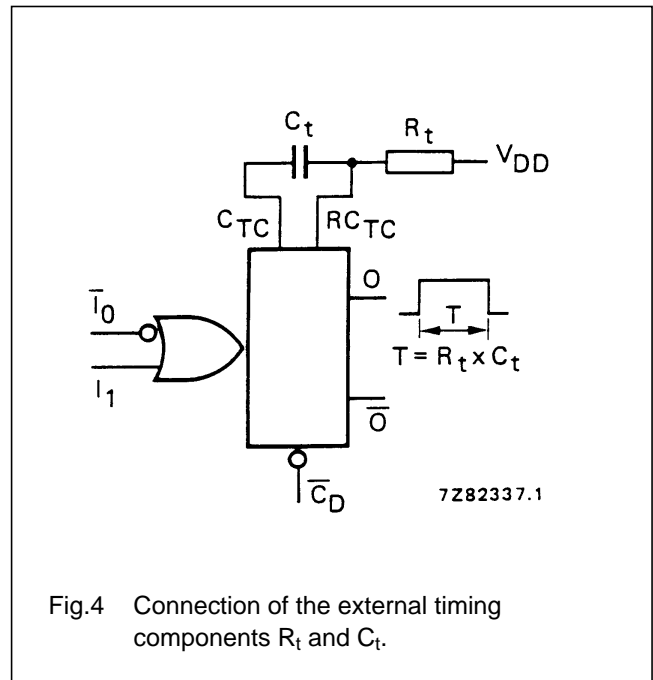


Fig.4 Connection of the external timing components R_t and C_t .

DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$

	V_{DD} V	SYMBOL	$T_{amb} (\text{°C})$					
			-40		+ 25		+ 85	
			TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
Supply current	5	I_D			55			μA
active state	10				150			μA
(see note)	15				220			μA
Input leakage current (pins 2 and 14)	15	$\pm I_{IN}$			300		1000	nA

Note

1. Only one monostable is switching: current present during output pulse (output O is HIGH).

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AC CHARACTERISTICS $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$.

PARAMETER	V_{DD} (V)	SYMBOL	MIN.	TYP.	MAX.	UNIT	TYPICAL EXTRAPOLATION FORMULA
Propagation delay \bar{I}_0, I_1 to O	5	t_{PHL}	–	200	460	ns	$173\text{ ns} + (0.55\text{ ns/pF}) C_L$
HIGH to LOW	10		–	90	180		$79\text{ ns} + (0.23\text{ ns/pF}) C_L$
	15		–	60	120		$52\text{ ns} + (0.16\text{ ns/pF}) C_L$
Propagation delay \bar{I}_0, I_1 to \bar{O}	5	t_{PLH}	–	220	440	ns	$193\text{ ns} + (0.55\text{ ns/pF}) C_L$
LOW to HIGH	10		–	85	190		$74\text{ ns} + (0.23\text{ ns/pF}) C_L$
	15		–	60	120		$52\text{ ns} + (0.16\text{ ns/pF}) C_L$
Propagation delay \bar{C}_D to O	5	t_{PHL}	–	125	250	ns	$98\text{ ns} + (0.55\text{ ns/pF}) C_L$
HIGH to LOW	10		–	55	110		$44\text{ ns} + (0.23\text{ ns/pF}) C_L$
	15		–	40	80		$32\text{ ns} + (0.16\text{ ns/pF}) C_L$
Propagation delay \bar{C}_D to O	5	t_{PLH}	–	125	250	ns	$98\text{ ns} + (0.55\text{ ns/pF}) C_L$
LOW to HIGH	10		–	55	110		$44\text{ ns} + (0.23\text{ ns/pF}) C_L$
	15		–	40	80		$32\text{ ns} + (0.16\text{ ns/pF}) C_L$
Recovery times \bar{C}_D to \bar{I}_0, I_1	5	t_{RCD}	–	20	40	ns	
	10		–	10	20		
	15		–	5	10		
Retrigger times O, \bar{O} to \bar{I}_0, I_1	5	t_{RO}	0	–	–	ns	
LOW to OFF	10		0	–	–		
	15		0	–	–		
Minimum output pulse width LOW \bar{I}_0	5	t_{WIOL}	90	45	–	ns	
	10		30	15	–		
	15		24	12	–		
Minimum output pulse width LOW I_1	5	t_{WI1H}	50	25	–	ns	
	10		24	12	–		
	15		20	10	–		
Output pulse width O, \bar{O}	5	t_{WO}	9.3	10.0	10.6	ms	$R_t = 100\text{ k}\Omega$; $C_t = 100\text{ nF}$
	10		9.2	9.9	10.5		
	15		9.1	9.8	10.4		

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AC CHARACTERISTICS $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Change in output O pulse width over temperature (T_{amb})	5	Δt_{WO}		$\pm 0,2$	%	$R_t = 100$ k Ω $C_t = 2$ nF to 10 μ F
	10			$\pm 0,2$	%	
	15			$\pm 0,2$	%	
Change in output O pulse width over V_{DD} range 5 to 15 V		Δt_{WO}		$\pm 1,5$	%	
Pulse width variation between circuits in same package	5	Δt_{WO}		± 1	%	
	10			± 1	%	
	15			± 1	%	
External timing resistor		R_t	5	–	(1) k Ω	
External timing capacitor		C_t	2000	–	no limits pF	
Input capacitance (pin 2 or 14)		C_{IN}		15	pF	

Note

1. The maximum permissible resistance R_t , which holds the specified accuracy of t_{WO} , depends on the leakage current of the capacitor C_t and the leakage of the HEF4538B.

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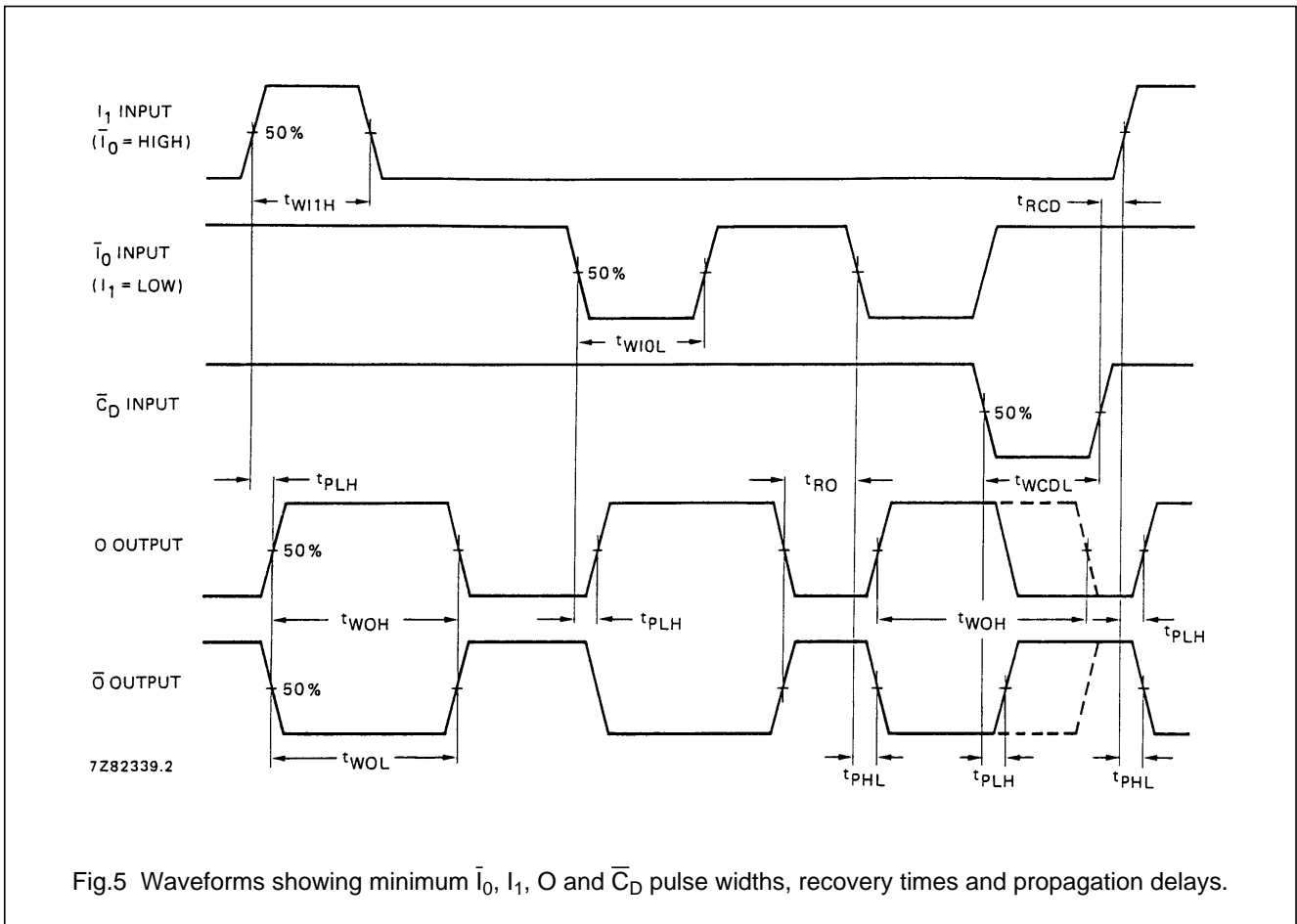


Fig.5 Waveforms showing minimum \bar{I}_0 , I_1 , O and \bar{C}_D pulse widths, recovery times and propagation delays.

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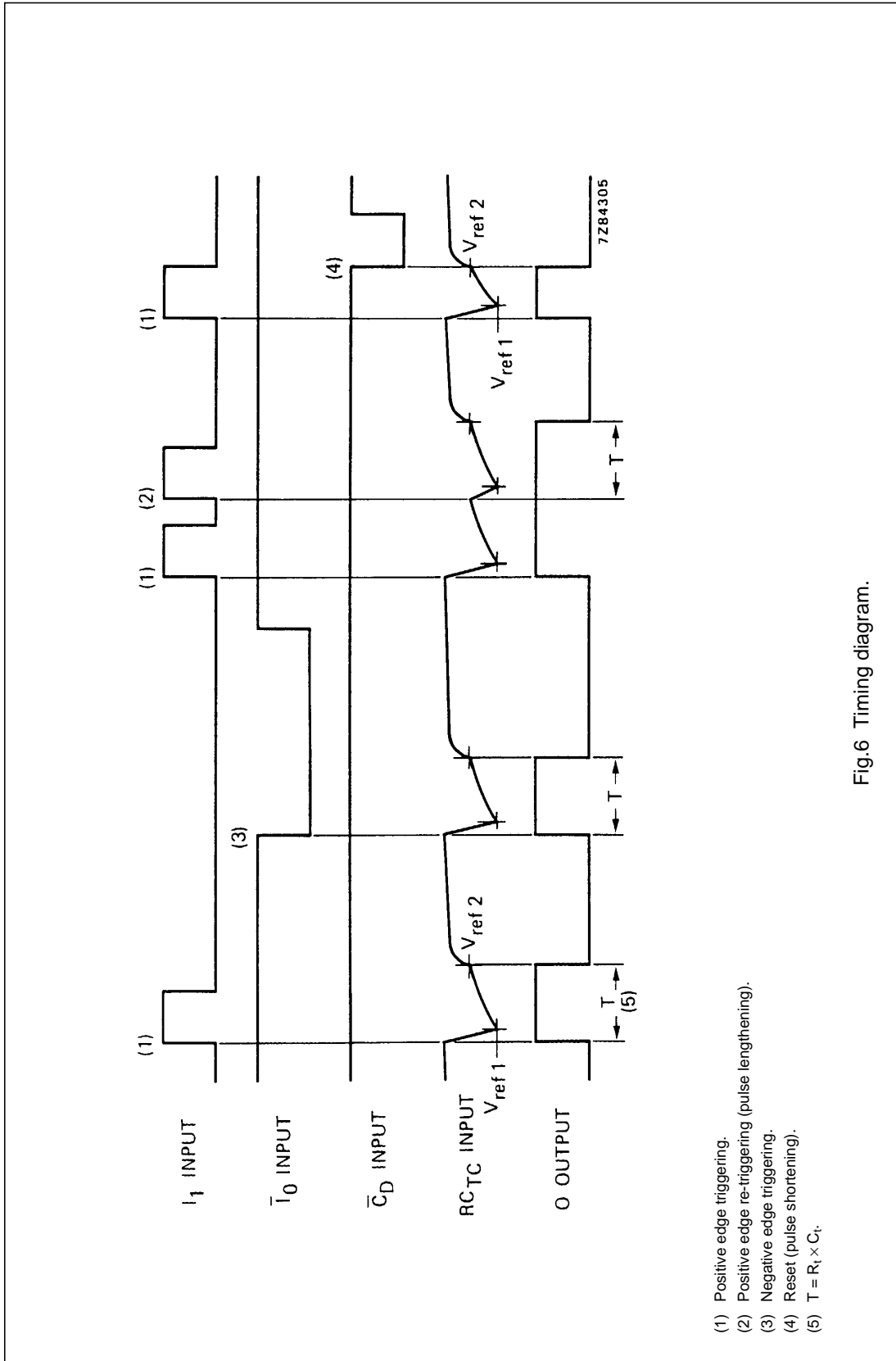


Fig.6 Timing diagram.

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