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CMOS LSI

SANYO No. 4347

LC7943D

Dot Matrix LCD Driver

Overview

The LC7943D is a large-scale dot matrix LCD common driver LSI. The LC7943D contains an 68-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC7943D can be used in conjunction with segment driver LC79400D, LC79401D (QIP100D) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (68 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support further increases in bit number
- Supports externally supplied bias voltage
- Operating power supply voltage/operating temperature include

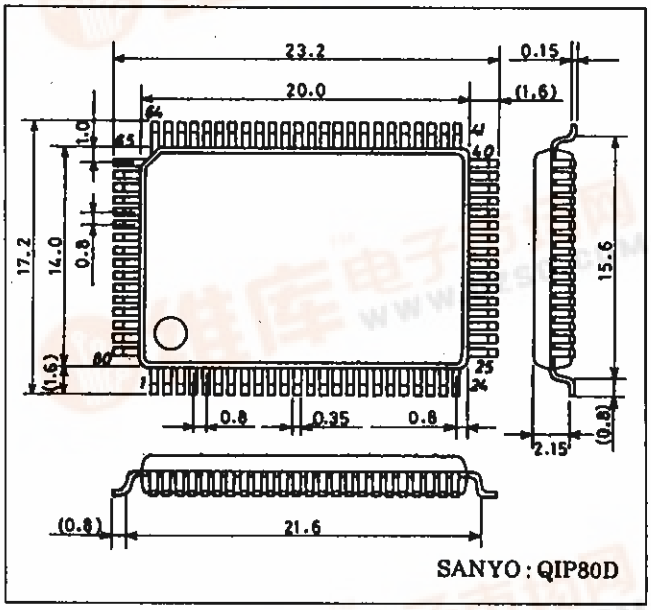
  V_{DD} (logic section) : 5 V ±10 % / –20 to +75 °C

  V_{DD}-V_{EE} (LCD section) : 12 V to 32 V / –20 to +75°C
- CMOS process

Package Dimensions

unit : mm

3177-QIP80D



SANYO : QIP80D

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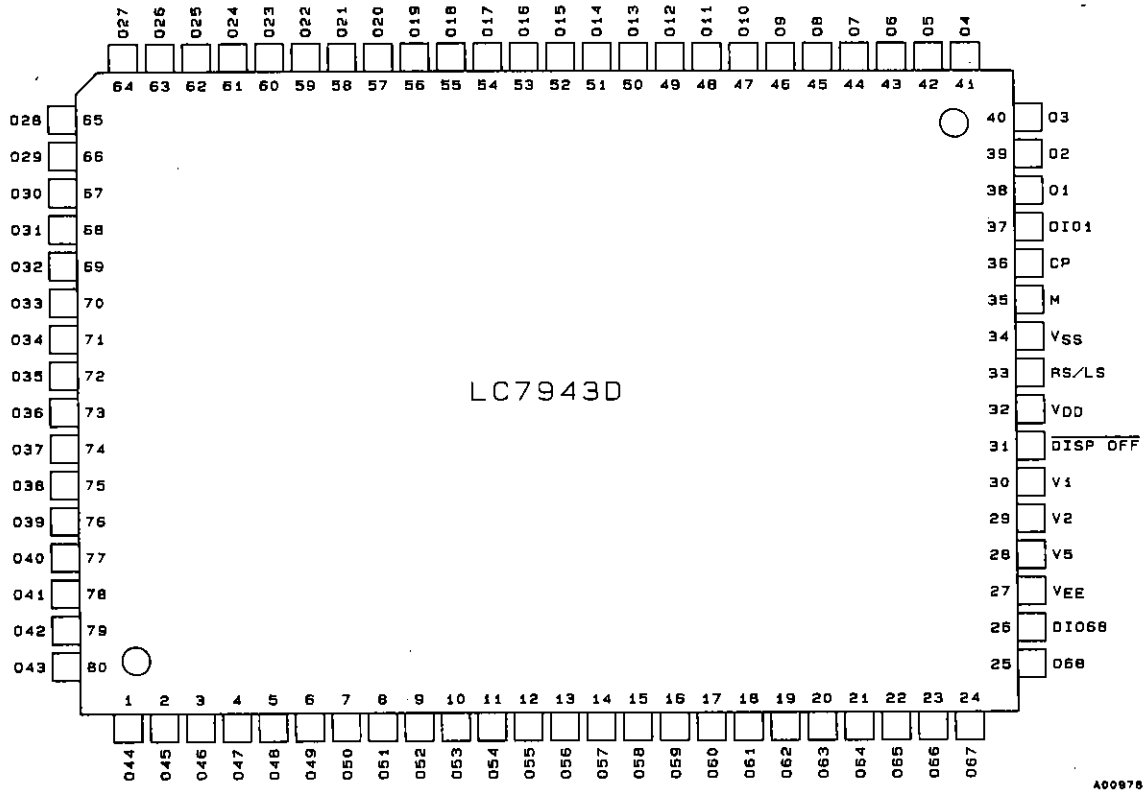
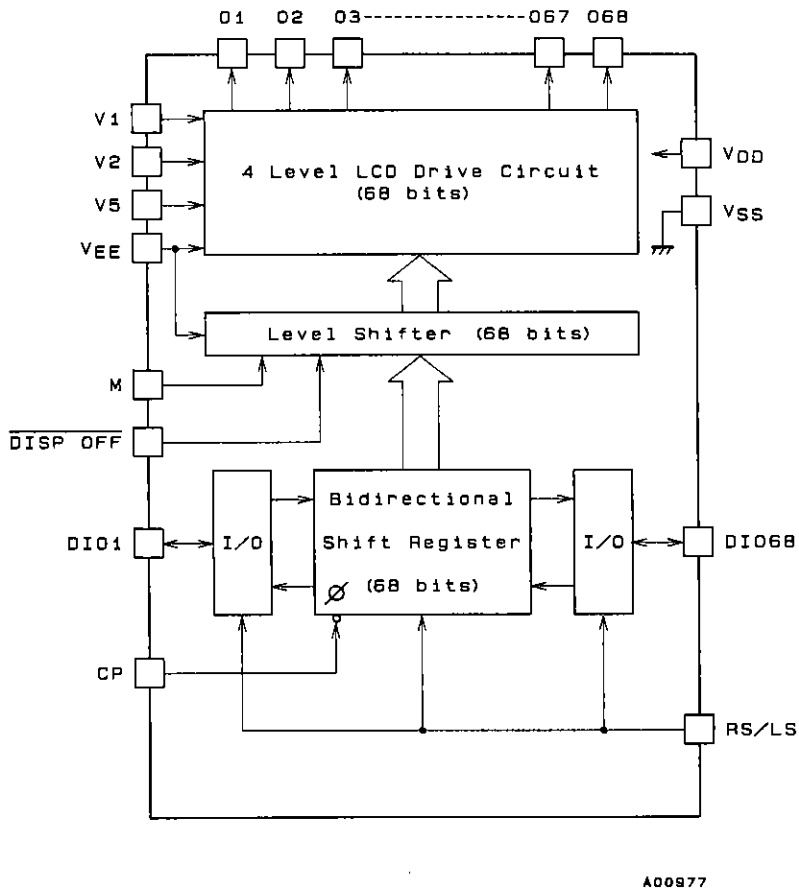
Pin Assignment



Equivalent Circuit Block Diagram



Pin Descriptions

Pin No	Pin name	Input/Output	Functions
32 34 27	V_{DD} V_{SS} V_{EE}	Power supply	V_{DD} and V_{SS}: Power supply for logic section V_{DD} and V_{EE}: Power supply for LCD drive circuit
30 29 28	V1 V2 V3	Power supply	Power supply for LCD drive level V1 and V_{EE} : Select level V2 and V5 : Non-select level
36	CP	Input	Bidirectional shift register shift clock (triggering on the trailing edge)
37 26 33	DIO1 DIO68 RS/LS	Input/Output Input	<table><tr><th>RS/LS</th><th>DIO1</th><th>DIO68</th><th>Shift Direction</th></tr><tr><td>L</td><td>IN</td><td>OUT</td><td>O1 → O68</td></tr><tr><td>H</td><td>OUT</td><td>IN</td><td>O68 → O1</td></tr></table>
35	M	Input	LCD drive output alternating current (AC) signal
31	$\overline{\text{DISP OFF}}$	Input	O1 to O68 output controlling input pins
38 ⋮ 80 1 ⋮ 25	O1 ⋮ O43 O44 ⋮ O68	Output	LCD drive output As shown in the following table, output levels switch in response to the particular combination of scan data, M and $\overline{\text{DISP OFF}}$ signals. <table><tr><th>M</th><th>Data</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr><tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr><tr><td>L</td><td>H</td><td>H</td><td>V_{EE}</td></tr><tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr><tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr><tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr></table>* Don't care (May be set to either "H" or "L")

Specifications

Absolute Maximum Ratings at Ta = 25±2°C, V_{SS} = 0V

			unit
Maximum supply voltage (LOGIC)	V_{DD} max	−0.3 to +7.0	V
Maximum supply voltage (LCD)	V_{DD}-V_{EE} max *1	0 to 35	V
Maximum input voltage	V_I max	−0.3 to V_{DD} +0.3	V
Storage temperature range	Tstg	−40 to +125	°C

*1: The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD} - V2 \leq 7V$, $V5 - V_{EE} \leq 7V$.

Allowable Operating Ranges at Ta = −20 to +75°C, V_{SS} = 0V

			min	typ	max	unit
Supply voltage (LOGIC)	V_{DD}		4.5		5.5	V
Supply voltage (LCD)	V_{DD}-V_{EE}	*2, *3	12		32	V
Input "H" level voltage	V_{IH}	DIO1, DIO68, CP, M, RS/LS, $\overline{\text{DISP OFF}}$	0.8V_{DD}			V
Input "L" level voltage	V_{IL}	DIO1, DIO68, CP, M, RS/LS, $\overline{\text{DISP OFF}}$			0.2V_{DD}	V
CP (Shift Clock)	f_{CP}	CP			1	MHz
CP (Pulse width)	t_{WC}	CP	125			ns
Setup time	t_{SETUP}	DIO1 → CP, DIO68 → CP	100			ns
Hold time	t_{HOLD}	DIO1 → CP, DIO68 → CP	100			ns
CP Rise-Fall Time	t_R	CP			50	ns
	t_F	CP			50	ns

*2 The following relations between elements should be maintained: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD} - V2 \leq 7V$, $V5 - V_{EE} \leq 7V$.

*3 When the power supply is turned on, power to the LCD drive is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

Electrical Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±10%			min	typ	max	unit
Input "H" level current	I_{IH}	V_{IN} = V_{DD}, V_{DD} = 5.5V; DIO1, DIO68, CP, M, RS/LS, $\overline{\text{DISP OFF}}$			1	µA
Input "L" level current	I_{IL}	V_{IN} = V_{SS}, V_{DD} = 5.5V; DIO1, DIO68, CP, M, RS/LS, $\overline{\text{DISP OFF}}$	–1			µA
Output "H" level voltage	V_{OH}	I_{OH} = –0.4mA, V_{DD} = 4.5V; DIO1, DIO68	V_{DD}–0.4			V
Output "L" level voltage	V_{OL}	I_{OL} = 0.4mA, V_{DD} = 4.5V; DIO1, DIO68			0.4	V
Driver On Resistor	R_{ON} (1)	V_{DD}-V_{EE} = 30V, | V_{DE}-Vo | = 0.5V, V_{DD} = 4.5V *4; O1 to O68			1.0	kΩ
	R_{ON} (2)	V_{DD}-V_{EE} = 20V, | V_{DE}-Vo | = 0.5V, V_{DD} = 4.5V *4; O1 to O68			1.0	kΩ
Consumable current (1)	I_{SS}	V_{DD}-V_{EE} = 30V, CP = 14kHz, no-load, V_{DD} = 5.5V; V_{SS}			100	µA
Consumable current (2)	I_{EE}	V_{DD}-V_{EE} = 30V, CP = 14kHz, no-load, V_{DD} = 5.5V; V_{EE}			100	µA
Input Capacity	C_I	f = 1MHz; CP		5		pF

*4 V_{DE} = V1 or V2 or V5 or V_{EE}, V1 = V_{DD}, V2 = 16/17 (V_{DD}-V_{EE}), V5 = 1/17 (V_{DD}-V_{EE})

Switching Characteristics at Ta = 25±2°C, V_{SS} = 0V, V_{DD} = 5V±10%			min	typ	max	unit
Output Delay Time	t_{PLH}	CL = 15PF; CP → DIO1, CP → DIO68			250	ns
	t_{PHL}	CL = 15PF; CP → DIO1, CP → DIO68			250	ns

Switching Characteristics