Dual Digitally Controlled Potentiometer (XDCP™) with Operational Amplifier

FEATURES

- Two CMOS voltage operational amplifiers
- Two digitally controlled potentiometers
- Can be combined or used separately
- Amplifiers
  - —Low voltage operation
  - —V+/V- = ±2.7V to ±5.5V
  - —Rail-to-rail CMOS performance
  - —1MHz gain bandwidth product
- Digitally controlled potentiometer
  - —Dual 64 tap potentiometers
  - —R_{total} = 10kΩ
  - —SPI serial interface
  - —V_{CC} = 2.7V to 5.5V

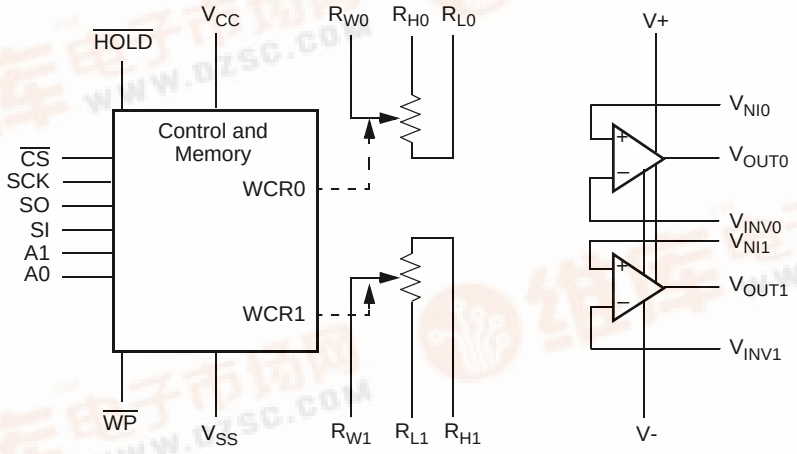
DESCRIPTION

The X9430 is a monolithic CMOS IC that incorporates two operational amplifiers and two nonvolatile digitally controlled potentiometers. The amplifiers are CMOS differential input voltage operational amplifiers with near rail-to-rail outputs. All pins for the two amplifiers are brought out of the package to allow combining them with the potentiometers or using them as complete stand-alone amplifiers.

The digitally controlled potentiometers consist of a series string of 63 polycrystalline resistors that behave as standard integrated circuit resistors. The SPI serial port, common to both pots, allows the user to program the connection of the wiper output to any of the resistor nodes in the series string. The wiper position is saved in the on board E2 memory to allow for nonvolatile restoration of the wiper position.

A wide variety of applications can be implemented using the potentiometers and the amplifiers. A typical application is to implement the amplifier as a wiper buffer in circuits that use the potentiometer as a voltage reference. The potentiometer can also be combined with the amplifier yielding a digitally programmable gain amplifier or programmable current source.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Host Interface Pins

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the device are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The SCK input is used to clock data into and out of the X9430.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9430 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{CS}$ LOW enables the X9430, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Hardware Write Protect Input $\overline{WP}$

The $\overline{WP}$ pin when low prevents nonvolatile writes to the wiper counter register.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

Device Address (A_0 - A_1)

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9430. A maximum of 4 devices may occupy the SPI serial bus.

Potentiometer Pins[1]

R_H (R_{H0} - R_{H1}), R_L (R_{L0} - R_{L1})

The R_H and R_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

R_W (R_{W0} - R_{W1})

The wiper output is equivalent to the wiper output of a mechanical potentiometer.

Amplifier and Device Pins

Amplifier Input Voltage $V_{NI}(0,1)$ and $V_{INV}(0,1)$

V_{NI} and V_{INV} are inputs to the noninverting (+) and inverting (-) inputs of the operational amplifiers.

Amplifier Output Voltage $V_{OUT}(0,1)$

V_{OUT} is the voltage output pin of the operational amplifier.

Analog Supplies V+, V-

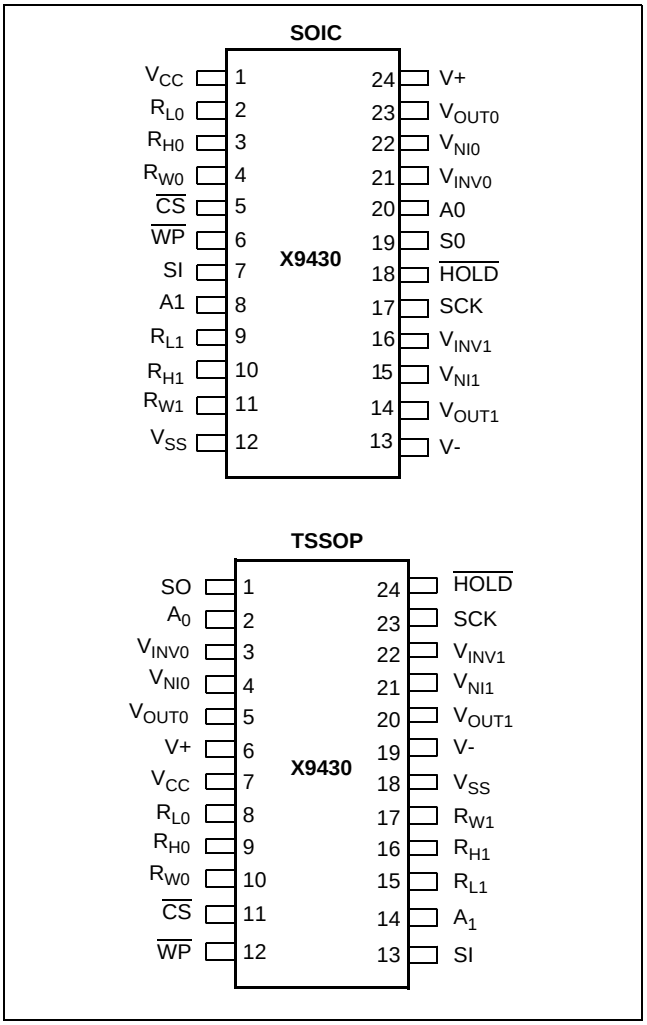
The Analog Supplies V+, V- are the supply voltages for the XDCP analog section and the operational amplifiers.

System Supply V_{CC} and Ground V_{SS}

The system supply V_{CC} and its reference V_{SS} is used to bias the interface and control circuits.

1. Alternate designations for R_H, R_L, R_W are V_H, V_L, V_W

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCK	Serial Clock
SI	Serial Input
SO	Serial Output
A0 - A1	Device Address
CS	Chip Select
HOLD	Hold
R_{H0} - R_{H1}, R_{L0} - R_{L1}	Potentiometers (terminal equivalent)
R_{W0} - R_{W1}	Potentiometers (wiper equivalent)
$V_{NI(0,1)}$, $V_{INV(0,1)}$	Amplifier Input Voltages
$V_{OUT0,}$ V_{OUT1}	Amplifier Outputs
WP	Hardware Write Protection
V+,V-	Analog and Voltage Amplifier Supplies
V_{CC}	System/Digital Supply Voltage
V_{SS}	System Ground

PRINCIPLES OF OPERATION

The X9430 is an integrated microcircuit incorporating two digitally controlled potentiometers, two operational amplifiers and their associated registers and counters; and the serial interface logic providing direct communication between the host and the digitally controlled potentiometers.

Serial Interface

The X9430 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

Potentiometer/Array Description

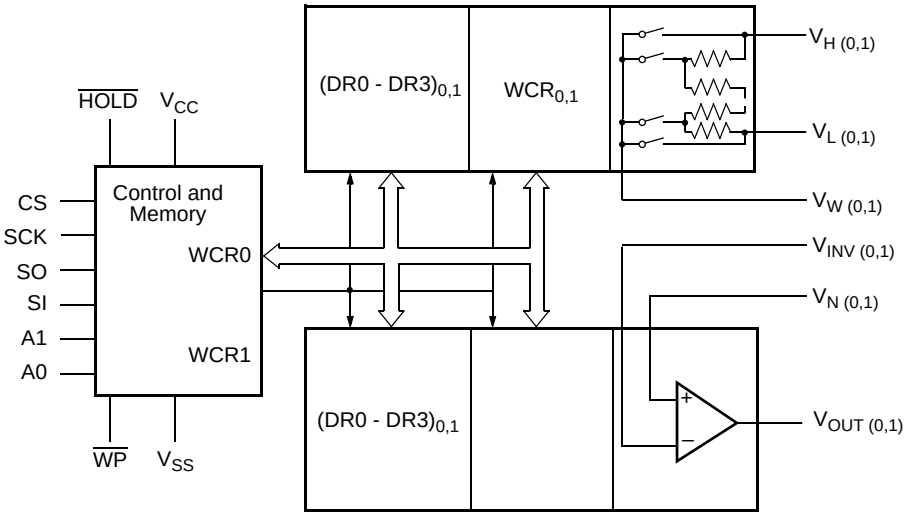
The X9430 is comprised of two resistor arrays and two operational amplifiers. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by a volatile wiper counter register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

Operational Amplifier

The voltage operational amplifiers are CMOS rail-to-rail output general purpose amplifiers. They are designed to operate from dual (±) power supplies. The amplifiers may be configured like any standard amplifier. All pins are externally available to allow connection with the potentiometers or as stand alone amplifiers.



Detailed Block Diagram
(One of 2 Circuits)

Write in Process

The contents of the data registers are saved to nonvolatile memory when the $\overline{CS}$ pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a write in process bit (WIP). The WIP bit is read with a read status command.

INSTRUCTIONS AND PROGRAMMING

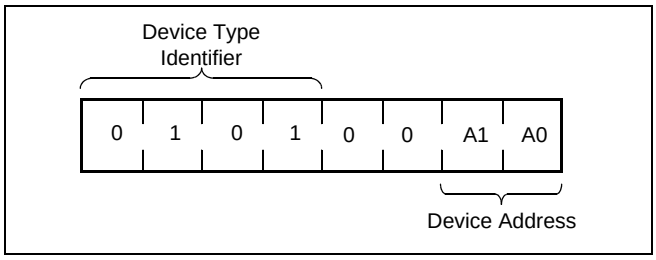
Identification (ID) Byte

The first byte sent to the X9430 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the identification byte. The most significant four bits of the slave address are a device type identifier, for the X9430 this is fixed as 0101[B] (refer to Figure 1).

The two least significant bits in the ID byte select one of four devices on the bus. The physical device address is defined by the state of the A_0 - A_1 input pins. The X9430 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9430 to successfully continue the command sequence. The A_0 - A_1 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

The remaining two bits in the slave byte must be set to 0.

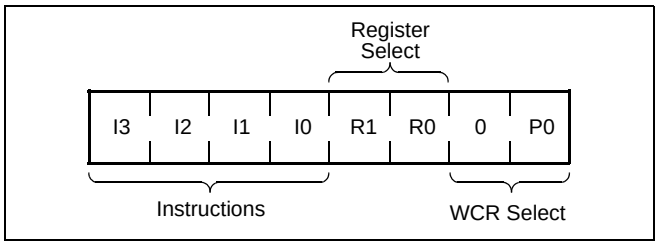
Figure 1. Identification Byte Format



Instruction Byte

The next byte sent to the X9430 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the WCRs of the two pots, and when applicable, they point to one of four associated data registers. The format is shown below in Figure 2.

Figure 2. Instruction Byte Format



The four high order bits of the instruction byte specify the operation. The next two bits (R_1 and R_0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last bit (P_0) selects which one of the two potentiometers is to be affected by the instruction.

Four of the ten instructions are two bytes in length and end with the transmission of the instruction byte.

The basic sequence of the two byte instructions is illustrated in Figure 3. These two-byte instructions exchange data between a wiper counter register and one of the four data registers associated with each. A transfer from a data register to a wiper counter register is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{WRL}. A transfer from the wiper counter register (current wiper position) to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the two potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between both of the potentiometers and one of their associated registers.

Five instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9430; either between the host and one of the data registers or directly between the host and the Wiper Counter and Registers. These instructions are: 1) Read Wiper Counter Register, read the current wiper position of the selected pot 2) Write Wiper Counter Register, i.e. change current wiper position of the selected pot; 3) Read Data Register, read the contents of the selected nonvolatile register; 4) Write Data Register, write a new value to the selected data register; 5)Read Status, returns the contents of the WIP bit which indicates if an internal write cycle is in progress.

The sequence of these operations is shown in Figure 4 and Figure 5.

The final command is Increment/Decrement. It is different from the other commands, because it's length is indeterminate. Once the command is issued, the master can clock the selected wiper up and/or down in one resistor segment steps; thereby, providing a fine tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the V_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the V_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figure 6 and Figure 7.

Figure 3. Two Byte Command Sequence

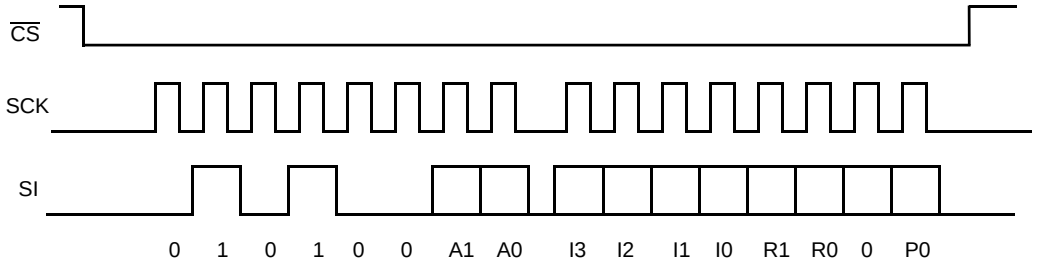


Figure 4. Three-Byte Command Sequence (Write)

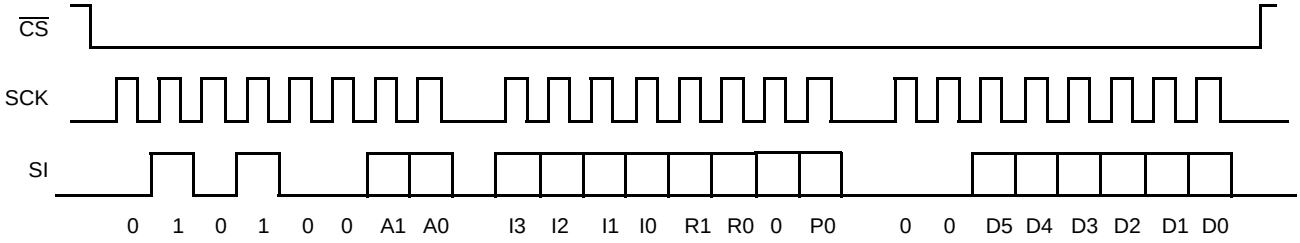


Figure 5. Three-Byte Command Sequence(Read)

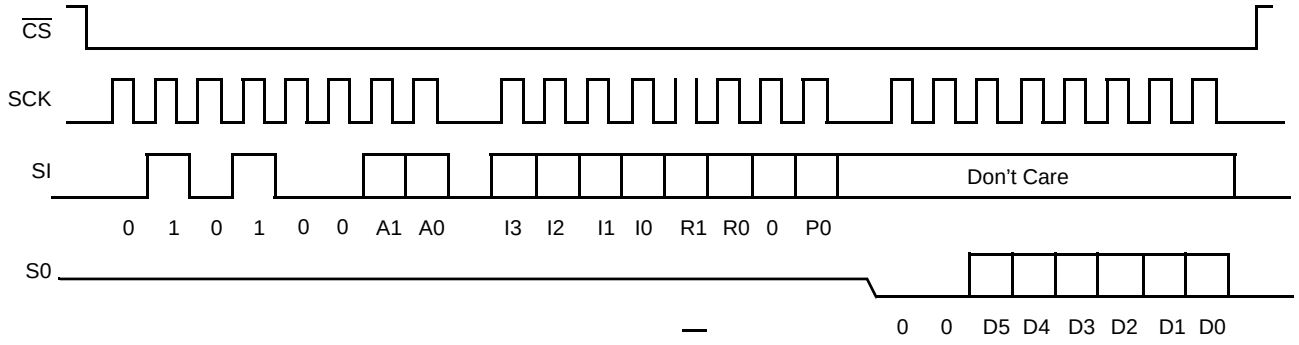


Figure 6. Increment/Decrement Command Sequence

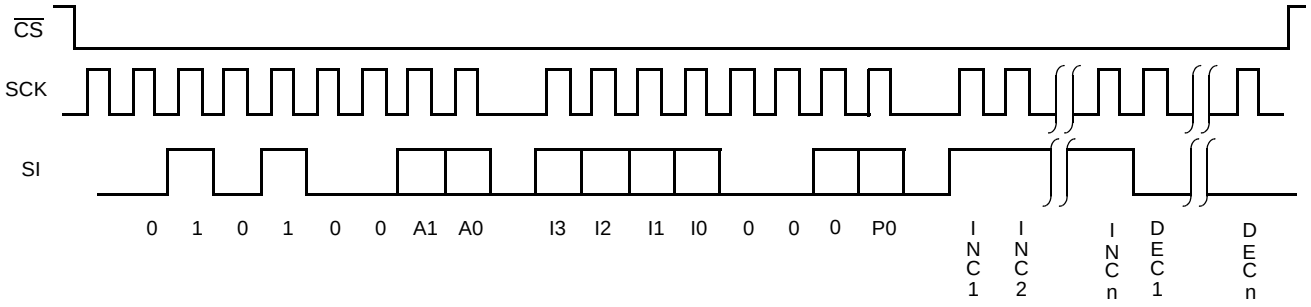
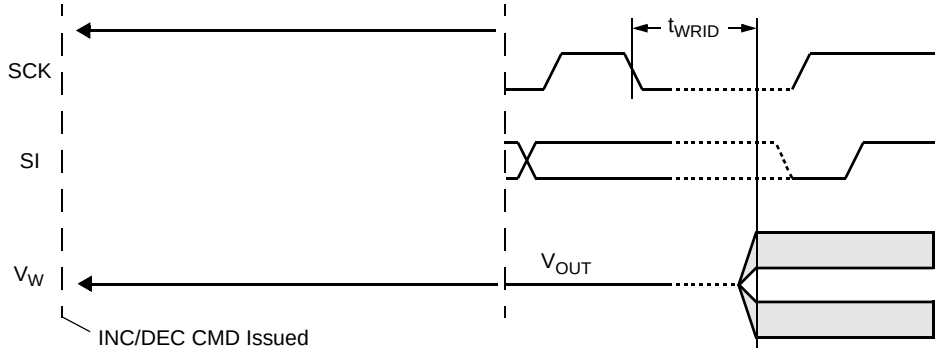


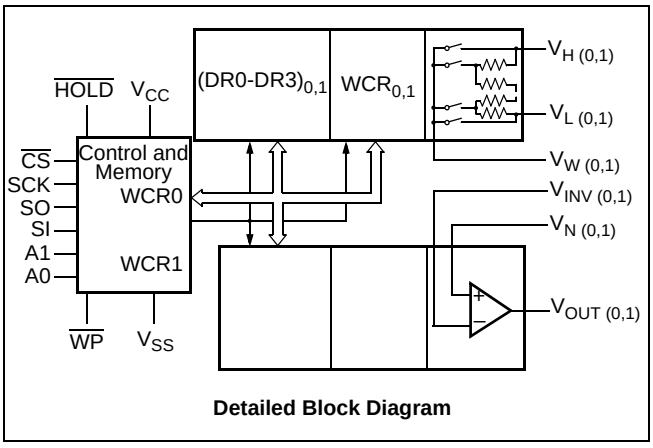
Figure 7. Increment/Decrement Timing



REGISTER OPERATION

Both digitally controlled potentiometers share the serial interface and share a common architecture. Each potentiometer is associated with a wiper counter register (WCR), and four data registers. Figure 8 illustrates the control, registers, and system features of the device.

Figure 8. System Block Diagram



Wiper Counter (WCR) and Analog Control Registers (ACR)

The X9430 contains two wiper counter registers, one for each XDCP. The wiper counter register is equivalent to a serial-in, parallel-out counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the wiper counter register can be altered in four ways: it may be written directly by the host via the write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers (DR) via the XFR data register instruction (parallel load); it can be modified one step at a time by the increment/decrement instruction (WCR only). Finally, it may be loaded with the contents of its associated data register zero (R0) upon power-up.

The wiper counter register is a volatile register; that is, its contents are lost when the X9430 is powered-down. Although the registers are automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers (DR)

Each potentiometer has four nonvolatile data registers (DR). These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could store system parameters or user preference data.

REGISTER DESCRIPTIONS AND MEMORY MAP

Memory Map

WCRO	WCR1
DR0	DR0
DR1	DR1
DR2	DR2
DR3	DR3

Wiper Counter Register (WCR)

0	0	WP5	WP4	WP3	WP2	WP1	WP0
			(volatile)				(LSB)

WP0 - WP5 identify wiper position.

Data Registers (DR, R0 - R3)

Wiper Position or User Data

(Nonvolatile)

Instruction Format

Notes: (1) “A1 ~ A0”: stands for the device addresses sent by the master.
(2) WPx refers to wiper position data in the Wiper Counter Register
(3) “I”: stands for the increment operation, SI held HIGH during active SCK phase (high).
(4) “D”: stands for the decrement operation, SI held LOW during active SCK phase (high).

Read Wiper Counter Register (WCR)

Read the contents of the Wiper Counter Register pointed to by P_1 - P_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				wiper position (sent by X9430 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	0	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Write Wiper Counter Register (WCR)

Write new value to the Wiper Counter Register pointed to by P_1 - P_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				Data Byte (sent by Host on SI)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	0	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Read Data Register (DR)

Read the contents of the Register pointed to by P_1 - P_0 and R_1 - R_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR/WCR addresses				Data Byte (sent by X9430 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	1	1	R1	R0	0	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Write Data Register (DR)

Write new value to the Register pointed to by P_1 - P_0 and R_1 - R_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR/WCR addresses				Data Byte (sent by host on SI)								$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	0	0	R1	R0	0	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Transfer Data Register (DR) to Wiper Counter Register (WCR)

Transfer the contents of the Register pointed to by R_1 - R_0 to the WCR

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR/WCR addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	R1	R0	0	P0	

Transfer Wiper Counter Register (WCR) to Data Register (DR)

Transfer the contents of the WCR to the Register pointed to by R_1 - R_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR/WCR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	R1	R0	0	P0		

P_0: 0-WCR0, 1-WCR1

Increment/Decrement Wiper Counter Register (WCR)

Enable Increment/decrement of the WCR pointed to by P_1 - P_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				increment/decrement (sent by master on SDA)						$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	1	0	X	X	0	P0	I/D	I/D	.	.	I/D	I/D	

Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

Transfer the contents of all four Data Registers pointed to by R_1 - R_0 to their respective WCR

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	0	1	R1	R0	0	0	

Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

Transfer the contents of all WCRs to their respective data Registers pointed to by R_1 - R_0

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	0	0	0	R1	R0	0	0		

Read Status

Returns the contents of the WIP bit which indicates if an internal write cycle is in progress

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				wiper addresses				Data Byte (sent by X9430 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on SCK, SCL or any
address input with respect to V_{SS} ..... -1V to +7V
Voltage on V+ (referenced to V_{SS}) .....+7V
Voltage on V- (referenced to V_{SS}) .....-7V
(V+) - (V-) 10V
Any V_H.....V+
Any V_L .....V-
Lead temperature (soldering, 10 seconds)..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Device	Supply Voltage (V_{CC}) Limits
X9430	5V ±10%
X9430-2.7	2.7V to 5.5V

POTENTIOMETER CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter		Limits				Test Conditions
			Min.	Typ.	Max.	Unit	
R_{TOTAL}	End to end resistance		-20		+20	%	
	Power rating				50	mW	25°C, each pot
I_W	Wiper current		-3		+3	mA	
R_W	Wiper resistance			40	100	Ω	V+ = 5V, V- = -5V, I_W = 3mA
				100	250	Ω	V+ = 2.7V, V- = -2.7V, I_W = 1mA
Vv+	Voltage on V+ pin	X9430	+4.5		+5.5	V	
		X9430-2.7	+2.7		+5.5		
Vv-	Voltage on V- pin	X9430	-5.5		-4.5	V	
		X9430-2.7	-5.5		-2.7		
V_{TERM}	Voltage on any R_H or R_L pin		V-		V+	V	
	Noise			-100		dBv	Ref: 1V
	Resolution (4)			1.6		%	
	Absolute linearity (1)		-1		+1	MI(3)	$V_{w(n)(actual)} - V_{w(n)(expected)}$
	Relative linearity (2)		-0.2		+0.2	MI(3)	$V_{w(n+1)} - [V_{w(n)} + MI]$
	Temperature coefficient of R_{TOTAL}			±300		ppm/°C	
	Ratiometric temperature coefficient				±20	ppm/°C	

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or (R_H - R_L)/63, single pot (=LSB)
(4) Individual array resolutions

AMPLIFIER ELECTRICAL CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Industrial			Commercial			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage	V+/V- ±3V to ±5V		1	3		1	2	mV
TC_{VOS}	Input Offset Voltage Temp. Coefficient	V+/V- ±3V to ±5V		-10			-10		µV/°C
I_B	Input bias current	V+/V- ±3V to ±5V		50			50		pA
I_{OS}	Input offset current	V+/V- ±3V to ±5V		25			25		pA
CMRR	Common mode rejection ratio	V_{CM} = -1V to +1V	70			70			dB
PSRR	Power supply rejection ratio	V+/V- ±3V to ±5V	70			70			dB
V_{CM}	Input common mode voltage range	T_j = 25°C	V-		V+	V-		V+	V
A_V	Large signal voltage gain	V_O = -1V to + 1V	30	50		30	50		V/mV
V_O	Output voltage swing	V- V+	+0.1		 -.15	+0.1		 -.15	V V
I_O	Output current	V+/V- = ±5.5V V+/V- = ±3.3V	50 30			50 30			mA mA
I_S	Supply current	V+/V- = ±5.0V			3			3	mA
		V+/V- = ±3.0V			1.5			1.5	mA
GB	Gain-bandwidth prod	R_L = 100k, C_L = 50pf		1.0			1.0		MHz
SR	Slew rate	R_L = 100k, C_L = 50pf		1.5			1.5		V/µsec
Φ_M	Phase margin	R_L = 100k, C_L = 50pf		80			80		Deg.

V+ and V- (±5V to ±3V) are the amplifier power supplies. The amplifiers are specified with dual power supplies. V_{CC} and V_{SS} are the logic supplies. All ratings are over the temperature range for the Industrial (-40 to + 85°C) and Commercial (0 to 70°C) versions of the part unless specified differently.

POTENTIOMETER D.C. OPERATING CHARACTERISTICS

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I_{CC1}	V_{CC} supply current (active)			400	µA	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}
I_{CC2}	V_{CC} supply current (nonvolatile write)			1	mA	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} current (standby)			1	µA	SCK = SI = V_{SS}, Addr. = V_{SS}
I_{LI}	Input leakage current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Input LOW voltage	-0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 3mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per register
Data retention	100	years

CAPACITANCE

Symbol	Test	Typ.	Max.	Unit	Test Conditions
C_{OUT}(5)	Output capacitance (SO)		8	pF	V_{OUT} = 0V
C_{IN}(5)	Input capacitance (A0, A1, SI, $\overline{WP}$, $\overline{HOLD}$ and SCK)		6	pF	V_{IN} = 0V
C_L | C_H | C_W	Potentiometer capacitance	10/10/2		pF	

POWER-UP TIMING

Symbol	Parameter	Max.	Unit
t_{PUR}(6)	Power-up to initiation of read operation	1	ms
t_{PUW}(6)	Power-up to initiation of write operation	5	ms

A.C. TEST CONDITIONS

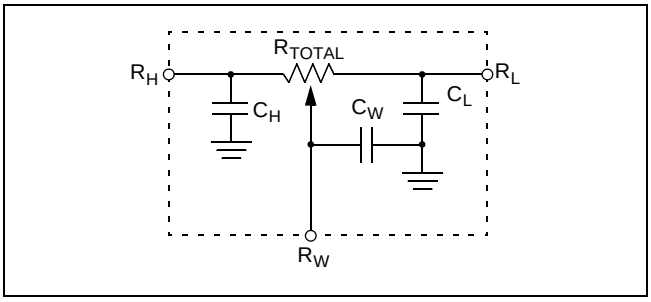
Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

Notes: (5) This parameter is periodically sampled and not 100% tested.

(6) t_{PUR} and t_{PUW} are the delays required from the time the third (last) power supply (V_{CC}, V+ or V-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

(7) The power-up order of power supplies are V_{CC}, V+ and V-.

SPICE Macro Model



AC TIMING

Symbol	Parameter	Min.	Max.	Unit
f_{SCK}	SSI/SPI clock frequency		2.0	MHz
t_{CYC}	SSI/SPI clock cycle time	500		ns
t_{WH}	SSI/SPI clock high time	200		ns
t_{WL}	SSI/SPI clock low time	200		ns
t_{LEAD}	Lead time	250		ns
t_{LAG}	Lag time	250		ns
t_{SU}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time	50		ns
t_H	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time	50		ns
t_{RI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time		2	µs
t_{FI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time		2	µs
t_{DIS}	SO output disable time	0	500	ns
t_V	SO output valid time		200	ns
t_{HO}	SO output hold time	0		ns
t_{RO}	SO output rise time		50	ns
t_{FO}	SO output fall time		50	ns
t_{HOLD}	$\overline{HOLD}$ time	400		ns
t_{HSU}	$\overline{HOLD}$ setup time	100		ns
t_{HH}	$\overline{HOLD}$ hold time	100		ns
t_{HZ}	$\overline{HOLD}$ low to output in high Z		100	ns
t_{LZ}	$\overline{HOLD}$ high to output in low Z		100	ns
T_I	Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		20	ns
t_{CS}	$\overline{CS}$ deselect time	2		µs
t_{WPASU}	$\overline{WP}$, A0 and A1 setup time	0		ns
t_{WPAH}	$\overline{WP}$, A0 and A1 hold time	0		ns

HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Unit
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

V_{CC} RAMP (sample tested)

Symbol	Parameter	Typ.	Max.	Unit
trV_{CC}	V_{CC} power-up rate	.2	50	V/ms

DCP Timing

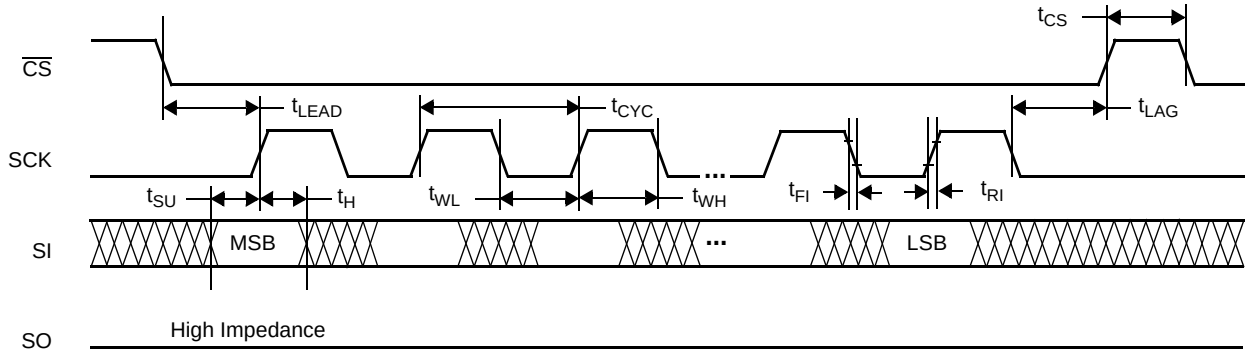
Symbol	Parameter	Min.	Max.	Unit
t_{WRPO}	Wiper response time after the third (last) power supply is stable		10	µs
t_{WRL}	Wiper response time after instruction issued (all load instructions)		10	µs
t_{WRID}	Wiper response time from an active SCL/SCK edge (increment/decrement instruction)		10	µs

SYMBOL TABLE

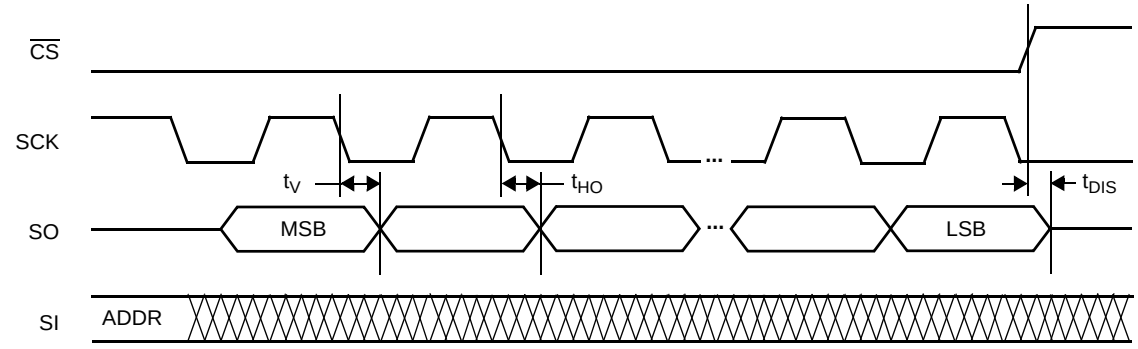
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

TIMING DIAGRAMS

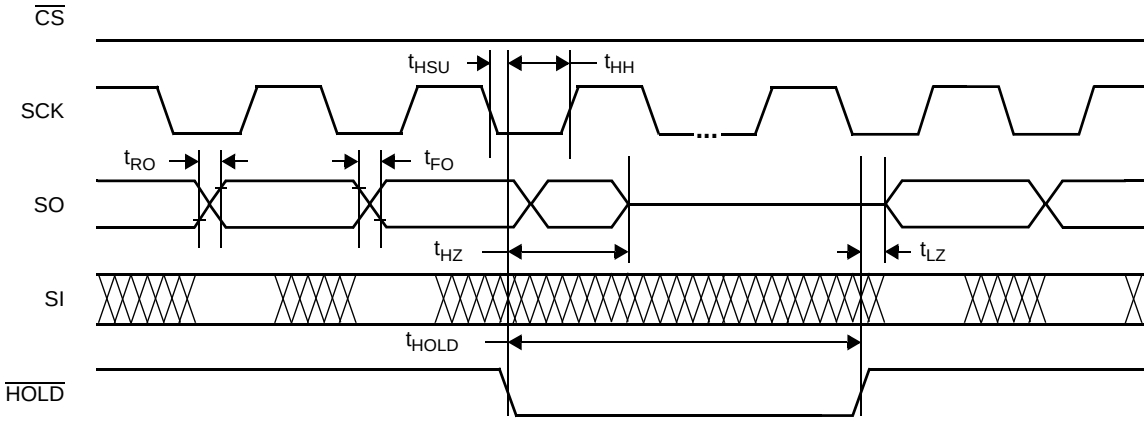
Input Timing



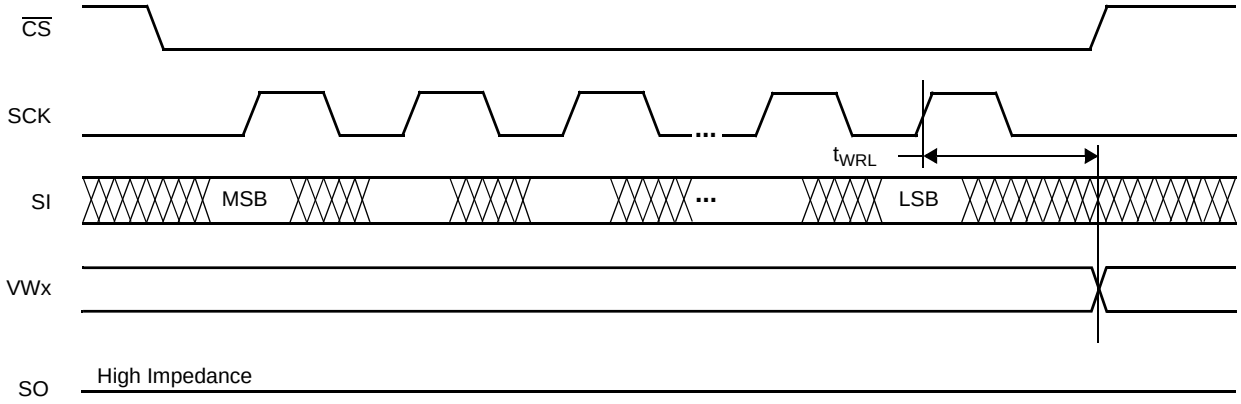
Output Timing



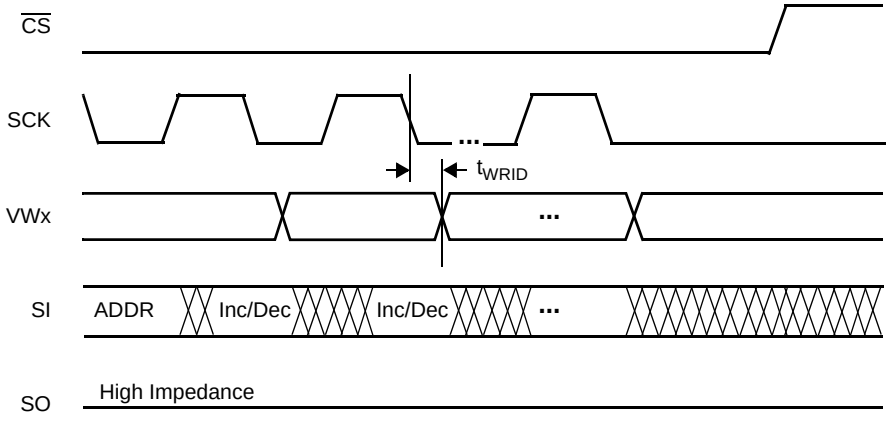
Hold Timing



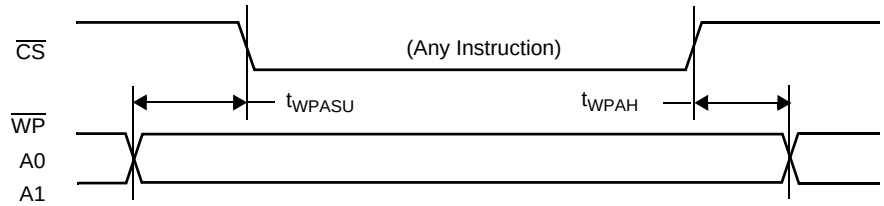
DCP Timing (for All Load Instructions)



DCP Timing (for Increment/Decrement Instruction)

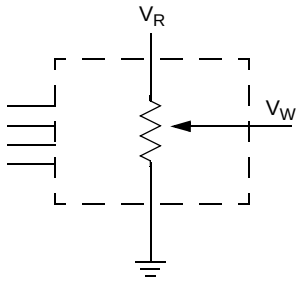


Write Protect and Device Address Pins Timing

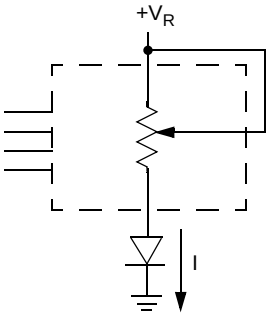


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



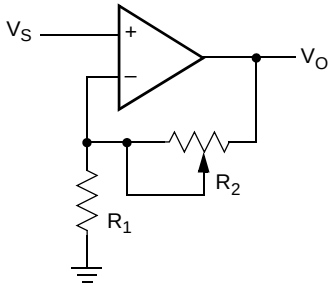
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

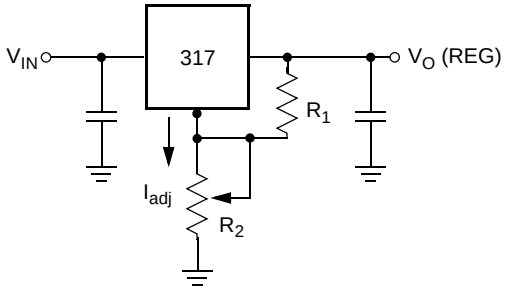
Application Circuits

Noninverting Amplifier



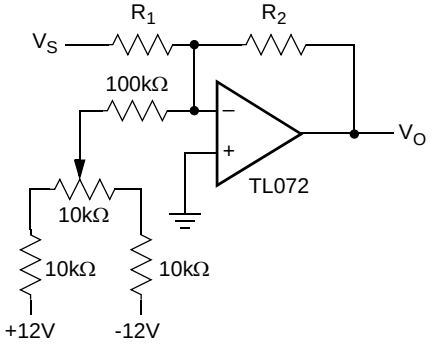
$V_O = (1+R_2/R_1)V_S$

Voltage Regulator

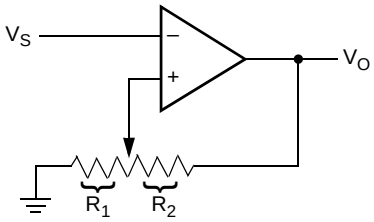


V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj} R_2$

Offset Voltage Adjustment



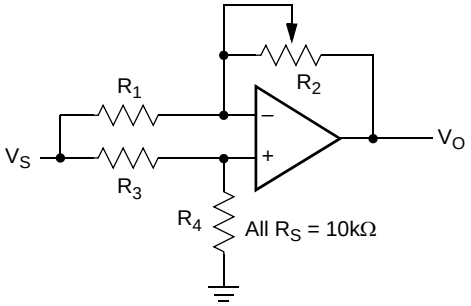
Comparator with Hysterisis



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

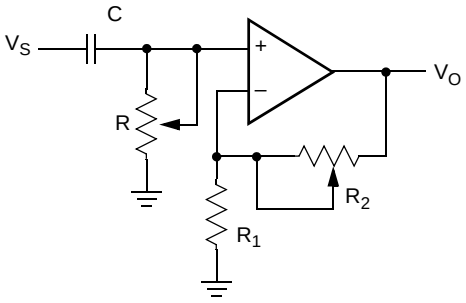
Application Circuits (continued)

Attenuator



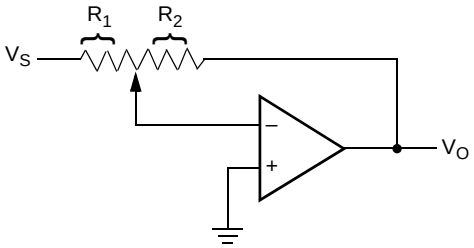
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

Filter



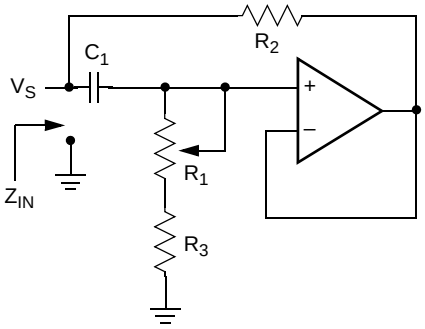
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

Inverting Amplifier



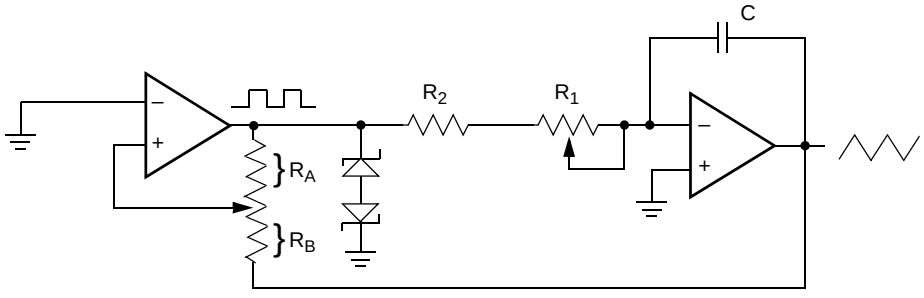
$V_O = G\ V_S$
$G = -R_2/R_1$

Equivalent L-R Circuit



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

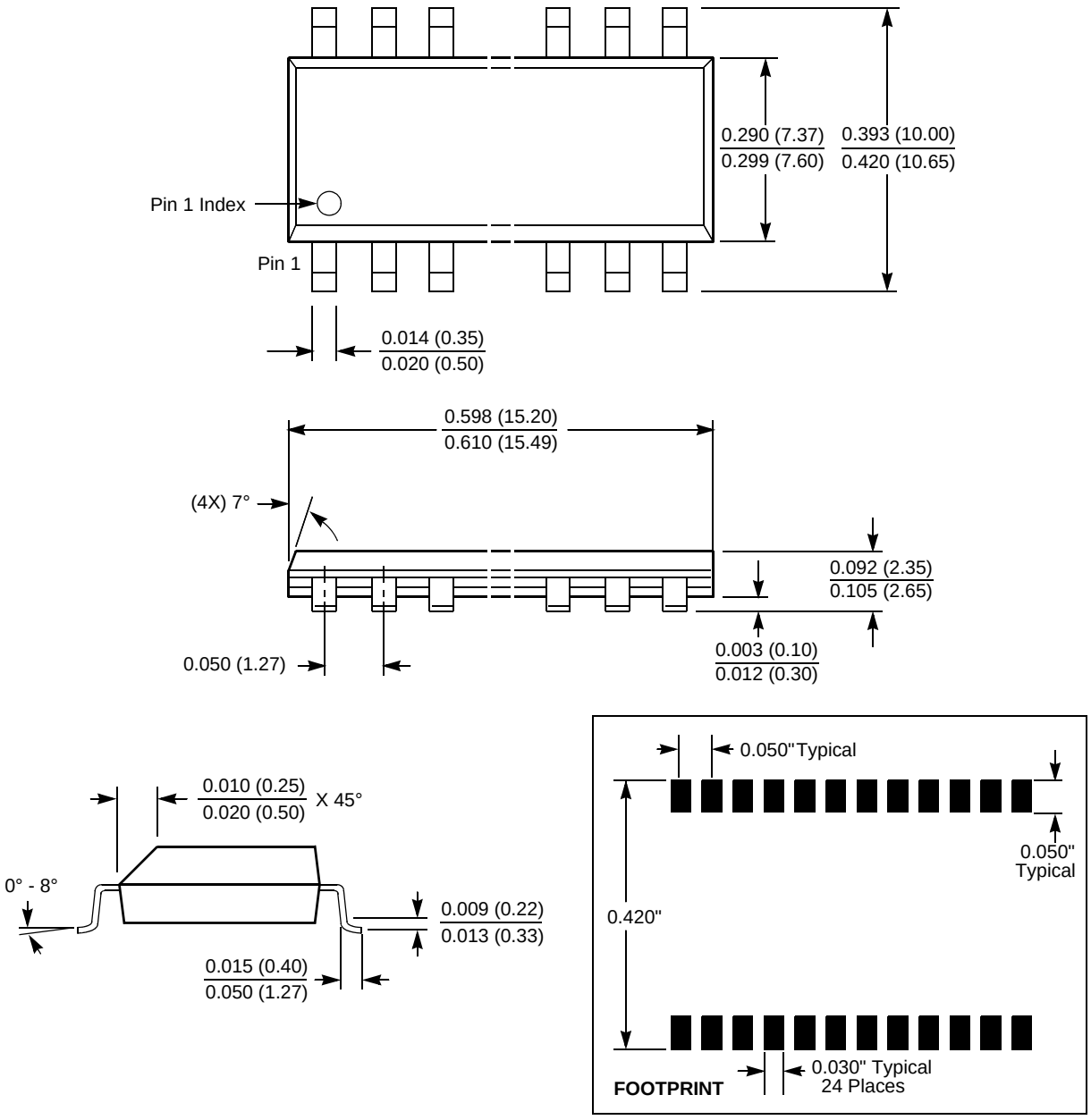
Function Generator



frequency μ R_1, R_2, C
amplitude μ R_A, R_B

PACKAGING INFORMATION

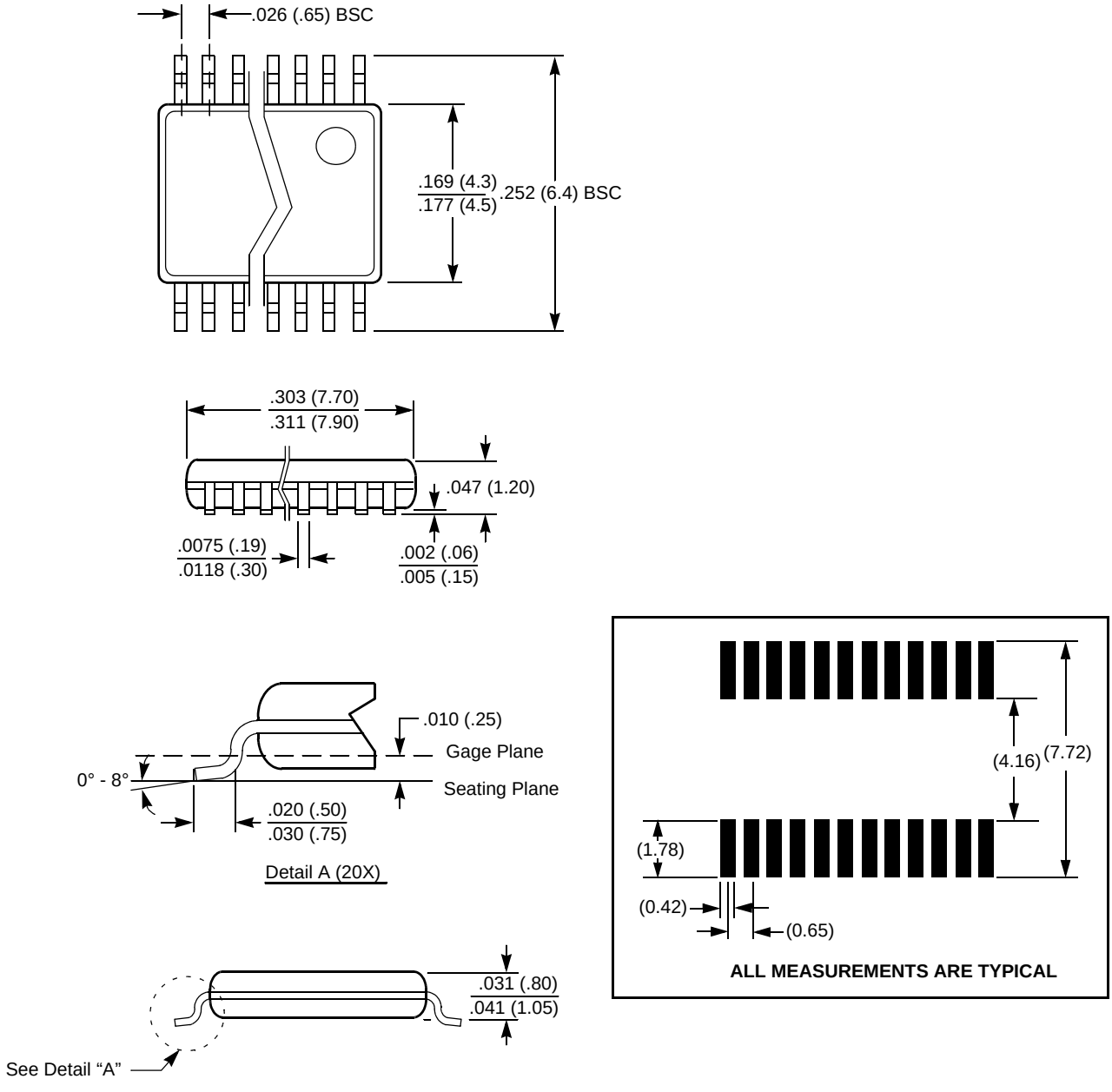
24-Lead Plastic Small Outline Gull Wing Package Type S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

24-Lead Plastic, TSSOP Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information