SDLS153 – D2628, JANUARY 1981 – REVISED MARCH 1988

- **Count Divider Chain**
- **Digitally Programmable from $2^2$ to $2^n$ (n = 31 for 'LS292, n = 15 for 'LS294)**
- **Useable Frequency Range from DC to 30 MHz**
- **Easily Expandable**
- **Applications**
  - **Frequency Division**
  - **Digital Timing**

## description

These programmable frequency dividers/digital timers contain 31 flip-flops plus 30 gates ('LS292) or 15 flip-flops plus 29 gates ('LS294) on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'LS292 and TP on the 'LS294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the function table below.)

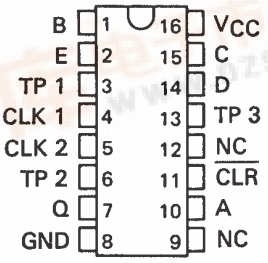
A brief look at the digital timing capabilities of the 'LS292 will show that with a 1-MHz input frequency, programming for $2^{10}$ will give a period of 1.024 ms, and $2^{20}$ will give a period of 1.05 sec, $2^{26}$ will give a period of 1.12 min, and $2^{31}$ will give a period of 35.79 min.

These devices are easily cascadable giving limitless possibilities to timing delays that can be achieved.

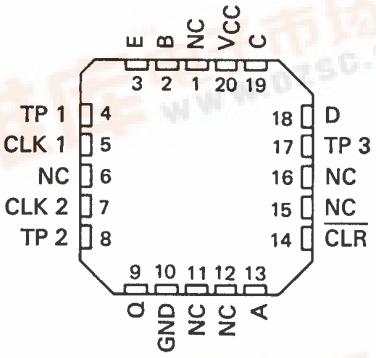
FUNCTION TABLE

| CLEAR | CLK 1 | CLK 2 | Q OUTPUT MODE |
|---|---|---|---|
| L | X | X | Cleared to L |
| H | ↑ | L | Count |
| H | L | ↑ | Count |
| H | H | X | Inhibit |
| H | X | H | Inhibit |

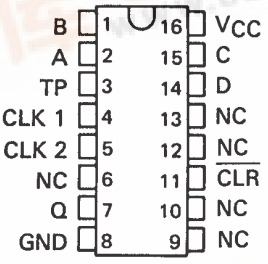
SN54LS292 . . . J OR W PACKAGE
SN74LS292 . . . N PACKAGE
(TOP VIEW)



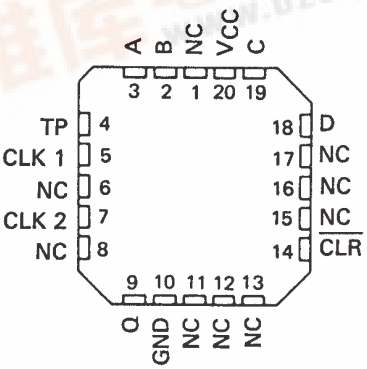

SN54LS292 . . . FK PACKAGE
(TOP VIEW)




SN54LS294 . . . J OR W PACKAGE
SN74LS294 . . . N PACKAGE
(TOP VIEW)




SN54LS294 . . . FK PACKAGE
(TOP VIEW)

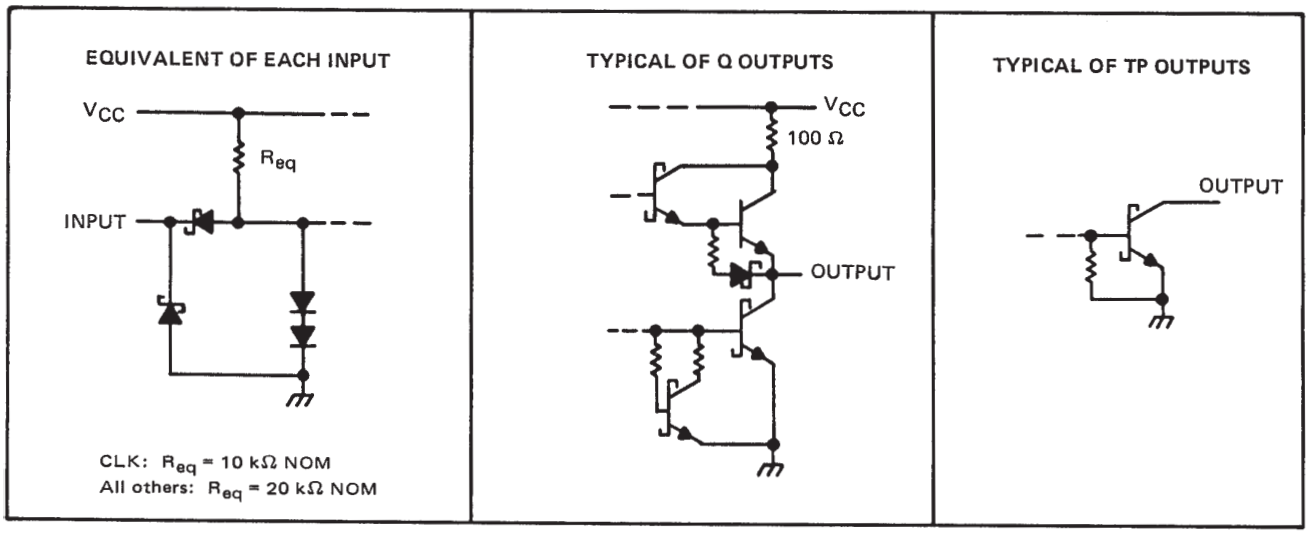



NC — No internal connection.



TEXAS INSTRUMENTS

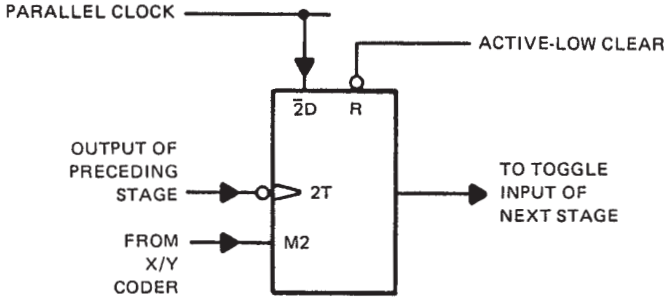
## schematics of inputs and outputs



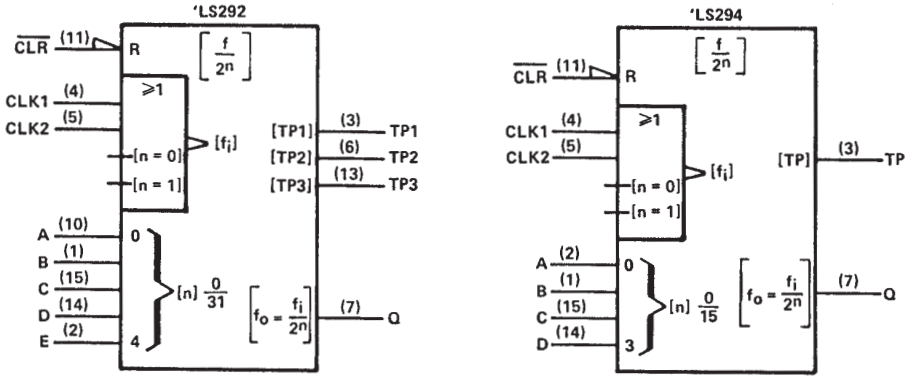

## operation

The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode control inputs of several flip-flops. These flip flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of that flip-flop is enabled, and the signal from the parallel clock line ($f_{in} \div 4$) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.



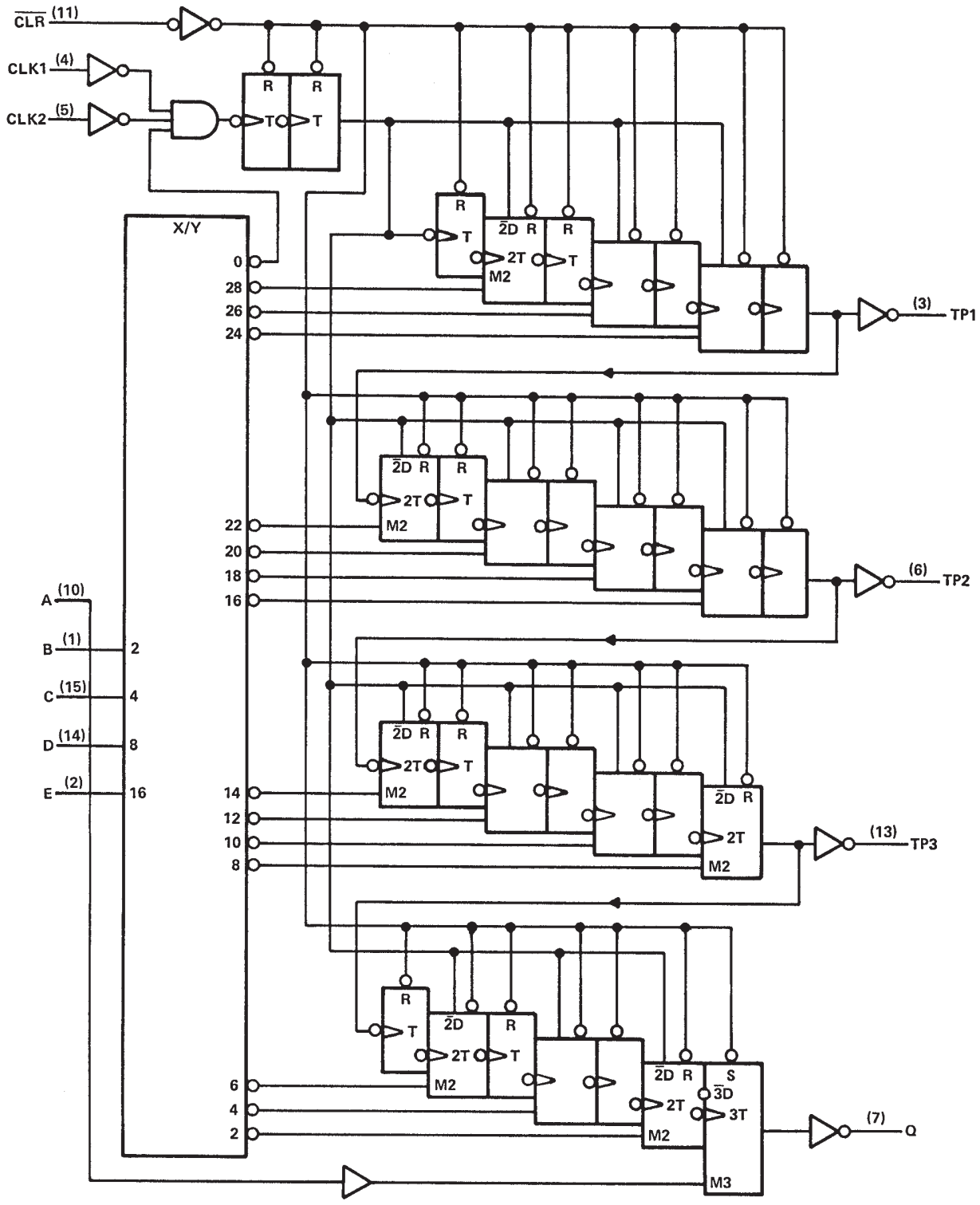

## logic symbols†




†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, N, and W packages.

## logic diagram (positive logic)

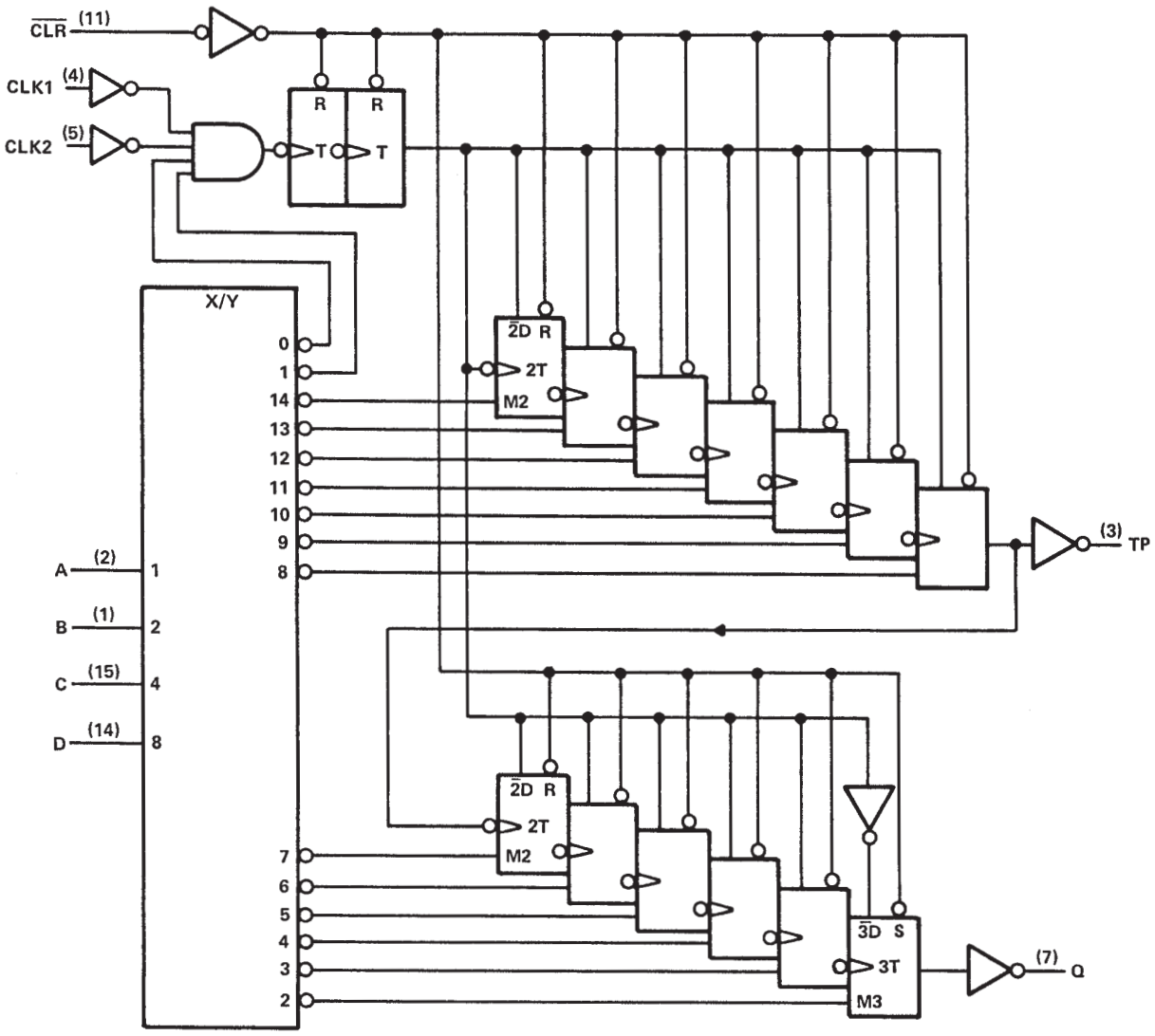
'LS292




Pin numbers shown are for J, N, and W packages.

## logic diagram (positive logic)

'LS294




Pin numbers shown are for J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | | |
|---|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | | 7 V |
| Input voltage | | 7 V |
| Operating free-air temperature range: | SN54LS292, SN54LS294 | –55°C to 125°C |
| | SN74LS292, SN74LS294 | 0°C to 70°C |
| Storage temperature range | | –65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current (Q only) | | | | −1.2 | | | −1.2 | mA |
| $I_{OL}$ | Low-level output current (Q only) | | | | 12 | | | 24 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 30 | 0 | | 30 | MHz |
| $t_w$ | Duration of clock input pulse | | 16 | | | 16 | | | ns |
| $t_w$ | Duration of clear pulse | 'LS292 | 55 | | | 55 | | | ns |
| | | 'LS294 | 35 | | | 35 | | | |
| $t_{su}$ | Clear inactive-state setup time | | 15 | | | 15 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | Q | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OH}$ = −1.2 mA, | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Q | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | TP¶ | | $I_{OL}$ = 0.5 mA | | | | | 0.25 | 0.4 | |
| $I_I$ | | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | CLK1, CLK2 | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.8 | | | −0.8 | mA |
| | All others | | | | | −0.4 | | | −0.4 | |
| $I_{OS}$§ | Q | $V_{CC}$ = MAX | | −30 | | −130 | −30 | | −130 | mA |
| $I_{CC}$ | 'LS292 | $V_{CC}$ = MAX, All inputs grounded, All outputs open | | | 40 | 75 | | 40 | 75 | mA |
| | 'LS294 | | | | 30 | 50 | | 30 | 50 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The duration of the short-circuit should not exceed one second.
¶ The TP output or outputs are not intended to drive external loads but are solely provided for test points.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C, $R_L$ = 667 Ω, $C_L$ = 45 pF (see Figure 1)

| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS292 | | | 'LS294 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{max}$ | CLK1 or 2 | | | 30 | 50 | | 30 | 50 | | MHz |
| $t_{PLH}$ | | Q | Modulo set at 22, A thru E = LLLHL ('LS292) A thru D = LLHL ('LS294) | | 55 | 90 | | 55 | 90 | ns |
| $t_{PHL}$ | | Q | | | 80 | 120 | | 80 | 120 | ns |
| $t_{PHL}$ | $\overline{CLR}$ | Q | | | 85 | 130 | | 35 | 65 | ns |

†$f_{MAX}$ = maximum clock frequency
$t_{PLH}$ = Propagation delay time, low-to-high-level output
$t_{PHL}$ = Propagation delay time, high-to-low-level output
NOTE 2: Load circuits and voltage waveforms are shown in Section 1. To be used on TP outputs only.

### 'LS292 FUNCTION TABLE

| PROGRAMMING INPUTS | | | | | FREQUENCY DIVISION | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Q | | TP1 | | TP2 | | TP3 | |
| E | D | C | B | A | BINARY | DECIMAL | BINARY | DECIMAL | BINARY | DECIMAL | BINARY | DECIMAL |
| L | L | L | L | L | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit |
| L | L | L | L | H | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit | Inhibit |
| L | L | L | H | L | $2^2$ | 4 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| L | L | L | H | H | $2^3$ | 8 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| L | L | H | L | L | $2^4$ | 16 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| L | L | H | L | H | $2^5$ | 32 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| L | L | H | H | L | $2^6$ | 64 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| L | L | H | H | H | $2^7$ | 128 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| L | H | L | L | L | $2^8$ | 256 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^2$ | 4 |
| L | H | L | L | H | $2^9$ | 512 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^2$ | 4 |
| L | H | L | H | L | $2^{10}$ | 1,024 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^4$ | 16 |
| L | H | L | H | H | $2^{11}$ | 2,048 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^4$ | 16 |
| L | H | H | L | L | $2^{12}$ | 4,096 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^6$ | 64 |
| L | H | H | L | H | $2^{13}$ | 8,192 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^6$ | 64 |
| L | H | H | H | L | $2^{14}$ | 16,384 | $2^9$ | 512 | Disabled Low | | $2^8$ | 256 |
| L | H | H | H | H | $2^{15}$ | 32,768 | $2^9$ | 512 | Disabled Low | | $2^8$ | 256 |
| H | L | L | L | L | $2^{16}$ | 65,536 | $2^9$ | 512 | $2^3$ | 8 | $2^{10}$ | 1,024 |
| H | L | L | L | H | $2^{17}$ | 131,072 | $2^9$ | 512 | $2^3$ | 8 | $2^{10}$ | 1,024 |
| H | L | L | H | L | $2^{18}$ | 262,144 | $2^9$ | 512 | $2^5$ | 32 | $2^{12}$ | 4,096 |
| H | L | L | H | H | $2^{19}$ | 524,288 | $2^9$ | 512 | $2^5$ | 32 | $2^{12}$ | 4,096 |
| H | L | H | L | L | $2^{20}$ | 1,048,576 | $2^9$ | 512 | $2^7$ | 128 | $2^{14}$ | 16,384 |
| H | L | H | L | H | $2^{21}$ | 2,097,152 | $2^9$ | 512 | $2^7$ | 128 | $2^{14}$ | 16,384 |
| H | L | H | H | L | $2^{22}$ | 4,194,304 | Disabled Low | | $2^9$ | 512 | $2^{16}$ | 65,536 |
| H | L | H | H | H | $2^{23}$ | 8,388,608 | Disabled Low | | $2^9$ | 512 | $2^{16}$ | 65,536 |
| H | H | L | L | L | $2^{24}$ | 16,777,216 | $2^3$ | 8 | $2^{11}$ | 2,048 | $2^{18}$ | 262,144 |
| H | H | L | L | H | $2^{25}$ | 33,554,432 | $2^3$ | 8 | $2^{11}$ | 2,048 | $2^{18}$ | 262,144 |
| H | H | L | H | L | $2^{26}$ | 67,108,864 | $2^5$ | 32 | $2^{13}$ | 8,192 | $2^{20}$ | 1,048,576 |
| H | H | L | H | H | $2^{27}$ | 134,217,728 | $2^5$ | 32 | $2^{13}$ | 8,192 | $2^{20}$ | 1,048,576 |
| H | H | H | L | L | $2^{28}$ | 268,435,456 | $2^7$ | 128 | $2^{15}$ | 32,768 | $2^{22}$ | 4,194,304 |
| H | H | H | L | H | $2^{29}$ | 536,870,912 | $2^7$ | 128 | $2^{15}$ | 32,768 | $2^{22}$ | 4,194,304 |
| H | H | H | H | L | $2^{30}$ | 1,073,741,824 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |
| H | H | H | H | H | $2^{31}$ | 2,147,483,648 | $2^9$ | 512 | $2^{17}$ | 131,072 | $2^{24}$ | 16,777,216 |

**'LS294 FUNCTION TABLE**

| PROGRAMMING INPUTS | | | | FREQUENCY DIVISION | | | |
|---|---|---|---|---|---|---|---|
| | | | | Q | | TP | |
| D | C | B | A | BINARY | DECIMAL | BINARY | DECIMAL |
| L | L | L | L | Inhibit | Inhibit | Inhibit | Inhibit |
| L | L | L | H | Inhibit | Inhibit | Inhibit | Inhibit |
| L | L | H | L | $2^2$ | 4 | $2^9$ | 512 |
| L | L | H | H | $2^3$ | 8 | $2^9$ | 512 |
| L | H | L | L | $2^4$ | 16 | $2^9$ | 512 |
| L | H | L | H | $2^5$ | 32 | $2^9$ | 512 |
| L | H | H | L | $2^6$ | 64 | $2^9$ | 512 |
| L | H | H | H | $2^7$ | 128 | Disabled Low | |
| H | L | L | L | $2^8$ | 256 | $2^2$ | 4 |
| H | L | L | H | $2^9$ | 512 | $2^3$ | 8 |
| H | L | H | L | $2^{10}$ | 1,024 | $2^4$ | 16 |
| H | L | H | H | $2^{11}$ | 2,048 | $2^5$ | 32 |
| H | H | L | L | $2^{12}$ | 4,096 | $2^6$ | 64 |
| H | H | L | H | $2^{13}$ | 8,192 | $2^7$ | 128 |
| H | H | H | L | $2^{14}$ | 16,384 | $2^8$ | 256 |
| H | H | H | H | $2^{15}$ | 32,768 | $2^9$ | 512 |

**switching loads**

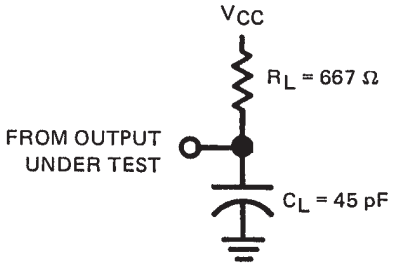
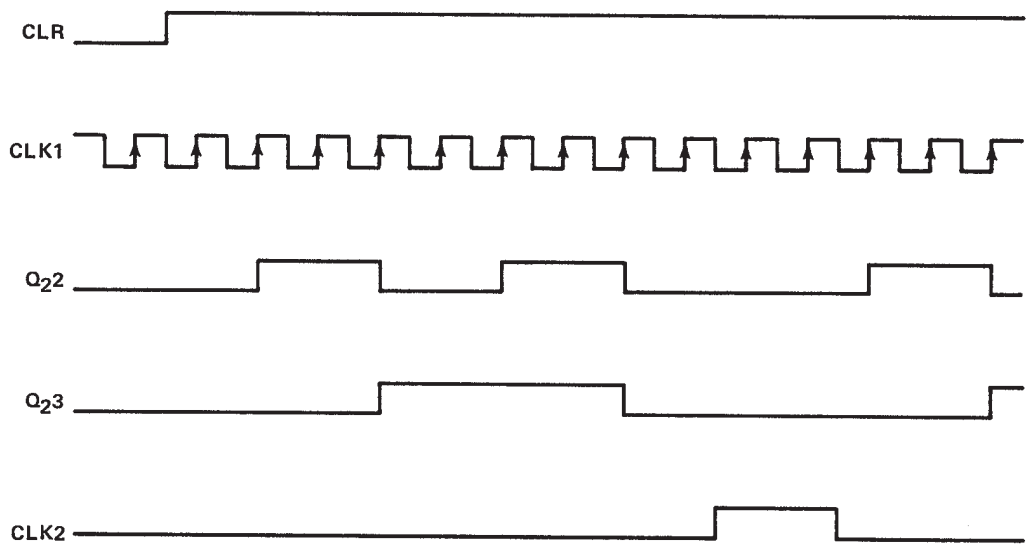



**FIGURE 1**

**'LS292 and 'LS294 timing diagram**



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