DATA SHEET

PCA9534

8-bit I²C and SMBus, low power I/O port with interrupt

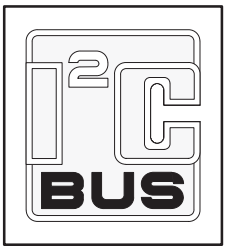
Product data sheet
Supersedes data of 2003 Dec 02

2004 Sep 30

Philips Semiconductors

PHILIPS

8-bit I²C and SMBus low power I/O port with interrupt PCA9534



FEATURES

- 8-bit I²C GPIO
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active low interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 kHz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Offered in three different packages: SO16, TSSOP16, and HVQFN16

DESCRIPTION

The PCA9534 is a16-pin CMOS device that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C/SMBus applications and was developed to enhance the Philips family of I²C I/O expanders. The improvements include higher drive capability, 5V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc.

The PCA9534 consist of an 8-bit Configuration register (Input or Output selection); 8-bit Input register, 8-bit Output register and an 8-bit Polarity inversion register (Active HIGH or Active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the input port register can be inverted with the Polarity Inversion Register. All registers can be read by the system master. Although pin-to-pin and I²C address compatible with the PCF8574 series, software changes are required due to the enhancements and are discussed in *Application Note AN469*.

The PCA9534 is identical to the PCA9554 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW.

The PCA9534 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C address and allow up to eight devices to share the same I²C/SMBus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
16-Pin Plastic SO (wide)	–40 °C to +85 °C	PCA9534D	PCA9534D	SOT162-1
16-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9534PW	PCA9534	SOT403-1
16-Pin Plastic HVQFN	–40 °C to +85 °C	PCA9534BS	9534	SOT629-1

Standard packing quantities and other packing data are available at www.standardproducts.philips.com/packaging.

PIN CONFIGURATION — SO, TSSOP

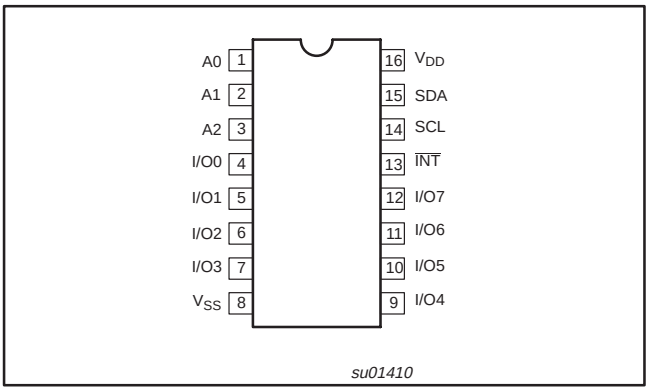


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION — HVQFN

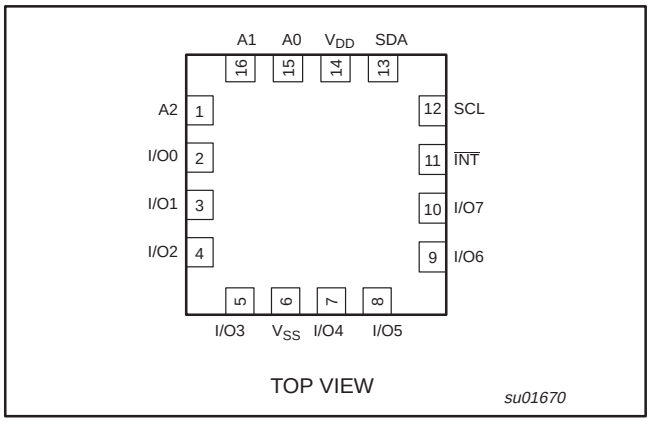


Figure 2. Pin Configuration — HVQFN

PIN DESCRIPTION

PIN NUMBER		SYMBOL	FUNCTION
SO, TSSOP	HVQFN		
1	15	A0	Address input 0
2	16	A1	Address input 1
3	1	A2	Address input 2
4–7	2–5	I/O0 to I/O3	I/O0 to I/O3
8	6	V_{SS}	Supply ground
9–12	7–10	I/O4 to I/O7	I/O4 to I/O7
13	11	$\overline{INT}$	Interrupt output (open drain)
14	12	SCL	Serial clock line
15	13	SDA	Serial data line
16	14	V_{DD}	Supply voltage

BLOCK DIAGRAM

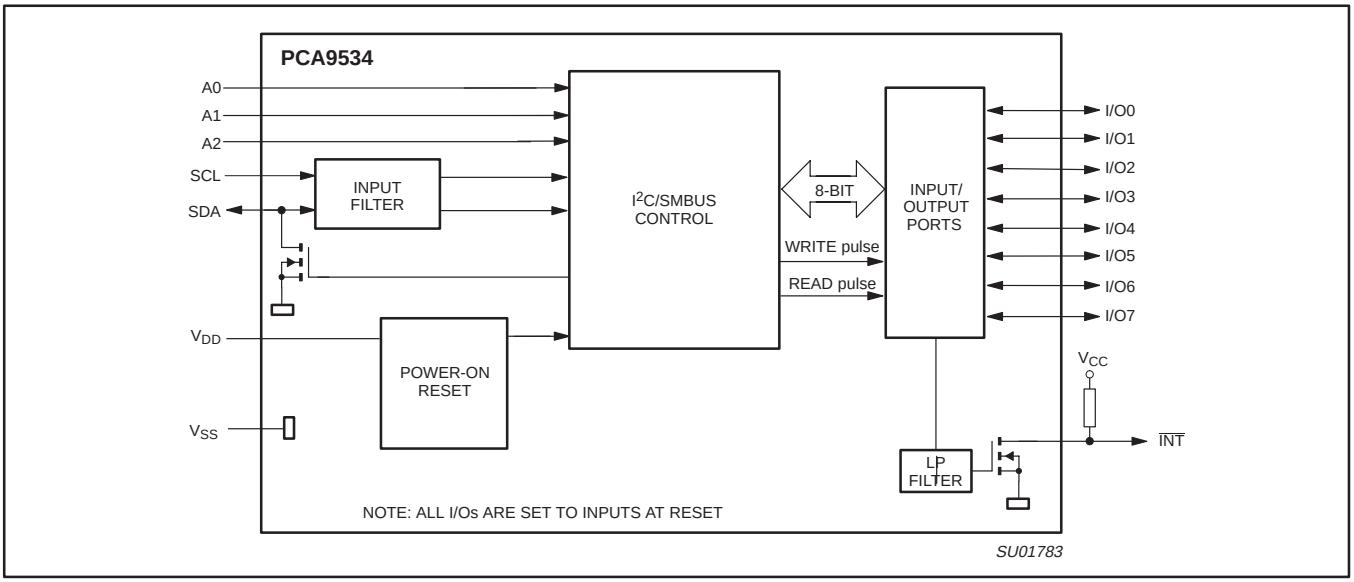


Figure 3. Block diagram

REGISTERS

Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0 – Input Port Register

bit	I7	I6	I5	I4	I3	I2	I1	I0
default	X	X	X	X	X	X	X	X

This register is a read only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value ‘X’ is determined by the externally applied logic level.

Register 1 – Output Port Register

bit	O7	O6	O5	O4	O3	O2	O1	O0
default	1	1	1	1	1	1	1	1

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Register 2 – Polarity Inversion Register

bit	N7	N6	N5	N4	N3	N2	N1	N0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port Register data. If a bit in this register is set (written with ‘1’), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a ‘0’), the Input Port data polarity is retained.

Register 3 – Configuration Register

bit	C7	C6	C5	C4	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

Power-on Reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9534 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9534 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

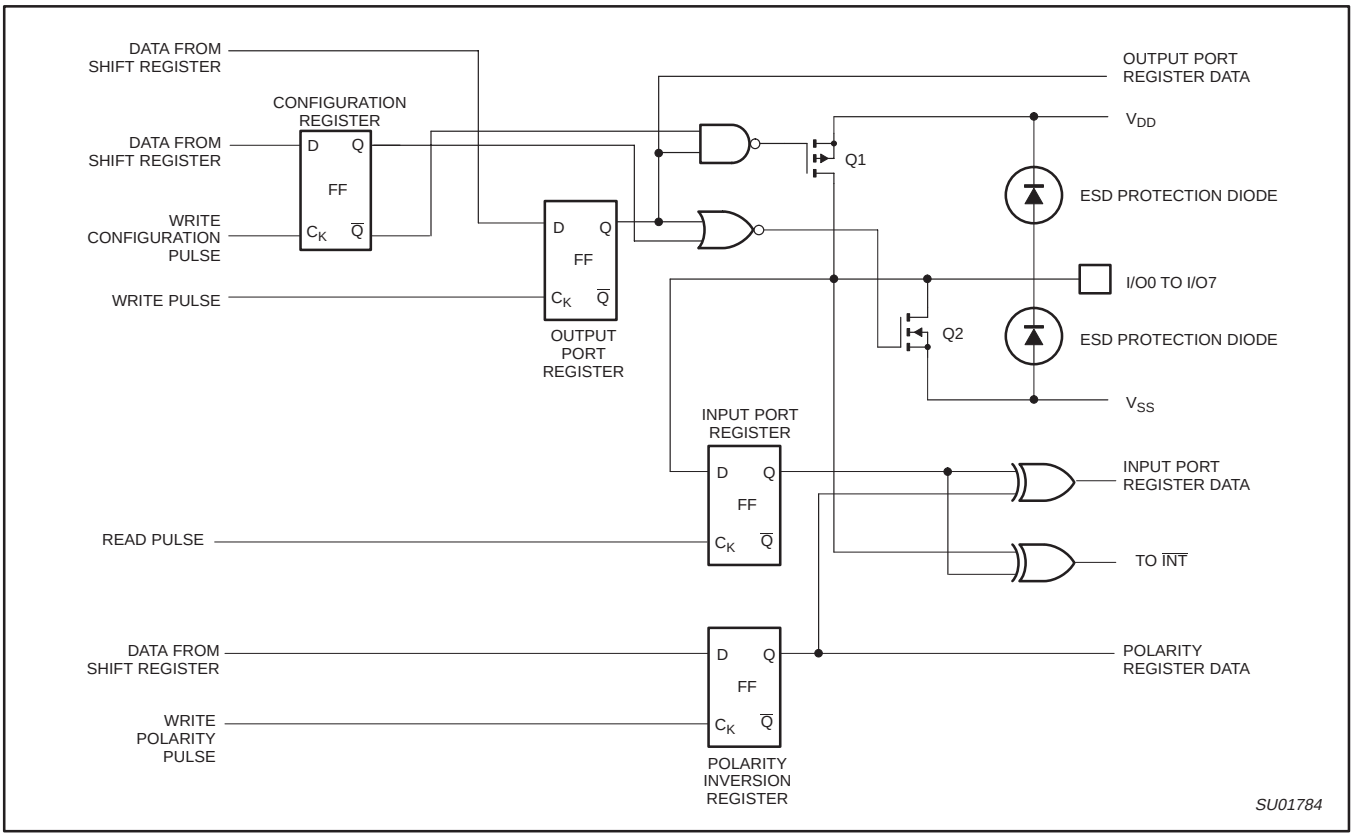
For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

Interrupt Output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

SIMPLIFIED SCHEMATIC OF I/O0 TO I/O7



NOTE: At Power-on Reset, all registers return to default values.

Figure 4. Simplified schematic of I/O0 to I/O7

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance paths that exist between the pin and either V_{DD} or V_{SS}.

Device address

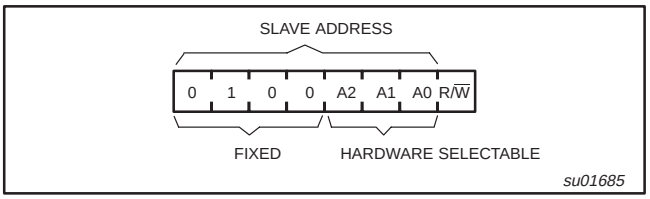


Figure 5. PCA9534 address

Bus transactions

Data is transmitted to the PCA9534 registers using the write mode as shown in Figures 6 and 7. Data is read from the PCA9534 registers using the read mode as shown in Figures 8 and 9. These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

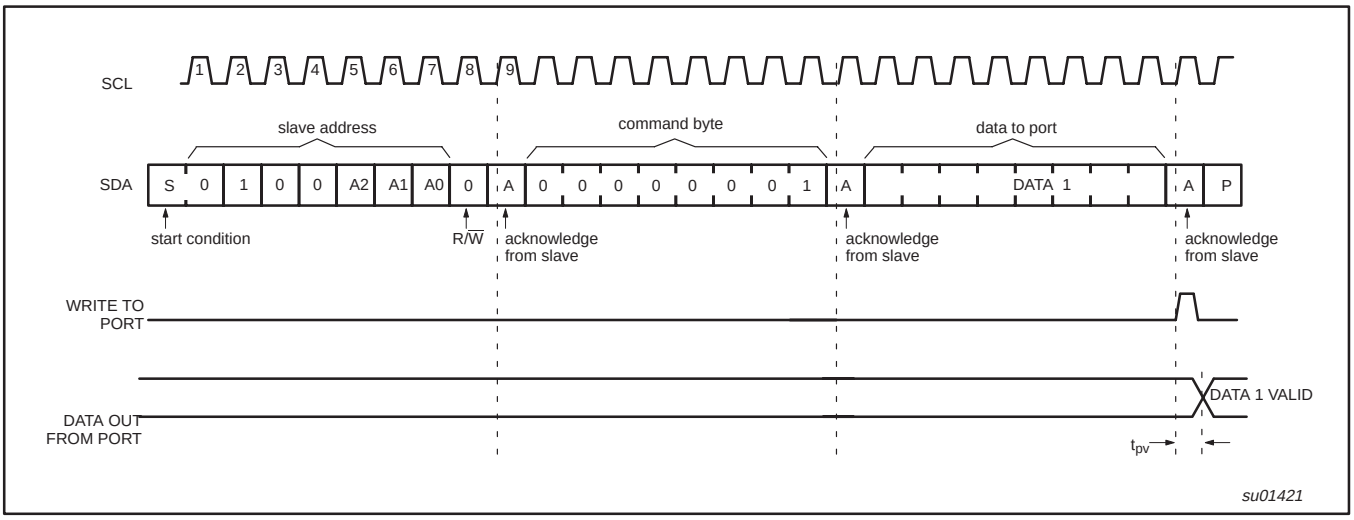


Figure 6. WRITE to output port register

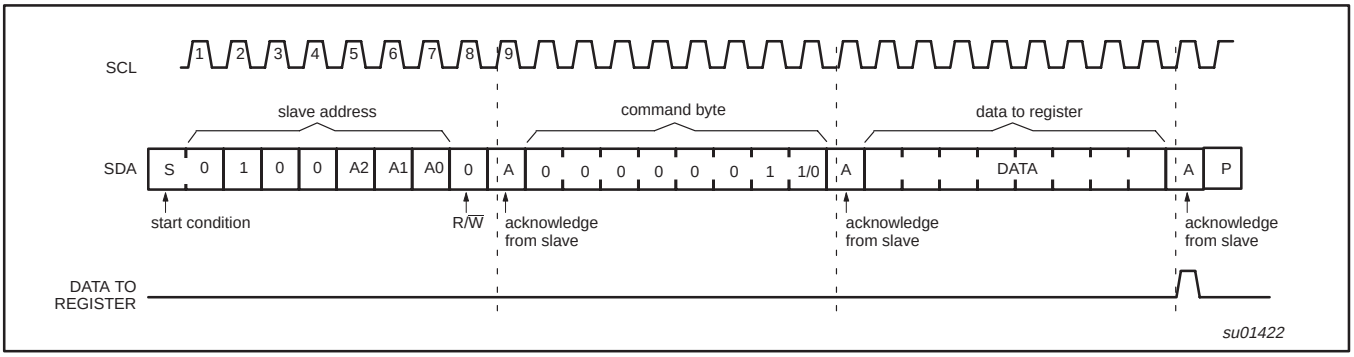


Figure 7. WRITE to configuration or polarity inversion registers

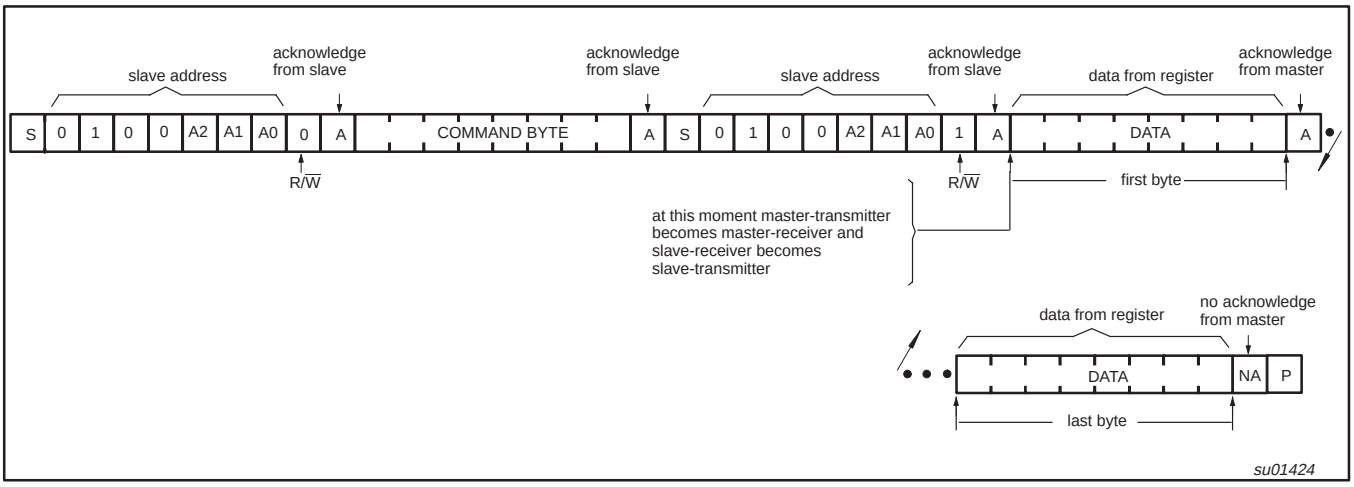
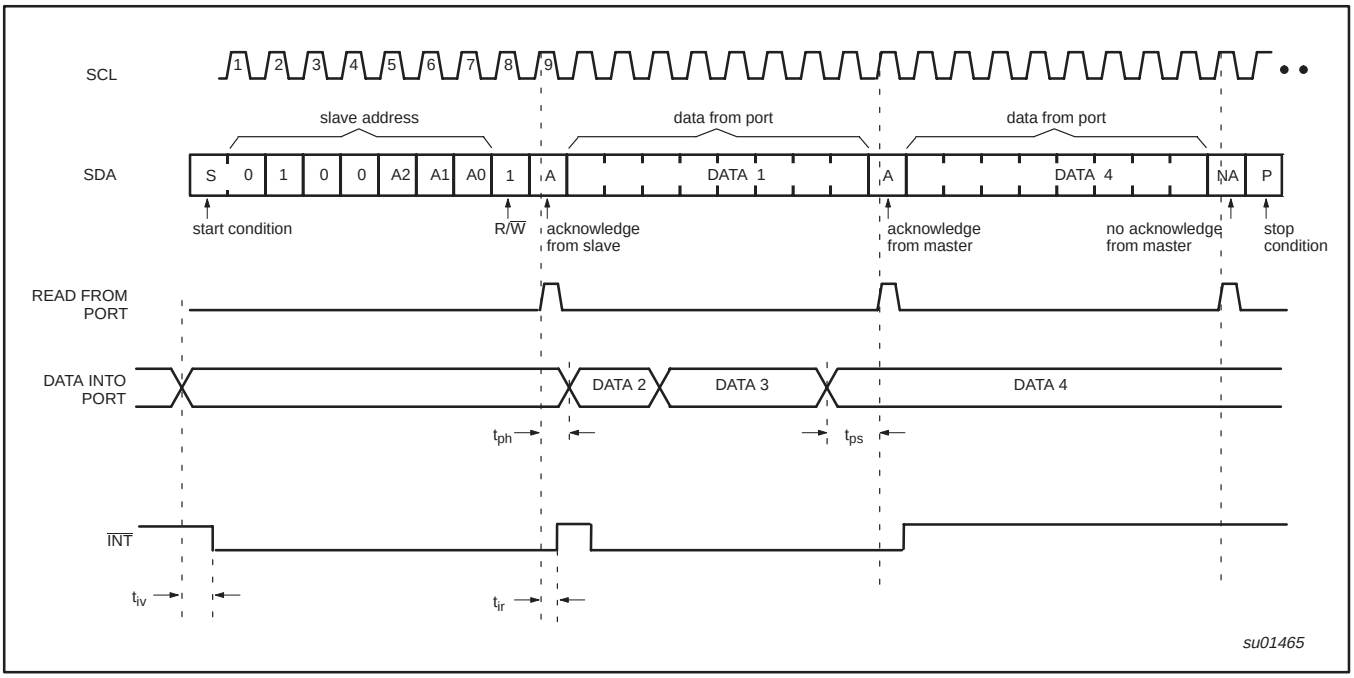


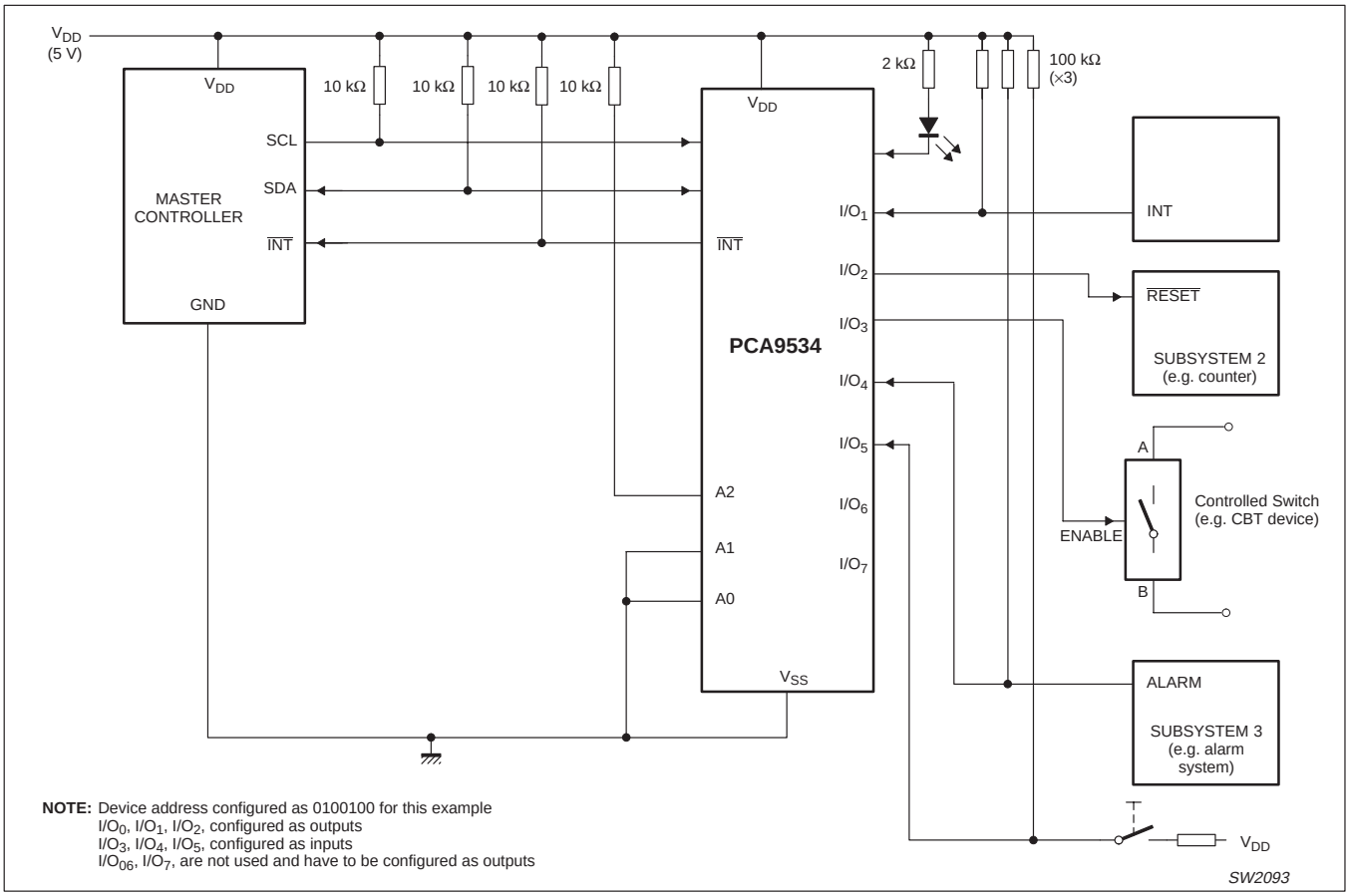
Figure 8. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition.

Figure 9. READ input port register

TYPICAL APPLICATION



NOTE: Device address configured as 0100100 for this example
I/O_0, I/O_1, I/O_2, configured as outputs
I/O_3, I/O_4, I/O_5, configured as inputs
I/O_{06}, I/O_7, are not used and have to be configured as outputs

Figure 10. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 10. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 11 shows a high value resistor in parallel with the LED. Figure 12 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

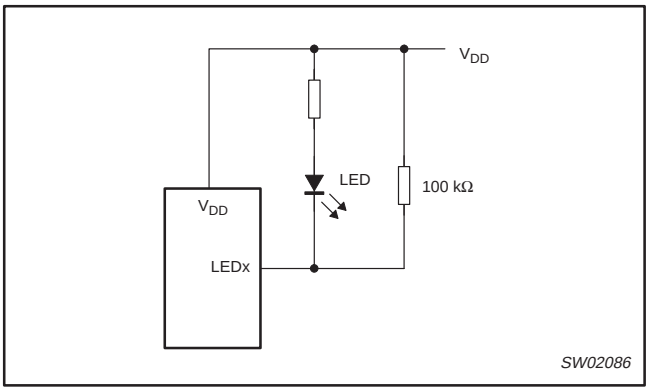


Figure 11. High value resistor in parallel with the LED

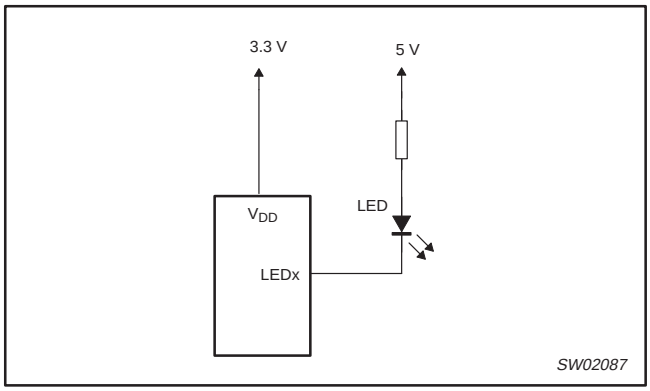


Figure 12. Device supplied by a lower voltage

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
I_I	DC input current		—	±20	mA
$V_{I/O}$	DC voltage on an I/O		V_{SS} – 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±50	mA
I_{DD}	Supply current		—	85	mA
I_{SS}	Supply current		—	100	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz	—	104	175	µA
I_{stbl}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
I_{stbh}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
V_{POR}	Power-on reset voltage (Note 1)	No load; $V_I = V_{DD}$ or V_{SS}	—	1.5	1.65	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	5	10	pF
I/Os						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V; Note 2	8	10	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 2	10	13	—	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V; Note 2	8	17	—	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V; Note 2	10	24	—	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V; Note 2	8	14	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 2	10	19	—	mA
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA; V_{DD} = 2.3 V; Note 3	1.8	—	—	V
		I_{OH} = –10 mA; V_{DD} = 2.3 V; Note 3	1.7	—	—	V
		I_{OH} = –8 mA; V_{DD} = 3.0 V; Note 3	2.6	—	—	V
		I_{OH} = –10 mA; V_{DD} = 3.0 V; Note 3	2.5	—	—	V
		I_{OH} = –8 mA; V_{DD} = 4.5 V; Note 3	4.1	—	—	V
		I_{OH} = –10 mA; V_{DD} = 4.5 V; Note 3	4.0	—	—	V
I_{IL}	Input leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	1	µA
C_I	Input capacitance		—	5	10	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
Select Inputs A0, A1, A2						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		–1	—	1	µA

NOTES:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.
3. The total current sourced by all I/Os must be limited to 85 mA.

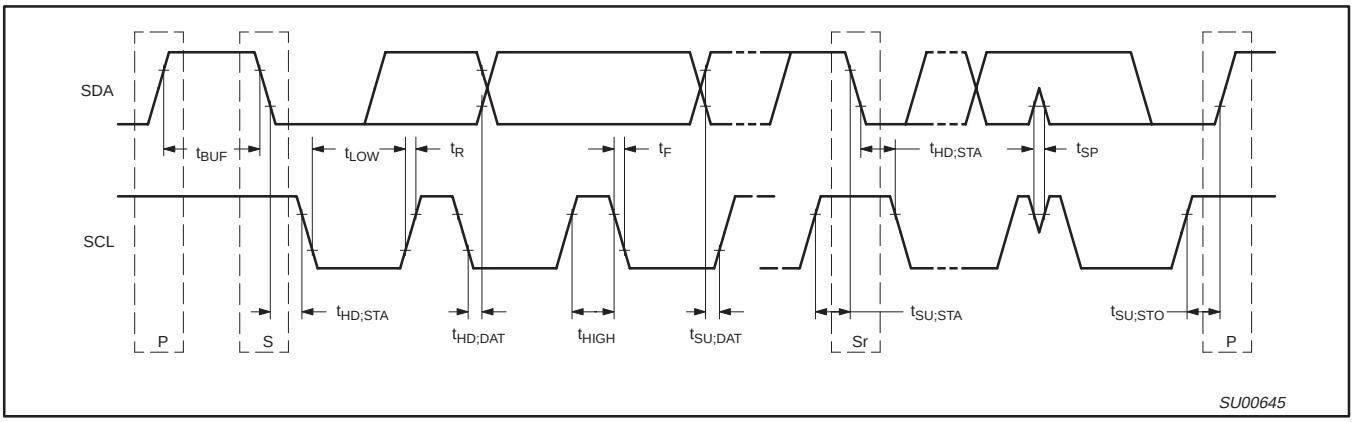


Figure 13. Definition of timing

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C-bus		FAST MODE I²C-bus		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	Data out valid time[3]	300	—	50	—	ns
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data setup time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Interrupt Timing						
t_{IV}	Interrupt valid	—	4	—	4	µs
t_{IR}	Interrupt reset	—	4	—	4	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

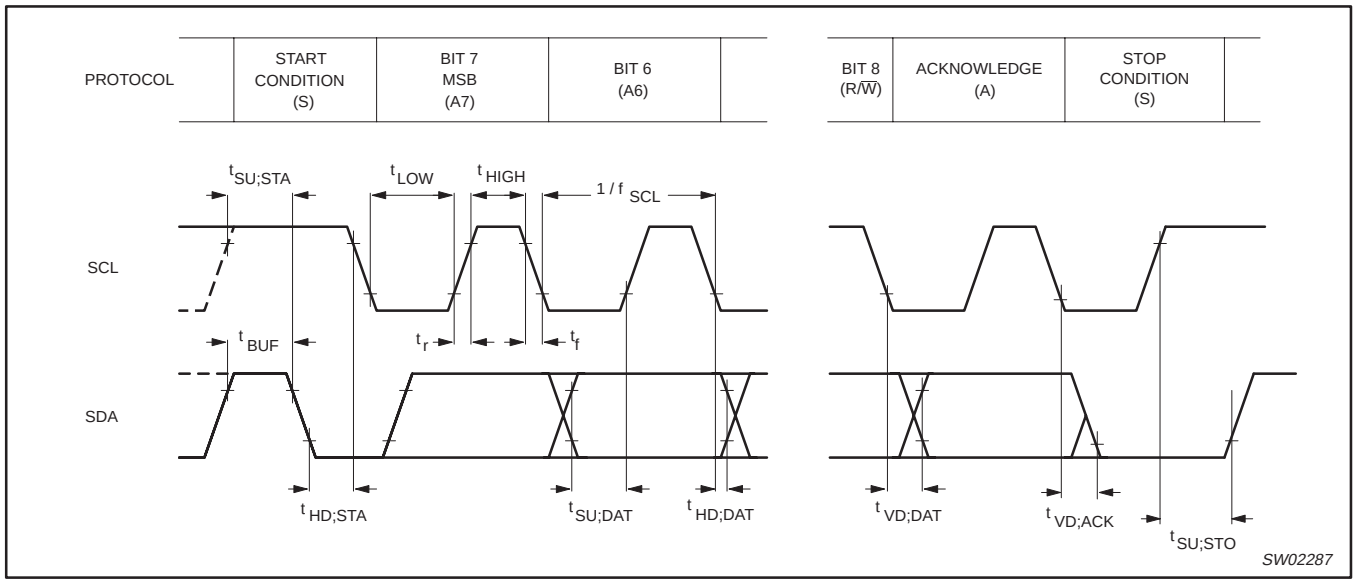
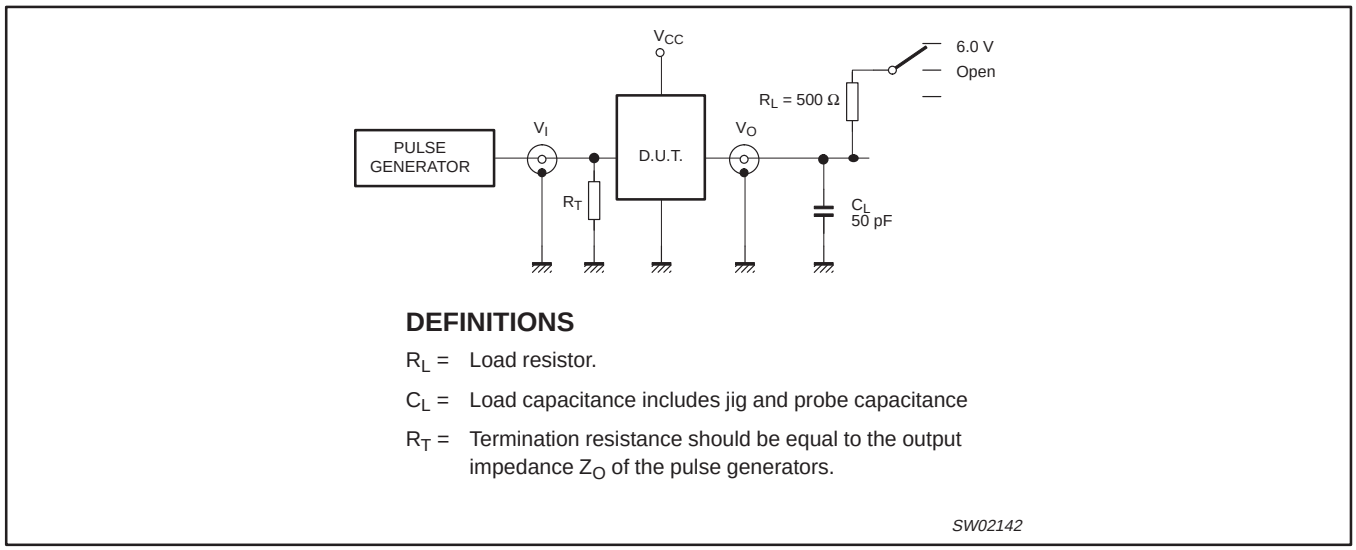


Figure 14. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}



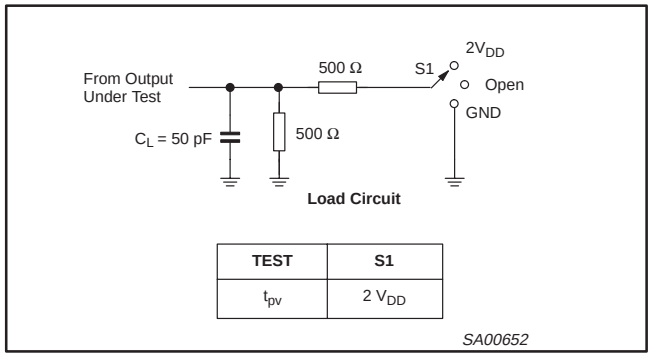
DEFINITIONS

R_L = Load resistor.

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

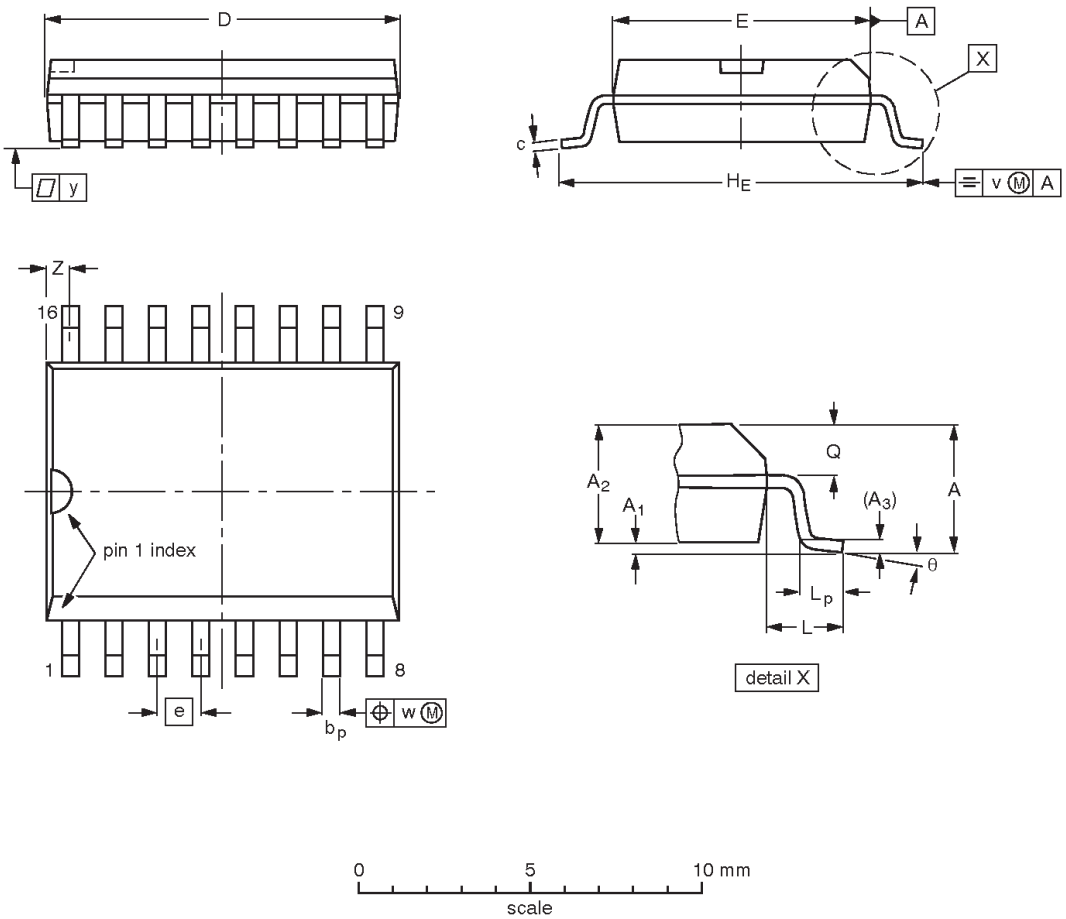
Figure 15. Test circuitry for switching times



TEST	S1
t_{pv}	2 V_{DD}

Figure 16. Test circuit

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

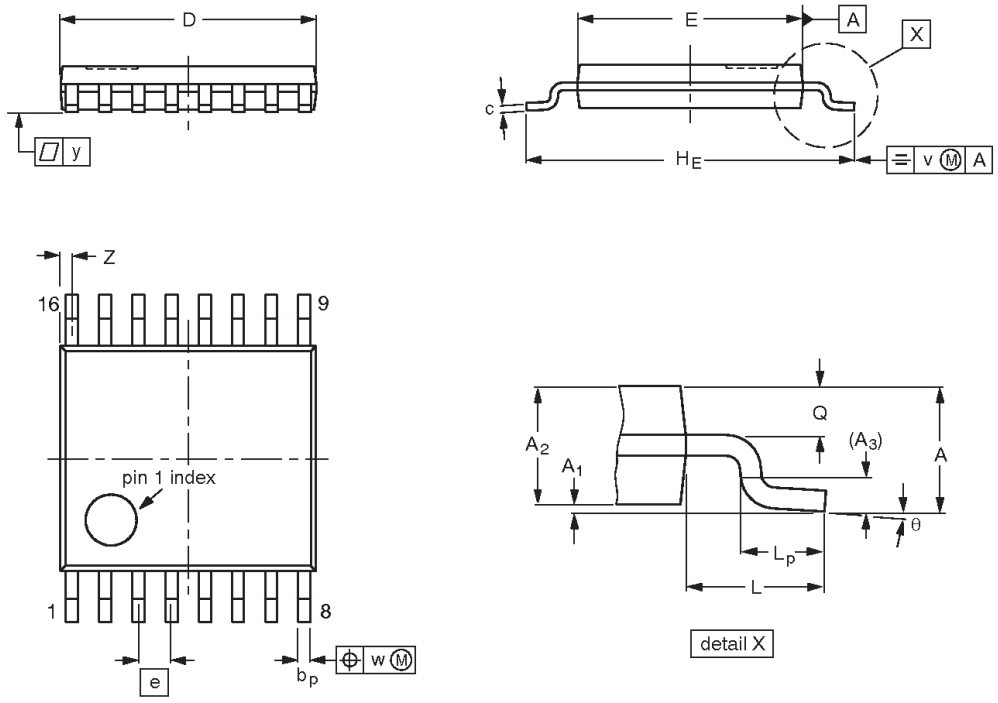
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

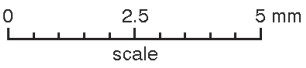
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

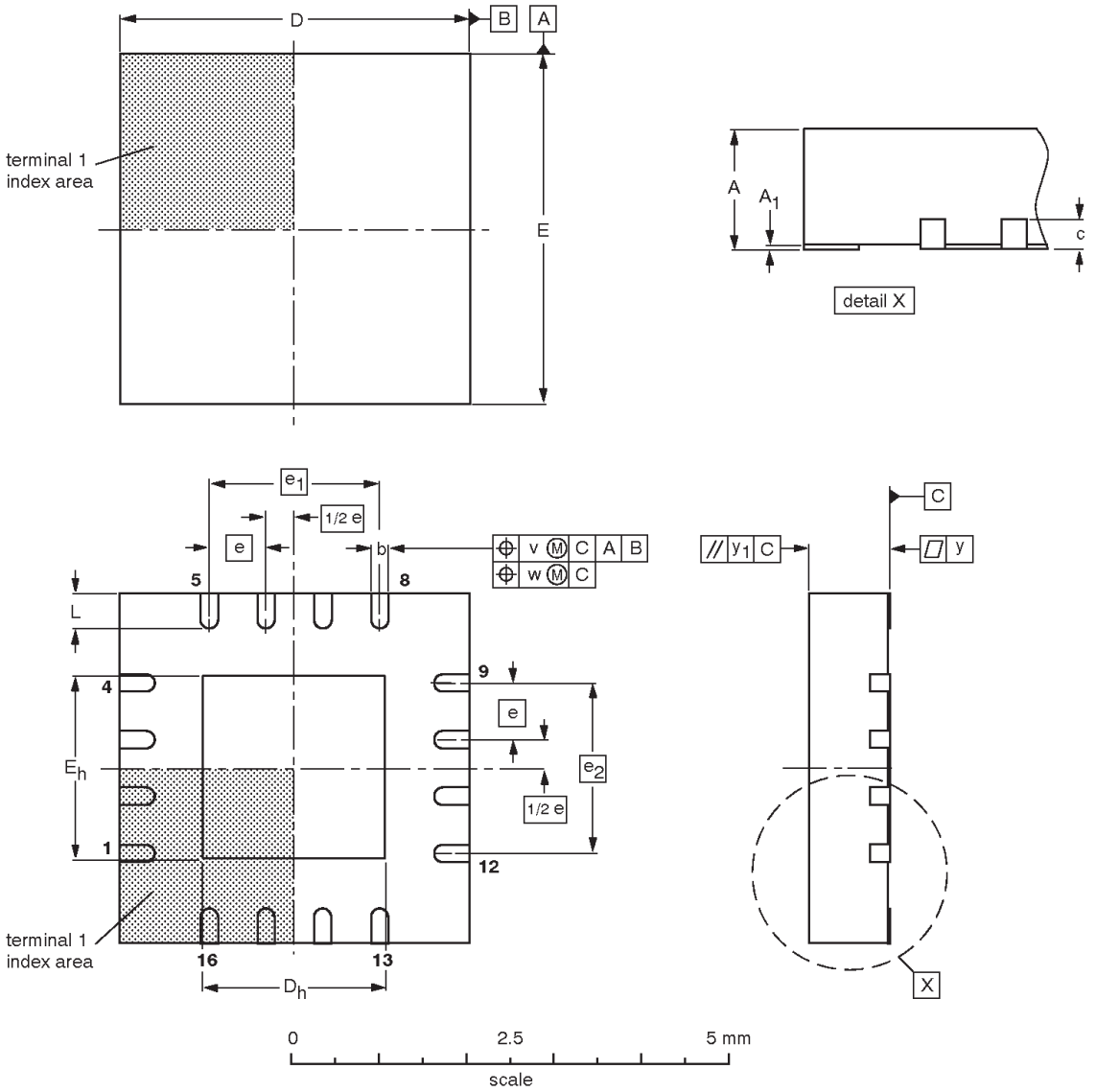
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 x 4 x 0.85 mm **SOT629-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.38 0.23	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.65	1.95	1.95	0.75 0.50	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT629-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_2	20040930	**Product data sheet (9397 750 13506); Supersedes data of 02 December 2003 (9397 750 12454).** Modifications: ● “Register 0—Input Port Register” section on page 4: add second paragraph. ● Section “Power-on reset” on page 4 re-written. ● Figure 10: resistor values modified ● (New) Note 1 added to DC Characteristics table on page 10. ● “DC Characteristics” table: Note 2 re-written.
_1	20031202	**Product data (9397 750 12454); ECN 853-2319 01-A14517 dated 14 November 2003.**

8-bit I²C and SMBus low power I/O port with interrupt PCA9534

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 09-04

Document number: 9397 750 13506

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