



UC1637
UC2637
UC3637

Switched Mode Controller for DC Motor Drive

FEATURES

- Single or Dual Supply Operation
- $\pm 2.5V$ to $\pm 20V$ Input Supply Range
- $\pm 5\%$ Initial Oscillator Accuracy; $\pm 10\%$ Over Temperature
- Pulse-by-Pulse Current Limiting
- Under-Voltage Lockout
- Shutdown Input with Temperature Compensated 2.5V Threshold
- Uncommitted PWM Comparators for Design Flexibility
- Dual 100mA, Source/Sink Output Drivers

DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with $\pm 100mA$ output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

The UC1637 is characterized for operation over the full military temperature range of $-55^{\circ}C$ to $+125^{\circ}C$, while the UC2637 and UC3637 are characterized for $-25^{\circ}C$ to $+85^{\circ}C$ and $0^{\circ}C$ to $+70^{\circ}C$, respectively.

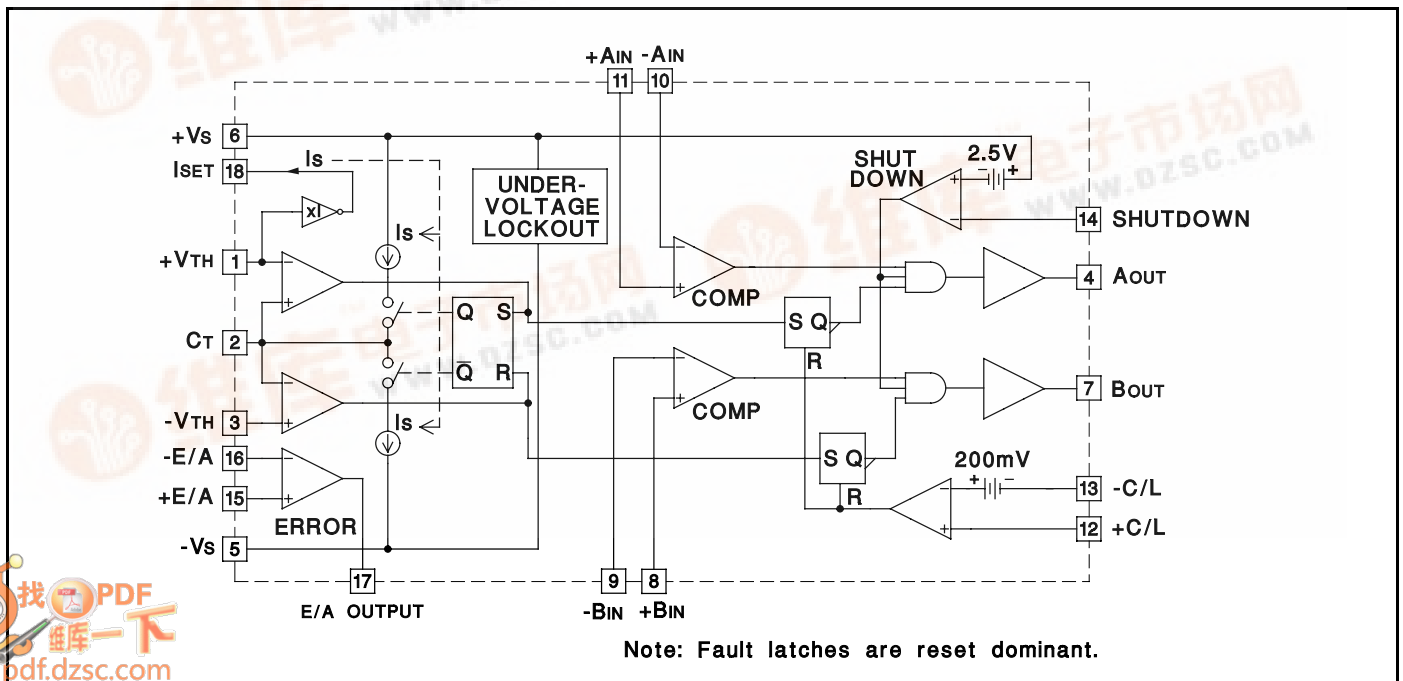
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($\pm V_s$)	$\pm 20V$
Output Current, Source/Sink (Pins 4, 7)	500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15, 16)	$\pm V_s$
Error Amplifier Output Current (Pin 17)	$\pm 20mA$
Oscillator Charging Current (Pin 18)	-2mA
Power Dissipation at $T_A = 25^{\circ}C$ (Note 2)	1000mW
Power Dissipation at $T_C = 25^{\circ}C$ (Note 2)	2000mW
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 10 Seconds)	$+300^{\circ}C$

Note 1: Currents are positive into, negative out of the specified terminal.

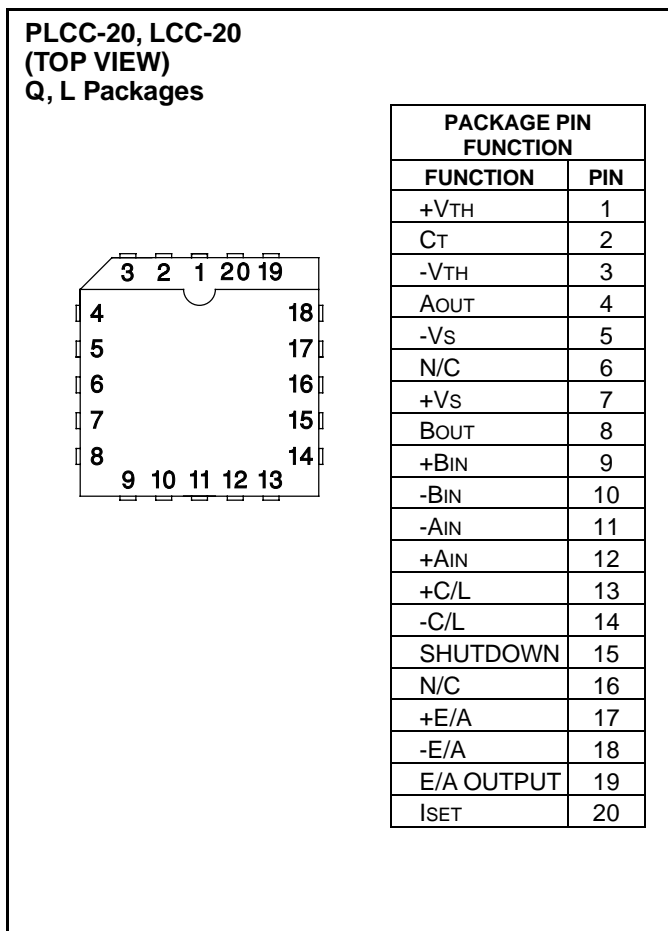
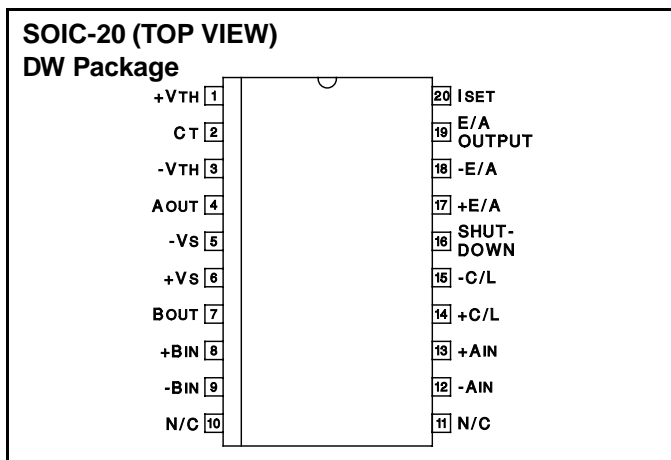
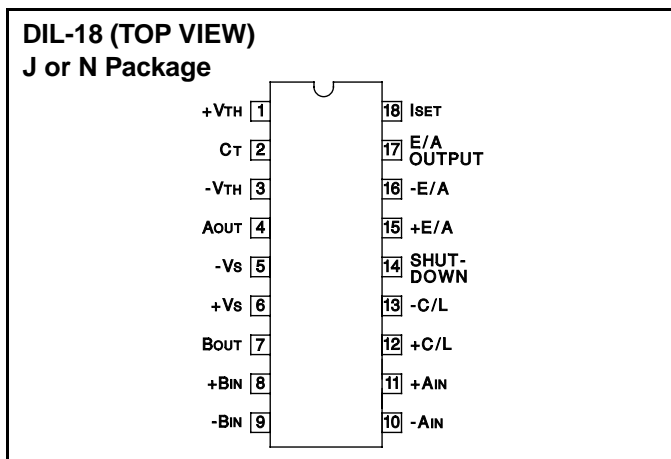
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM



Note: Fault latches are reset dominant.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the UC1637; -25°C to $+85^\circ\text{C}$ for the UC2637; and 0°C to $+70^\circ\text{C}$ for the UC3637; $+V_S = +15\text{V}$, $-V_S = -15\text{V}$, $+V_{TH} = 5\text{V}$, $-V_{TH} = -5\text{V}$, $R_T = 16.7\text{k}\Omega$, $C_T = 1500\text{pF}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	$T_J = 25^\circ\text{C}$ (Note 6)	9.4	10	10.6	9	10	11	kHz
Voltage Stability	$V_S = \pm 5\text{V}$ to $\pm 20\text{V}$, $V_{PIN 1} = 3\text{V}$, $V_{PIN 3} = -3\text{V}$		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
+V _{TH} Input Bias Current	$V_{PIN 2} = 6\text{V}$	-10	0.1	10	-10	0.1	10	μA
-V _{TH} Input Bias Current	$V_{PIN 2} = 0\text{V}$	-10	-0.5		-10	-0.5		μA
+V _{TH} , -V _{TH} Input Range		$+V_S - 2$		$-V_S + 2$	$+V_S - 2$		$-V_S + 2$	V
Error Amplifier								
Input Offset Voltage	$V_{CM} = 0\text{V}$		1.5	5		1.5	10	mV
Input Bias Current	$V_{CM} = 0\text{V}$		0.5	5		0.5	5	μA
Input Offset Current	$V_{CM} = 0\text{V}$		0.1	1		0.1	1	μA
Common Mode Range	$V_S = \pm 2.5$ to 20V	$-V_S + 2$		$+V_S$	$-V_S + 2$		$+V_S$	V
Open Loop Voltage Gain	$R_L = 10\text{k}$	75	100		80	100		dB
Slew Rate			15			15		V/ μs
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	$V_S = \pm 2.5$ to $\pm 20\text{V}$	75	110		75	110		dB

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PARAMETERS	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier (Continued)								
Output Sink Current	$V_{PIN\ 17} = 0\text{V}$		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17} = 0\text{V}$	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	$V_{CM} = 0\text{V}$		20			20		mV
Input Bias Current	$V_{CM} = 0\text{V}$		2	10		2	10	μA
Input Hysteresis	$V_{CM} = 0\text{V}$		10			10		mV
Common Mode range	$V_S = \pm 5\text{V}$ to $\pm 20\text{V}$	$-V_S + 1$		$+V_S - 2$	$-V_S + 1$		$+V_S - 2$	V
Current Limit								
Input Offset Voltage	$V_{CM} = 0\text{V}$, $T_J = 25^{\circ}\text{C}$	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/ $^{\circ}\text{C}$
Input Bias Current		-10	-1.5		-10	-1.5		μA
Common Mode Range	$V_S = \pm 2.5\text{V}$ to $\pm 20\text{V}$	$-V_S$		$+V_S - 3$	$-V_S$		$+V_S - 3$	V
Shutdown								
Shutdown Threshold	(Note 4)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14} = +V_S$ to $-V_S$	-10	-0.5		-10	-0.5		μA
Under-Voltage Lockout								
Start Threshold	(Note 5)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	$I_{SINK} = 20\text{mA}$		-14.9	-13		-14.9	-13	V
	$I_{SINK} = 100\text{mA}$		-14.5	-13		-14.5	-13	
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 100\text{mA}$	12	13.5		12	13.5		
Rise Time	(Note 3) $C_L = \text{Inf}$, $T_J = 25^{\circ}\text{C}$		100	600		100	600	ns
Fall Time	(Note 3) $C_L = \text{Inf}$, $T_J = 25^{\circ}\text{C}$		100	300		100	300	ns

Note 3: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 4: Parameter measured with respect to $+V_S$ (Pin 6).

Note 5: Parameter measured at $+V_S$ (Pin 6) with respect to $-V_S$ (Pin 5).

Note 6: R_T and C_T referenced to Ground.

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, ISET and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ ter-

minal voltage is buffered internally and also applied to the ISET terminal to develop the capacitor charging current through R_T . If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

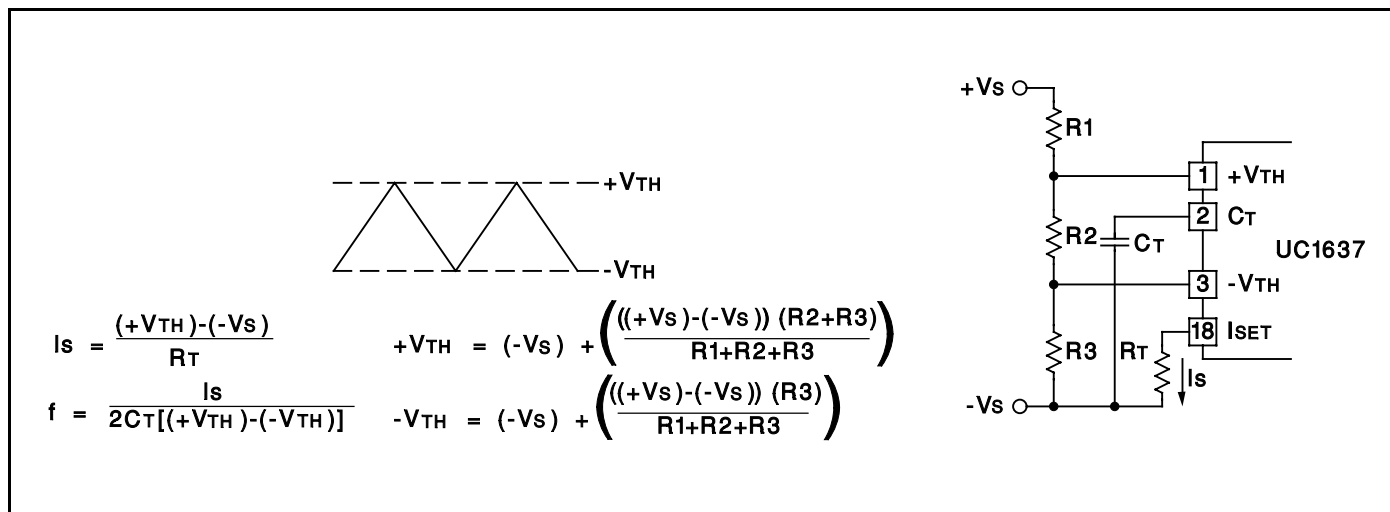


Figure 1. Oscillator Setup

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

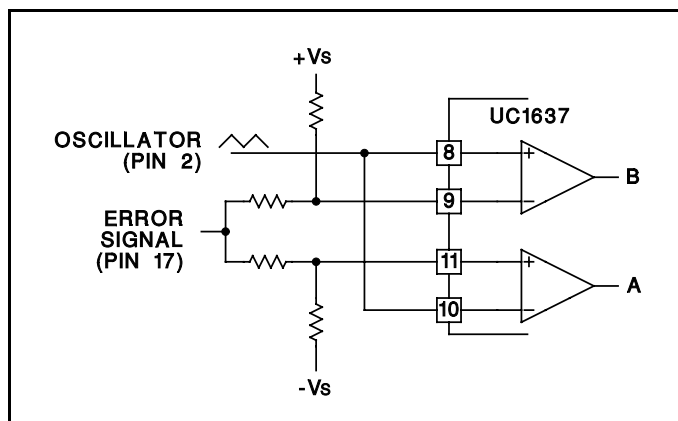


Figure 2. Comparator Biasing

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)

In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)

A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode

(Voltage on Pin 9 > Pin 11)

With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically $-V_s + 0.2V$ @50mA low level and $+V_s - 2.0V$ @50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate ($15V/\mu s$) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the $\pm V_s$ supply voltage, the common mode input range and the voltage output swing is within 2V of the V_s supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

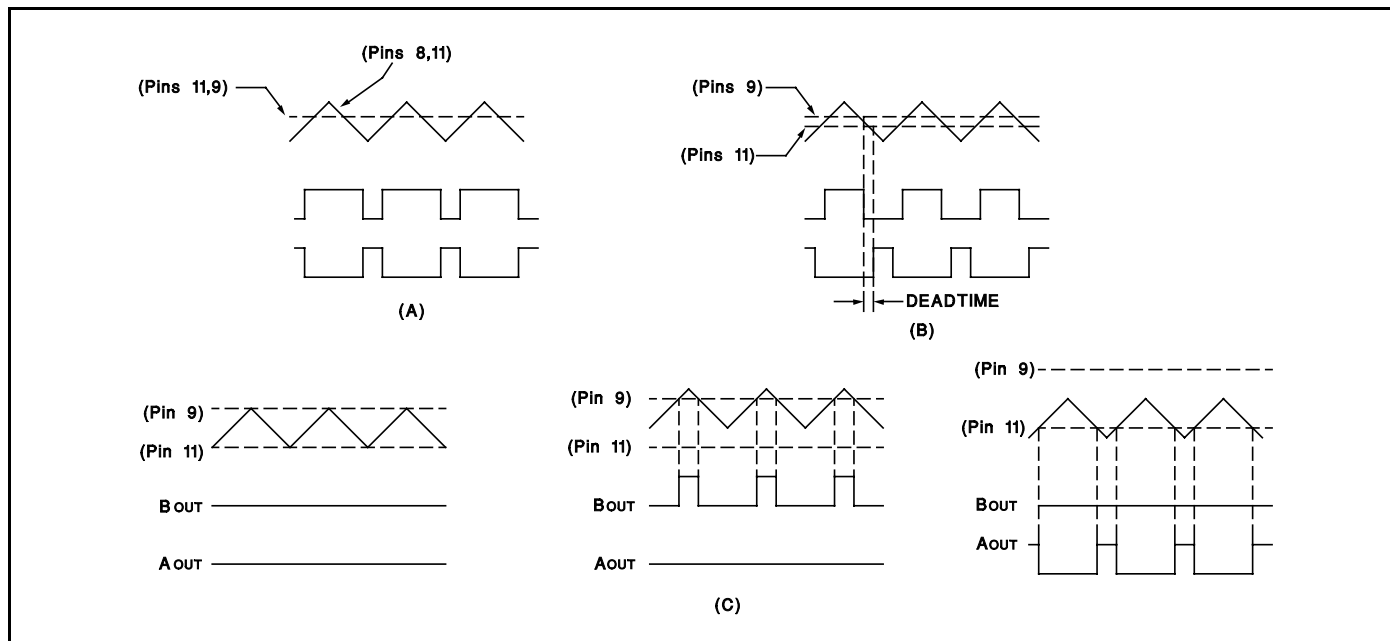


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below V_{IN} , the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

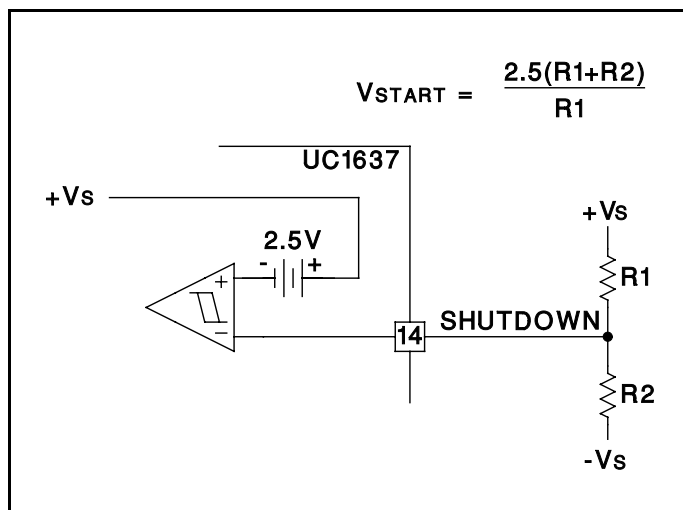


Figure 4. External Under-Voltage Lockout

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from

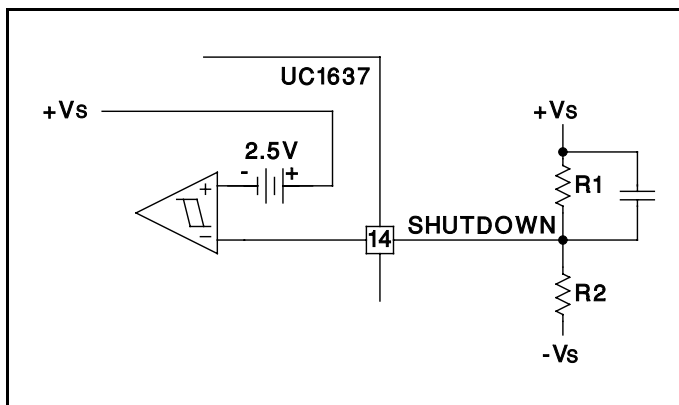


Figure 5. Delayed Start-Up

$-V_s$ to within 3V of the $+V_s$ supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

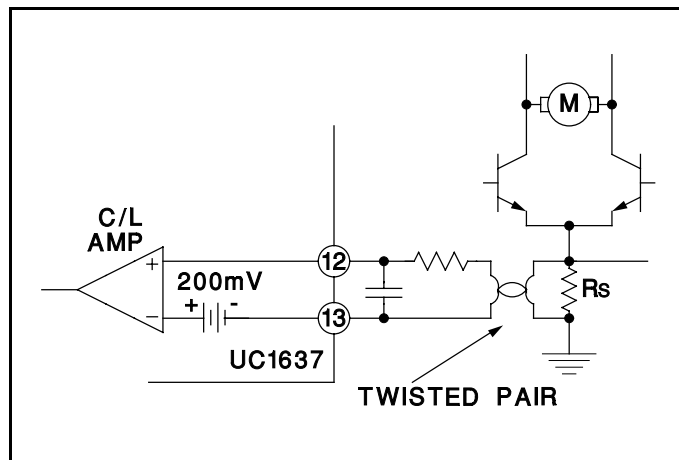


Figure 6. Current Limit Sensing

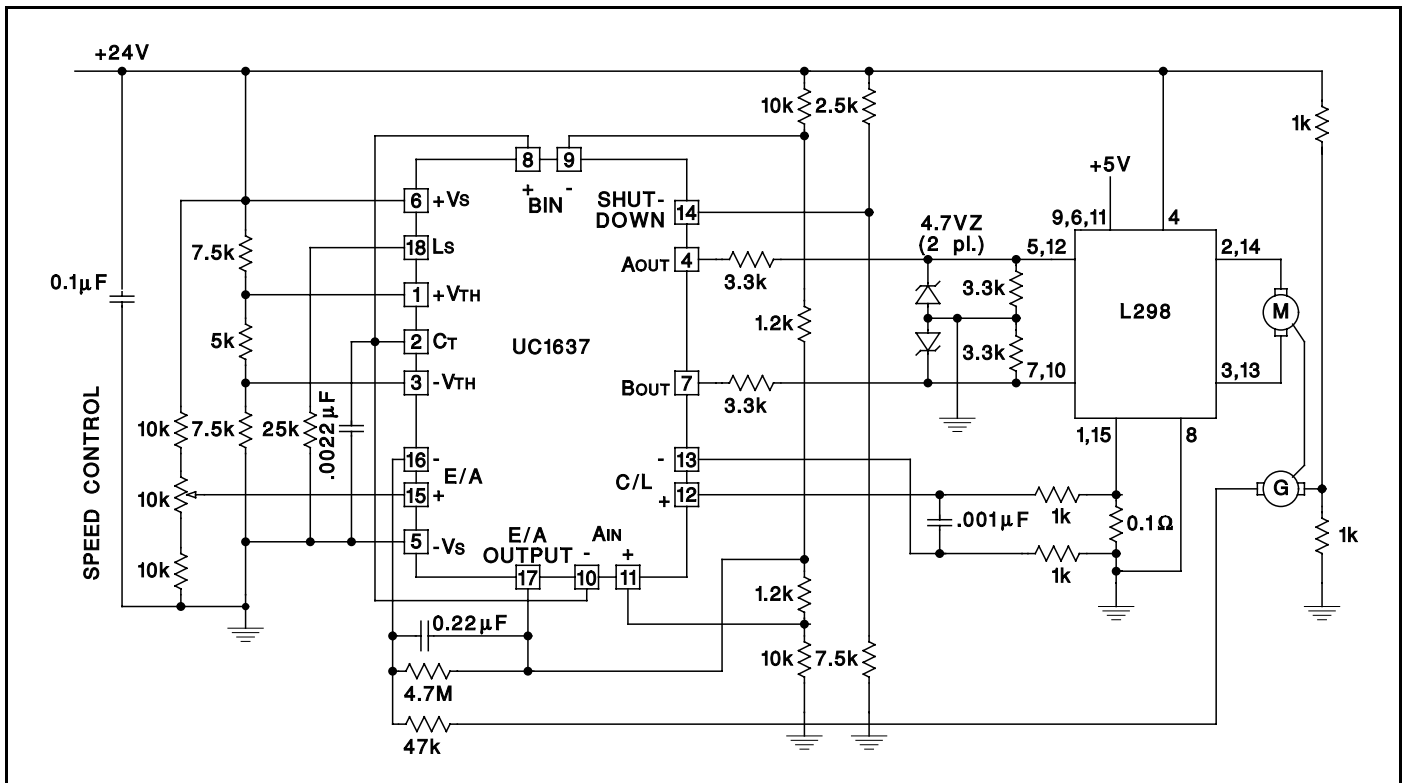


Figure 7. Bi-Directional Motor Drive with Speed Control Power-Amplifier

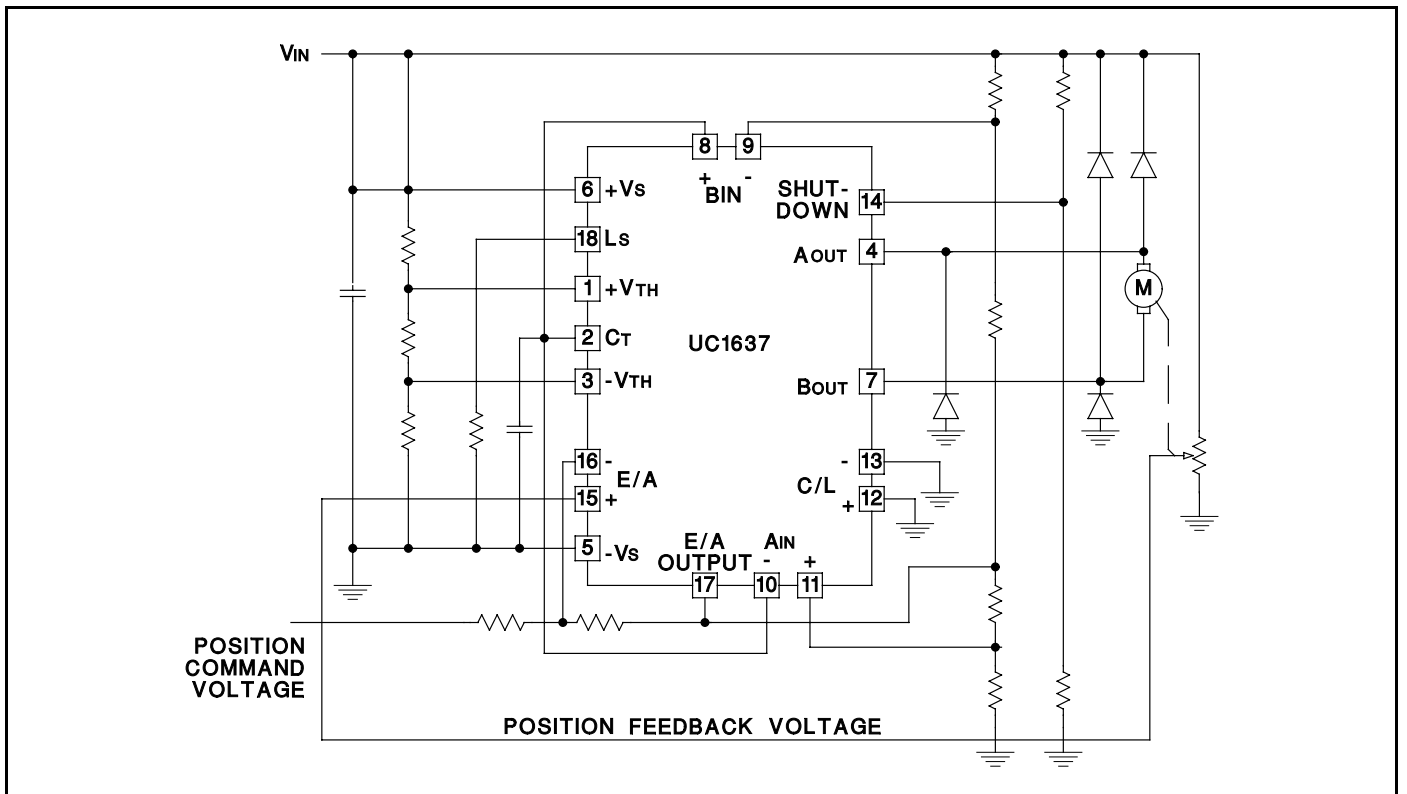


Figure 8. Single Supply Position Servo Motor Drive

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-89957012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-8995701VA	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1637J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1637J883B	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1637L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1637L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC2637DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2637DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2637DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2637J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC2637N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC2637NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC2637Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2637QTR	ACTIVE	PLCC	FN	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3637DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3637DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3637DWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3637J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3637N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3637NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3637Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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