ANALOG DEVICES

192 kHz Stereo Asynchronous Sample Rate Converter

AD1895*

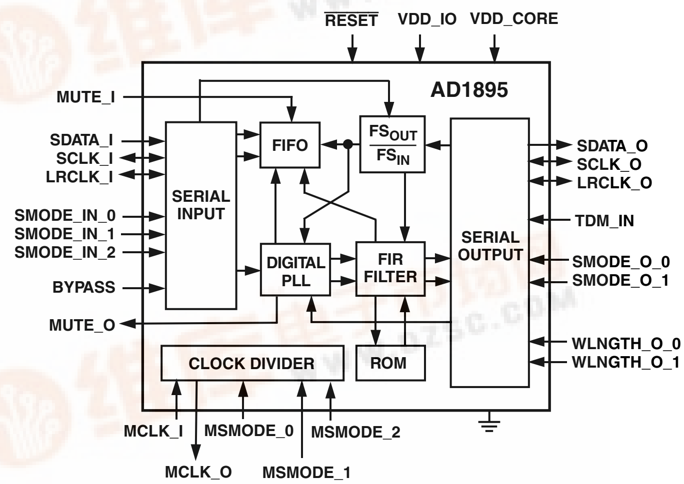
FEATURES

- Automatically Senses Sample Frequencies
- No Programming Required
- Attenuates Sample Clock Jitter
- 3.3 V–5 V Input and 3.3 V Core Supply Voltages
- Accepts 16-/18-/20-/24-Bit Data
- Up to 192 kHz Sample Rate
- Input/Output Sample Ratios from 7.75:1 to 1:8
- Bypass Mode
- Multiple AD1895 TDM Daisy-Chain Mode
- 128 dB Signal-to-Noise and Dynamic Range (A-Weighted, 20 Hz–20 kHz BW)
- Up to –122 dB THD + N
- Linear Phase FIR Filter
- Hardware Controllable Soft Mute
- Supports 256 × f_S, 512 × f_S or 768 × f_S Master Mode Clock
- Flexible Three-Wire Serial Data Port with Left-Justified, I^{2}S, Right-Justified (16-, 18-, 20-, 24-Bits), and TDM Serial Port Modes
- Master/Slave Input and Output Modes
- 28-Lead SSOP Plastic Package

APPLICATIONS

Home Theater Systems, Automotive Audio Systems, DVD, DVD-R, CD-R, Set-Top Boxes, Digital Audio Effects Processors

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The AD1895 is a 24-bit, high-performance, single-chip, second-generation asynchronous sample rate converter. Based upon Analog Devices, Inc. experience with its first asynchronous sample rate converter, the AD1890, the AD1895 offers improved performance and additional features. This improved performance includes a THD + N range of –115 dB to –122 dB depending on sample rate and input frequency, 128 dB (A-Weighted) dynamic range, 192 kHz sampling frequencies for both input and output sample rates, improved jitter rejection, and 1:8 upsampling and 7.75:1 downsampling ratios. Additional features include more serial formats, a bypass mode, and better interfacing to digital signal processors.

The AD1895 has a 3-wire interface for the serial input and output ports that supports left-justified, I^{2}S, and right-justified (16-, 18-, 20-, 24-bit) modes. Additionally, the serial output port supports TDM mode for daisy chaining multiple AD1895s to a digital signal processor. The serial output data is dithered down to 20, 18 or 16 bits when 20-, 18- or 16-bit output data is selected. The AD1895 sample rate converts the data from the serial input port to the sample rate of the serial output port. The sample rate at the serial input port can be asynchronous with respect to the output sample rate of the output serial port. The master clock to the AD1895, MCLK, can be asynchronous to both the serial input and output ports.

MCLK can either be generated off-chip or on-chip by the AD1895 master clock oscillator. Since MCLK can be asynchronous to the input or output serial ports, a crystal can be used to generate MCLK internally to reduce noise and EMI emissions on the board. When MCLK is synchronous to either the output or input serial port, the AD1895 can be configured in a master mode where MCLK is divided down and used to generate the left/right and bit clocks for the serial port that is synchronous to MCLK. The AD1895 supports master modes of 256 × f_S, 512 × f_S, and 768 × f_S for both input and output serial ports.

Conceptually, the AD1895 interpolates the serial input data by a rate of 2^{20} and samples the interpolated data stream by the output sample rate. In practice, a 64-tap FIR filter with 2^{20} polyphases, a FIFO, a digital servo loop that measures the time difference between input and output samples within 5 ps, and a digital circuit to track the sample rate ratio are used to perform the interpolation and output sampling. Refer to the Theory of Operation section. The digital servo loop and sample rate ratio circuit automatically track the input and output sample rates.

(Continued on page 15)

*Patents pending.

REV. A

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AD1895–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	
VDD_CORE	3.3 V
VDD_IO	5.0 V or 3.3 V
Ambient Temperature	25°C
Input Clock	30.0 MHz
Input Signal	1.000 kHz, 0 dBFS
Measurement Bandwidth	20 to $f_{S\_OUT}/2$ Hz
Word Width	24 Bits
Load Capacitance	50 pF
Input Voltage HI	2.4 V
Input Voltage LO	0.8 V

Specifications subject to change without notice.

DIGITAL PERFORMANCE (VDD_CORE = 3.3 V ± 5%, VDD_IO = 5.0 V ± 10%)

Parameter	Min	Typ	Max	Unit
Resolution		24		Bits
Sample Rate @ MCLK_I = 30 MHz	6		215	kHz
Sample Rate (@ Other Master Clocks)[1]	MCLK_I/5000 ≤ f_{S_OUT} ≤ MCLK_I/138			kHz
Sample Rate Ratios				
Upsampling			1:8	
Downsampling			7.75:1	
Dynamic Range[2]				
(20 Hz to $f_{S\_OUT}/2$, 1 kHz, –60 dBFS Input) A-Weighted				
44.1 kHz: 48 kHz		128		dB
48 kHz: 44.1 kHz		128		dB
48 kHz: 96 kHz		128		dB
44.1 kHz: 192 kHz		128		dB
96 kHz: 48 kHz		127		dB
192 kHz: 32 kHz		127		dB
(20 Hz to $f_{S\_OUT}/2$, 1 kHz, –60 dBFS Input) No Filter				
44.1 kHz: 48 kHz		125		dB
48 kHz: 44.1 kHz		125		dB
48 kHz: 96 kHz		125		dB
44.1 kHz: 192 kHz		125		dB
96 kHz: 48 kHz		124		dB
192 kHz: 32 kHz		124		dB
Total Harmonic Distortion + Noise[2]				
(20 Hz to $f_{S\_OUT}/2$, 1 kHz, 0 dBFS Input) No Filter				
Worst-Case (48 kHz:96 kHz)[3]	–115			dB
44.1 kHz: 48 kHz		–120		dB
48 kHz: 44.1 kHz		–119		dB
48 kHz: 96 kHz		–118		dB
44.1 kHz: 192 kHz		–120		dB
96 kHz: 48 kHz		–122		dB
192 kHz: 32 kHz		–122		dB
Interchannel Gain Mismatch		0.0		dB
Interchannel Phase Deviation		0.0		Degrees
Mute Attenuation (24 Bits Word Width)		–127		dB

NOTES
[1]Lower sampling rates than given by this formula are possible, but the jitter rejection will decrease.
[2]Refer to the Typical Performance Characteristics section for DNR and THD+N numbers over wide range of Input and Output Sample Rates.
[3]For any other ratio, minimum THD+N will be better than –115 dB. Please refer to detailed performance plots.

Specifications subject to change without notice.

DIGITAL TIMING (–40°C < T_A < +105°C, VDD_CORE = 3.3 V ± 5%, VDD_IO = 5.0 V ± 10%)

Parameter[1]		Min	Max	Unit
t_{MCLKI}	MCLK_I Period	33.3		ns
f_{MCLK}	MCLK_I Frequency		30.0[2, 3]	MHz
t_{MPWH}	MCLK_I Pulsewidth High	8		ns
t_{MPWL}	MCLK_I Pulsewidth Low	12		ns
Input Serial Port Timing				
t_{LRIS}	LRCLK_I Setup to SCLK_I	8		ns
t_{SIH}	SCLK_I Pulsewidth High	8		ns
t_{SIL}	SCLK_I Pulsewidth Low	8		ns
t_{DIS}	SDATA_I Setup to SCLK_I Rising Edge	8		ns
t_{DIH}	SDATA_I Hold from SCLK_I Rising Edge	3		ns
Output Serial Port Timing				
t_{TDMS}	TDM_IN Setup to SCLK_O Falling Edge	3		ns
t_{TDMH}	TDM_IN Hold from SCLK_O Falling Edge	3		ns
t_{DOPD}	SDATA_O Propagation Delay from SCLK_O, LRCLK_O		20	ns
t_{DOH}	SDATA_O Hold from SCLK_O	3		ns
t_{LROS}	LRCLK_O Setup to SCLK_O (TDM Mode Only)	5		ns
t_{LROH}	LRCLK_O Hold from SCLK_O (TDM Mode Only)	3		ns
t_{SOH}	SCLK_O Pulsewidth High	10		ns
t_{SOL}	SCLK_O Pulsewidth Low	5		ns
t_{RSTL}	RESET Pulsewidth LO		200	ns

NOTES
[1]Refer to Timing Diagram Section.
[2]The maximum possible sample rate is: $FS_{MAX} = f_{MCLK}/138$.
[3]f_{MCLK} of up to 34 MHz is possible under the following conditions: 0°C < T_A < 70°C, 45/55 or better MCLK_I duty cycle.

Specifications subject to change without notice.

TIMING DIAGRAMS

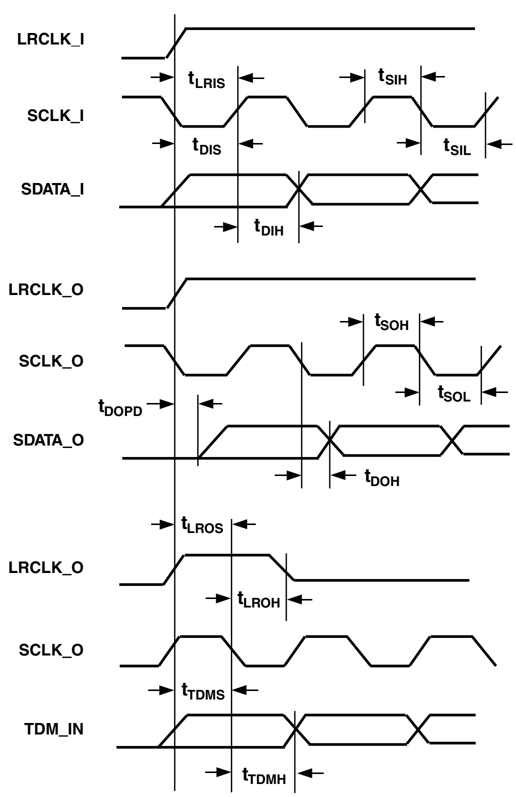


Figure 1. Input and Output Serial Port Timing (SCLK I/O, LRCLK I/O, SDATA I/O, TDM_IN)

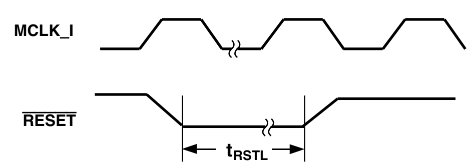


Figure 2. $\overline{RESET}$ Timing

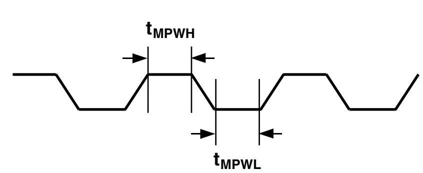


Figure 3. MCLK_I Timing

AD1895–SPECIFICATIONS

DIGITAL FILTERS (VDD_CORE = 3.3 V ± 5%, VDD_IO = 5.0 V ± 10%)

Parameter	Min	Typ	Max	Unit
Passband			0.4535 f_{S_OUT}	Hz
Passband Ripple			±0.016	dB
Transition Band	0.4535 f_{S_OUT}		0.5465 f_{S_OUT}	Hz
Stop Band	0.5465 f_{S_OUT}			Hz
Stop Band Attenuation		–125		dB
Group Delay	Refer to the Group Delay Equations Section			

Specifications subject to change without notice.

DIGITAL I/O CHARACTERISTICS (VDD_CORE = 3.3 V ± 5%, VDD_IO = 5.0 V ± 10%)

Parameter	Min	Typ	Max	Unit
Input Voltage HI (V_{IH})	2.4			
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 5 V)			2	µA
Input Leakage (I_{IL} @ V_{IL} = 0 V)			–2	µA
Input Capacitance		5	10	pF
Output Voltage HI (V_{OH} @ I_{OH} = –4 mA)	VDD_CORE – 0.5	VDD_CORE – 0.4		V
Output Voltage LO (V_{OL} @ I_{OL} = +4 mA)		0.2	0.5	V
Output Source Current HI (I_{OH})			–4	mA
Output Sink Current LO (I_{OL})			+4	mA

Specifications subject to change without notice.

POWER SUPPLIES

Parameter	Min	Typ	Max	Unit
Supply Voltage				
VDD_CORE	3.135	3.3	3.465	V
VDD_IO*	VDD_CORE	3.3/5.0	5.5	V
Active Supply Current				
I_ CORE_ACTIVE				
48 kHz: 48 kHz		20		mA
96 kHz: 96 kHz		26		mA
192 kHz: 192 kHz		43		mA
I_IO_ACTIVE		2		mA
Power-Down Supply Current: (All Clocks Stopped)				
I_CORE_PWRDN		0.5		mA
I_IO_PWRDN		10		µA

*For 3.3 V tolerant Inputs, VDD_IO supply should be set to 3.3 V; however, VDD_CORE supply voltage should not exceed VDD_IO.

Specifications subject to change without notice.

POWER SUPPLIES (VDD_CORE = 3.3 V ± 5%, VDD_IO = 5.0 V ± 10%)

Parameter	Min	Typ	Max	Unit
Total Active Power Dissipation				
48 kHz: 48 kHz		65		mW
96 kHz: 96 kHz		85		mW
192 kHz: 192 kHz		132		mW
Total Power Down Dissipation: (RESET LO)		2		mW

Specifications subject to change without notice.

TEMPERATURE RANGE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+105	°C
Storage	–55		+150	°C
Thermal Resistance, θ_{JA} (Junction-to-Ambient)		109		°C/W

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
Power Supplies			
VDD_CORE	–0.3	+3.6	V
VDD_IO	–0.3	+6.0	V
Digital Inputs			
Input Current		±10	mA
Input Voltage	DGND – 0.3	VDD_IO + 0.3	V
Ambient Temperature (Operating)	–40	+105	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1895YRS	–40°C to +105°C	28-Lead SSOP	RS-28
AD1895YRSRL	–40°C to +105°C	28-Lead SSOP	RS-28 on 13" Reel

CAUTION

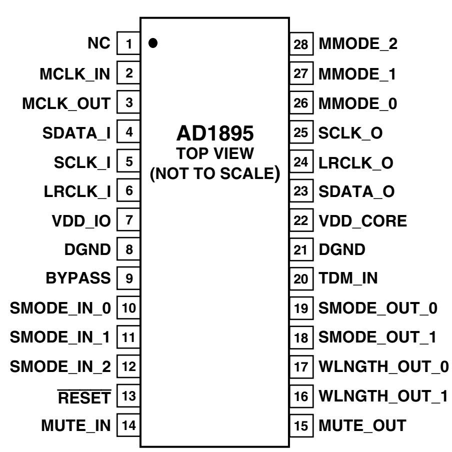
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1895 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

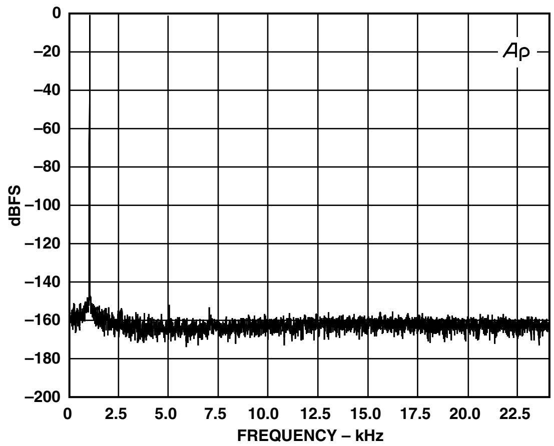
Pin No.	IN/OUT	Mnemonic	Description
1	IN	NC	No Connect
2	IN	MCLK_IN	Master Clock or Crystal Input
3	OUT	MCLK_OUT	Master Clock Output or Crystal Output
4	IN	SDATA_I	Input Serial Data (at Input Sample Rate)
5	IN/OUT	SCLK_I	Master/Slave Input Serial Bit Clock
6	IN/OUT	LRCLK_I	Master/Slave Input Left/Right Clock
7	IN	VDD_IO	3.3 V/5 V Input/Output Digital Supply Pin
8	IN	DGND	Digital Ground Pin
9	IN	BYPASS	ASRC Bypass Mode, Active High
10	IN	SMODE_IN_0	Input Port Serial Interface Mode Select Pin 0
11	IN	SMODE_IN_1	Input Port Serial Interface Mode Select Pin 1
12	IN	SMODE_IN_2	Input Port Serial Interface Mode Select Pin 2
13	IN	$\overline{\text{RESET}}$	Reset Pin, Active Low
14	IN	MUTE_IN	Mute Input Pin— Active HI Normally Connected to MUTE_OUT
15	OUT	MUTE_OUT	Output Mute Control – Active HI
16	IN	WLNGTH_OUT_1	Hardware Selectable Output Wordlength—Select Pin 1
17	IN	WLNGTH_OUT_0	Hardware Selectable Output Wordlength—Select Pin 0
18	IN	SMODE_OUT_1	Output Port Serial Interface Mode Select Pin 1
19	IN	SMODE_OUT_0	Output Port Serial Interface Mode Select Pin 0
20	IN	TDM_IN	Serial Data Input* (Only for Daisy-Chain Mode). Ground when not used.
21	IN	DGND	Digital Ground Pin
22	IN	VDD_CORE	3.3 V Digital Supply Pin
23	OUT	SDATA_O	Output Serial Data (at Output Sample Rate)
24	IN/OUT	LRCLK_O	Master/Slave Output Left/Right Clock
25	IN/OUT	SCLK_O	Master/Slave Output Serial Bit Clock
26	IN	MMODE_0	Master/Slave Clock Ratio Mode Select Pin 0
27	IN	MMODE_1	Master/Slave Clock Ratio Mode Select Pin 1
28	IN	MMODE_2	Master/Slave Clock Ratio Mode Select Pin 2

*Also used to input matched-phase mode data.

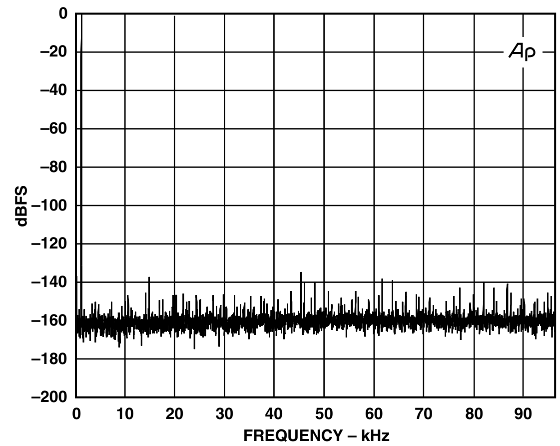
PIN CONFIGURATION



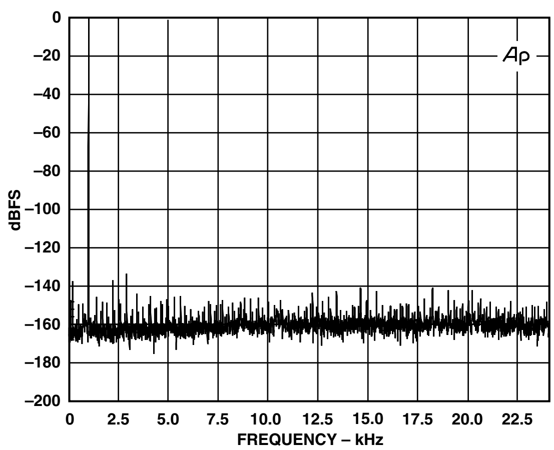
NC = NO CONNECT



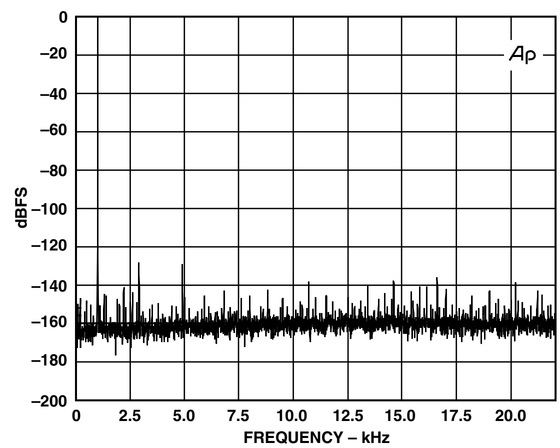
TPC 1. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 48 kHz:48 kHz (Asynchronous)



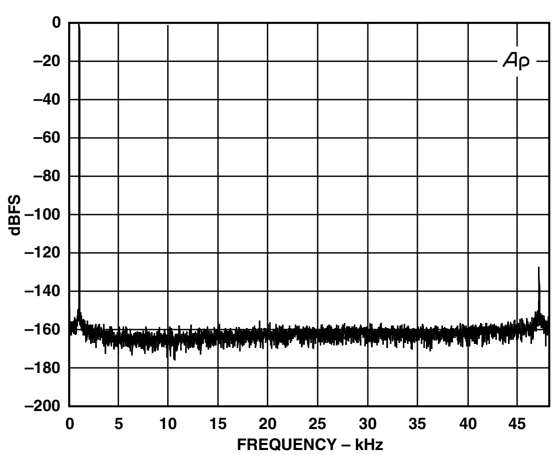
TPC 4. Wideband FFT Plot (16k Points) 44.1 kHz:192 kHz, 0 dBFS 1 kHz Tone



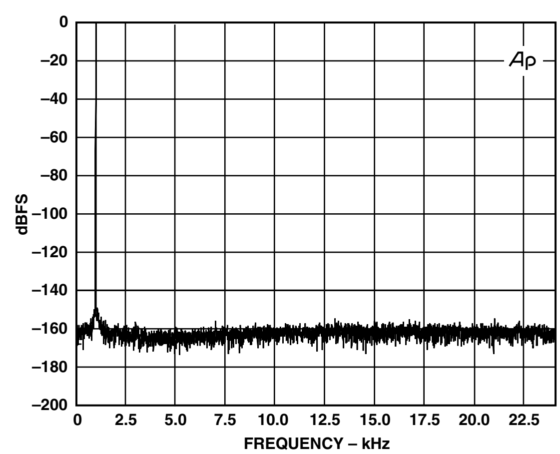
TPC 2. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 44.1 kHz:48 kHz (Asynchronous)



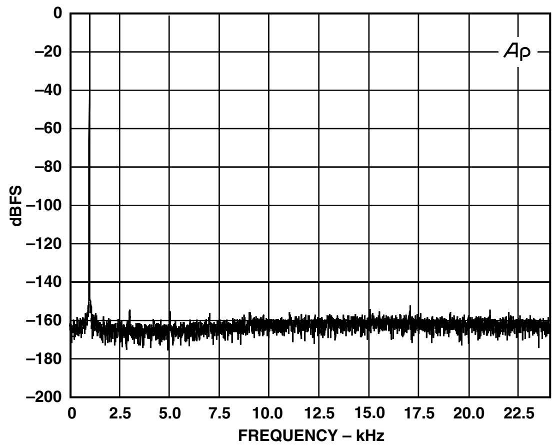
TPC 5. Wideband FFT Plot (16k Points) 48 kHz:44.1 kHz, 0 dBFS 1 kHz Tone



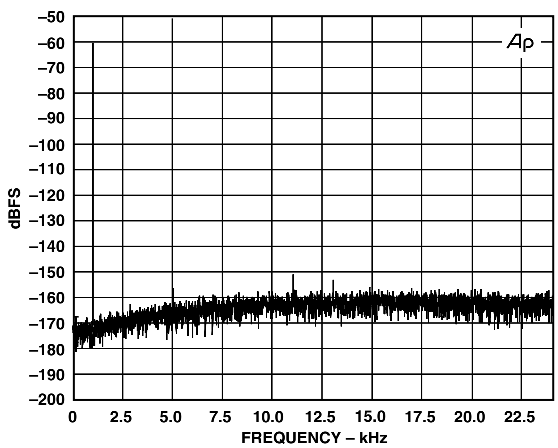
TPC 3. Wideband FFT Plot (16k Points) 48 kHz:96 kHz, 0 dBFS 1 kHz Tone



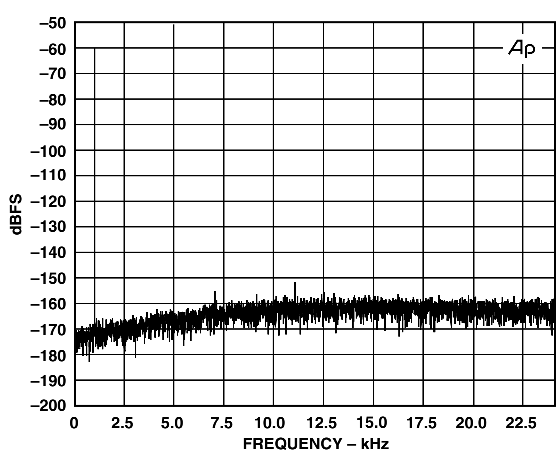
TPC 6. Wideband FFT Plot (16k Points) 96 kHz:48 kHz, 0 dBFS 1 kHz Tone



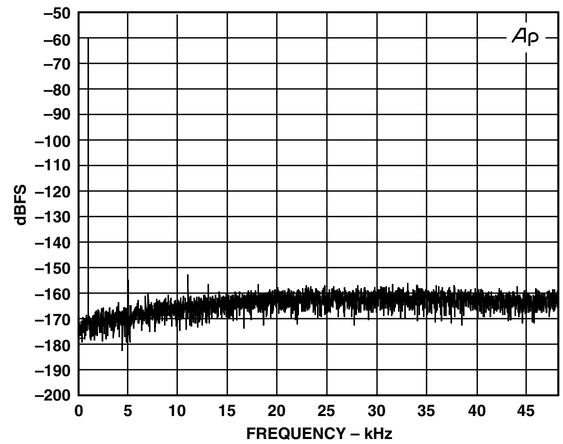
TPC 7. Wideband FFT Plot (16k Points) 192 kHz:48 kHz, 0 dBFS 1 kHz Tone



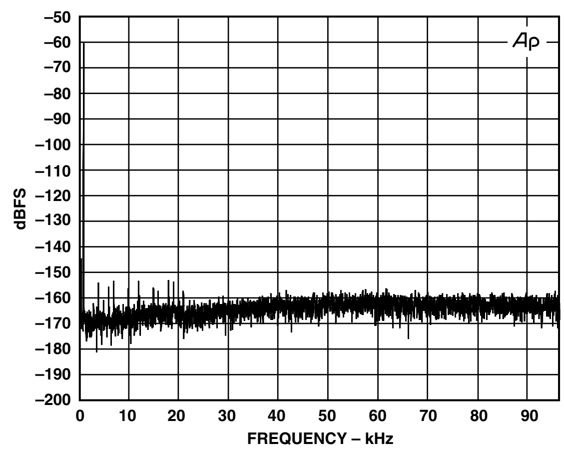
TPC 8. Wideband FFT Plot (16k Points) –60 dBFS 1 kHz Tone, 48 kHz:48 kHz (Asynchronous)



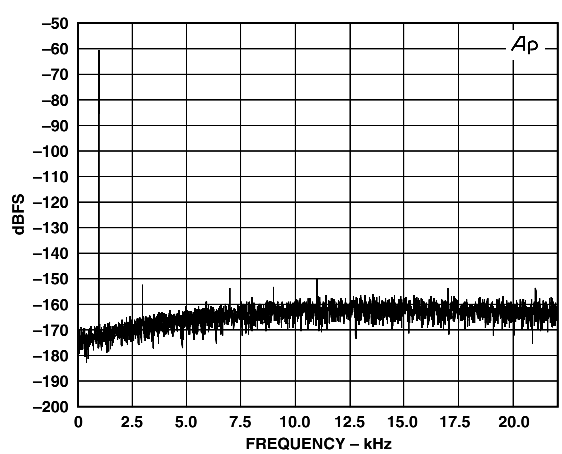
TPC 9. Wideband FFT Plot (16k Points) 44.1 kHz:48 kHz, –60 dBFS 1 kHz Tone



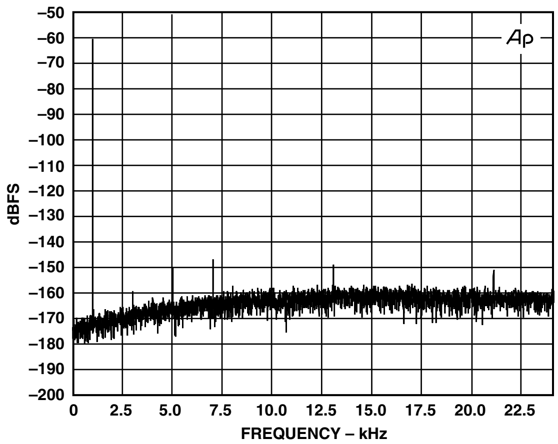
TPC 10. Wideband FFT Plot (16k Points) 48 kHz:96 kHz, –60 dBFS 1 kHz Tone



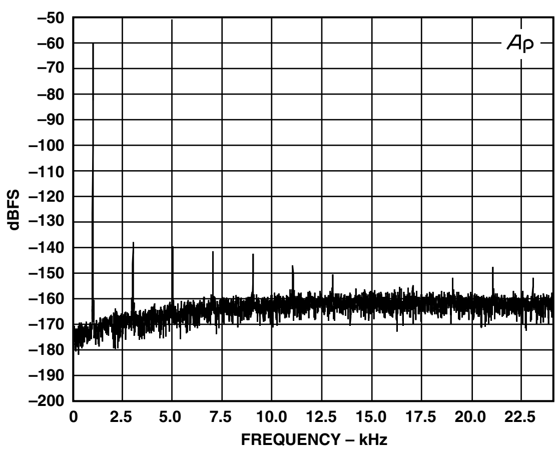
TPC 11. Wideband FFT Plot (16k Points) 44.1 kHz:192 kHz, –60 dBFS 1 kHz Tone



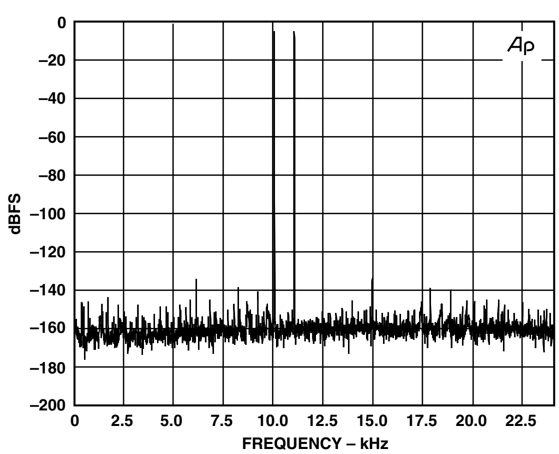
TPC 12. Wideband FFT Plot (16k Points) 48 kHz:44.1 kHz, –60 dBFS 1 kHz Tone



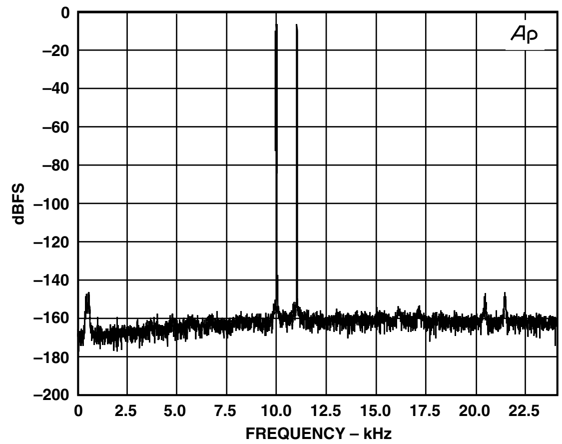
TPC 13. Wideband FFT Plot (16k Points) 96 kHz:48 kHz, –60 dBFS 1 kHz Tone



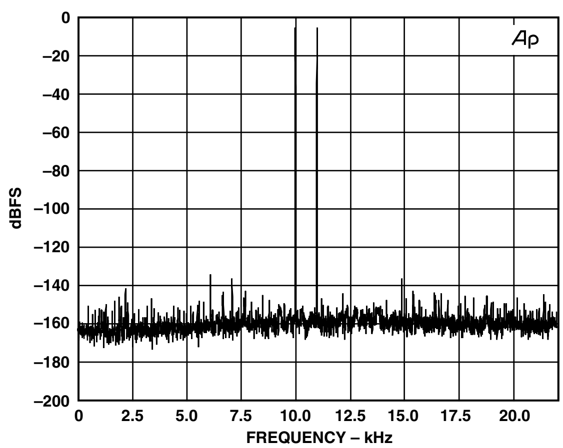
TPC 14. Wideband FFT Plot (16k Points) 192 kHz:48 kHz, –60 dBFS 1 kHz Tone



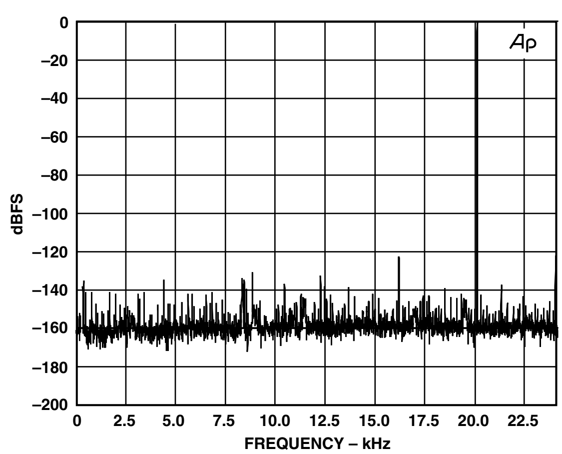
TPC 15. IMD, 10 kHz and 11 kHz 0 dBFS Tone 44:1 kHz:48 kHz



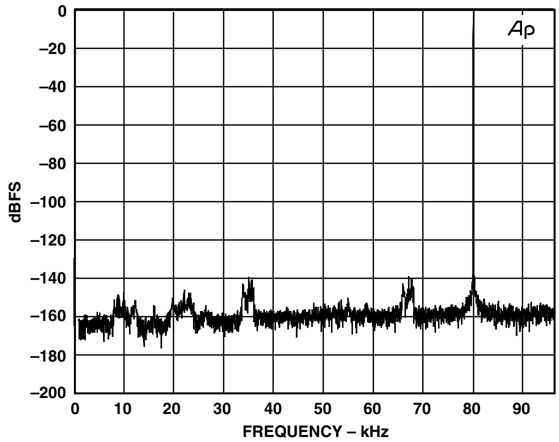
TPC 16. IMD, 10 kHz and 11 kHz 0 dBFS Tone 96 kHz:48 kHz



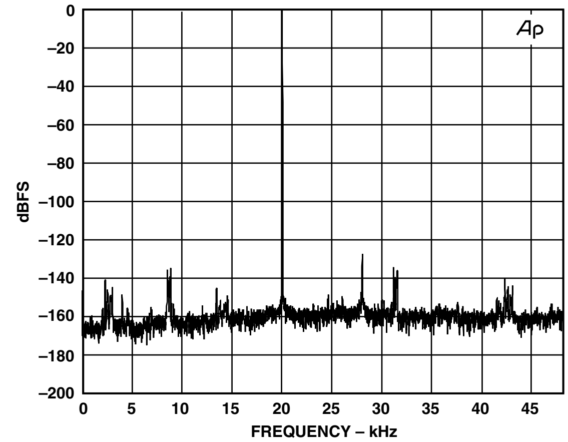
TPC 17. IMD, 10 kHz and 11 kHz 0 dBFS Tone 48 kHz:44.1 kHz



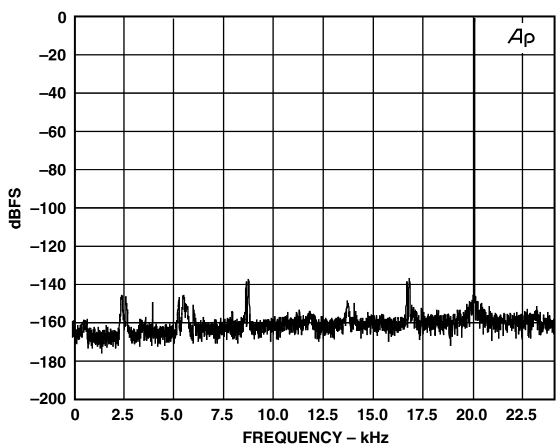
TPC 18. Wideband FFT Plot (16k Points) 44.1 kHz:48 kHz, 0 dBFS 20 kHz Tone



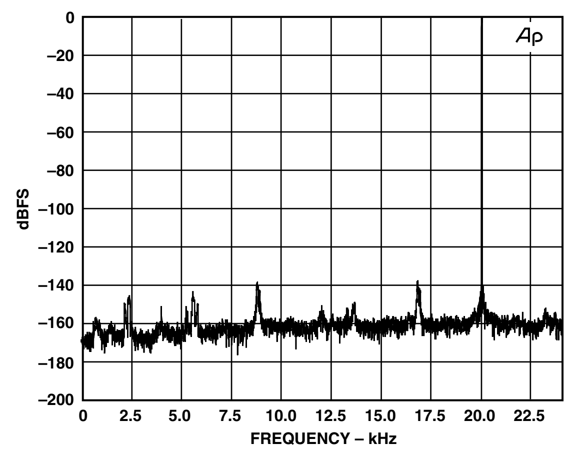
TPC 19. Wideband FFT Plot (16k Points) 192 kHz:192 kHz, 0 dBFS 80 kHz Tone



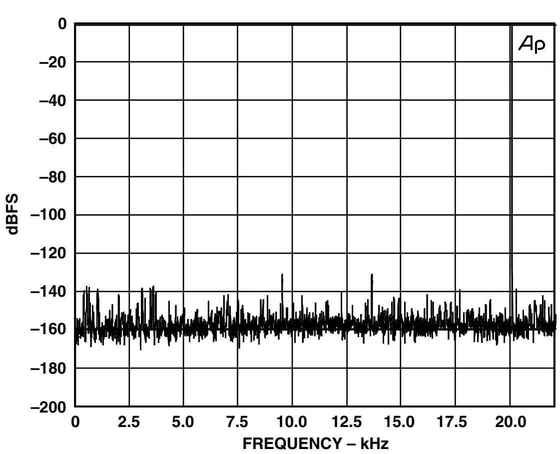
TPC 22. Wideband FFT Plot (16k Points) 48 kHz:96 kHz, 0 dBFS 20 kHz Tone



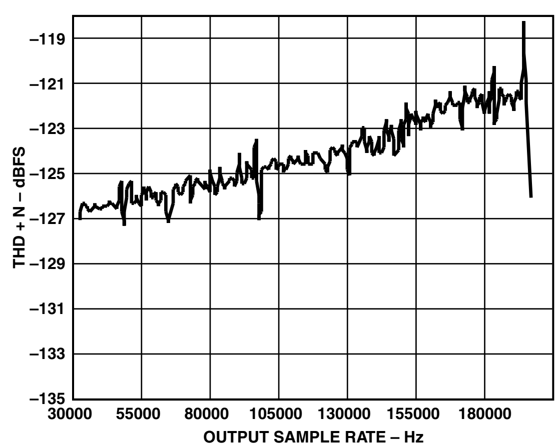
TPC 20. Wideband FFT Plot (16k Points) 48 kHz:48 kHz, 0 dBFS 20 kHz Tone



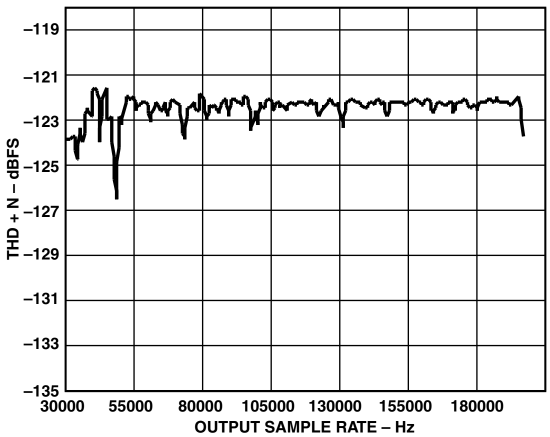
TPC 23. Wideband FFT Plot (16k Points) 96 kHz:48 kHz, 0 dBFS 20 kHz Tone



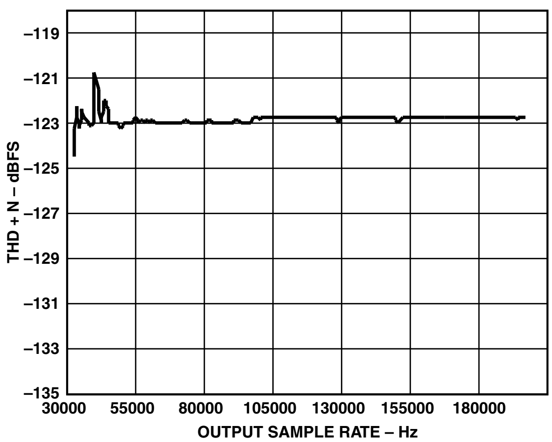
TPC 21. Wideband FFT Plot (16k Points) 48 kHz:44:1 kHz, 0 dBFS 20 kHz Tone



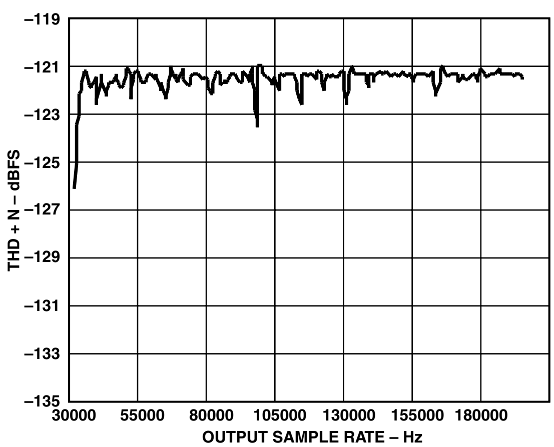
TPC 24. THD + N vs. Output Sample Rate, f_{S_IN} = 192 kHz, 0 dBFS 1 kHz Tone



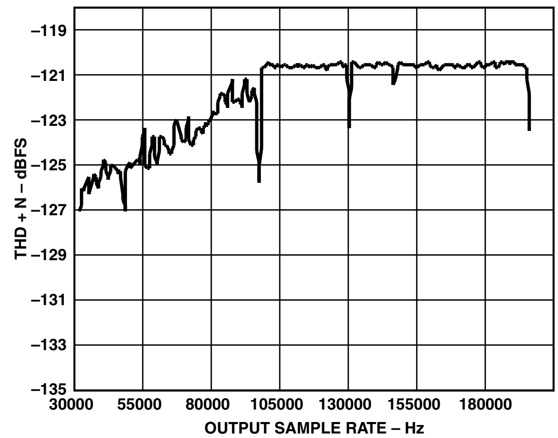
TPC 25. THD + N vs. Output Sample Rate, f_{S_IN} = 48 kHz, 0 dBFS 1 kHz Tone



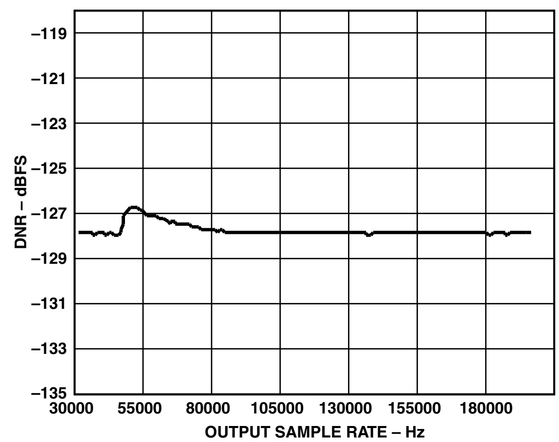
TPC 26. THD + N vs. Output Sample Rate, f_{S_IN} = 44.1 kHz, 0 dBFS 1 kHz Tone



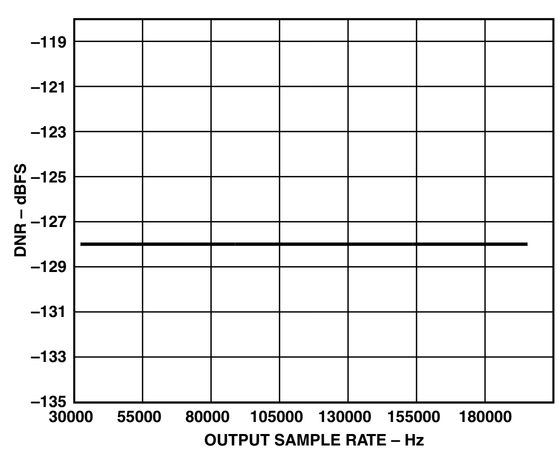
TPC 27. THD + N vs. Output Sample Rate, f_{S_IN} = 32 kHz, 0 dBFS 1 kHz Tone



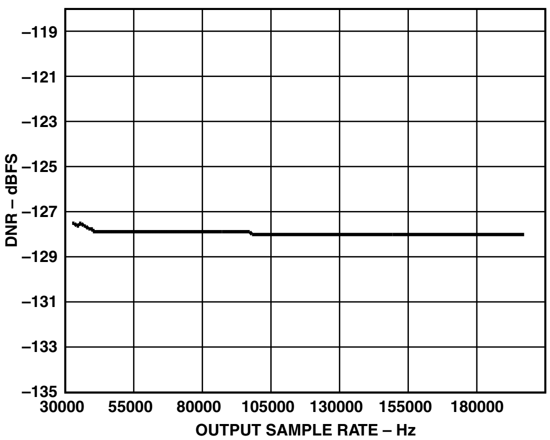
TPC 28. THD + N vs. Output Sample Rate, f_{S_IN} = 96 kHz, 0 dBFS 1 kHz Tone



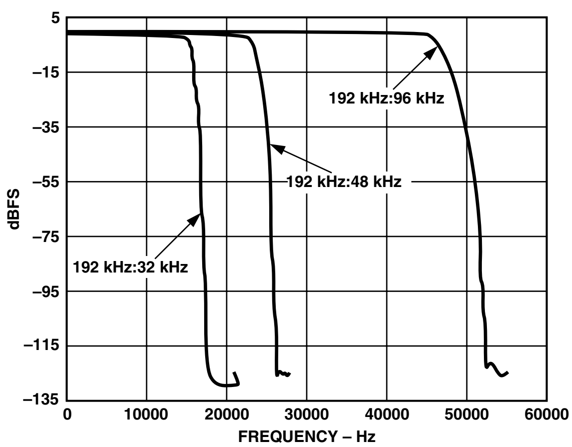
TPC 29. DNR vs. Output Sample Rate, f_{S_IN} = 192 kHz, –60 dBFS 1 kHz Tone



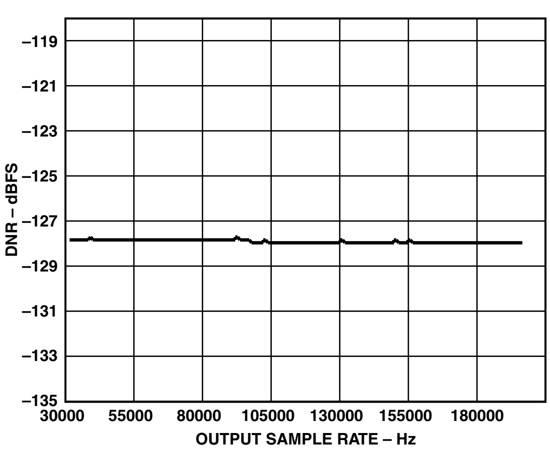
TPC 30. DNR vs. Output Sample Rate, f_{S_IN} = 32 kHz, –60 dBFS 1 kHz Tone



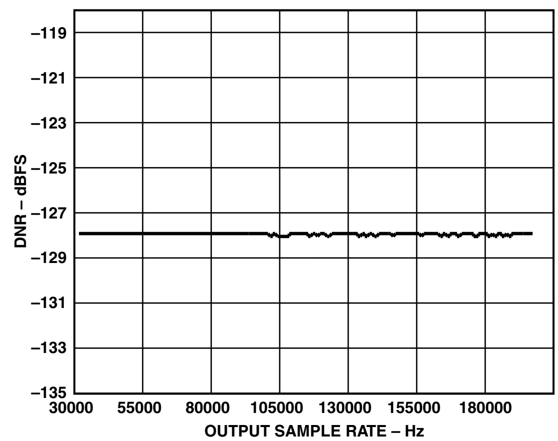
TPC 31. DNR vs. Output Sample Rate, f_{S_IN} = 96 kHz, –60 dBFS 1 kHz Tone



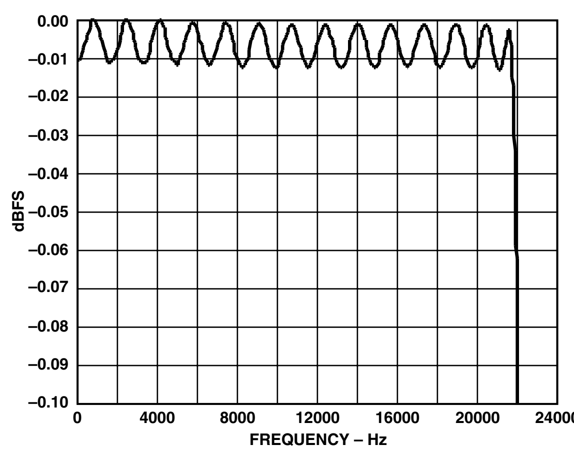
TPC 32. Digital Filter Frequency Response



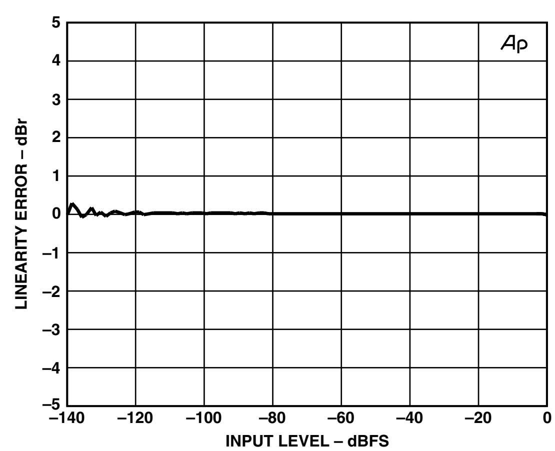
TPC 33. DNR vs. Output Sample Rate, f_{S_IN} = 48 kHz, –60 dBFS 1 kHz Tone



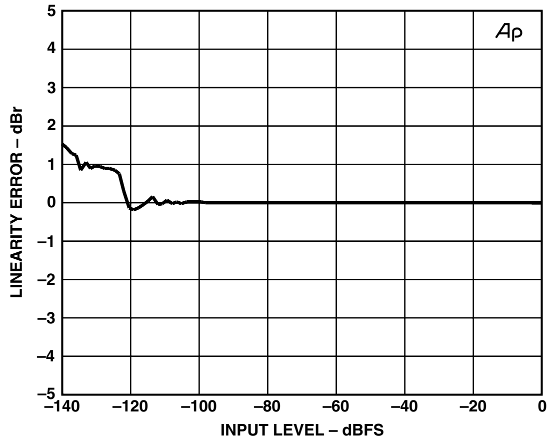
TPC 34. DNR vs. Output Sample Rate, f_{S_IN} = 44.1 kHz, –60 dBFS 1 kHz Tone



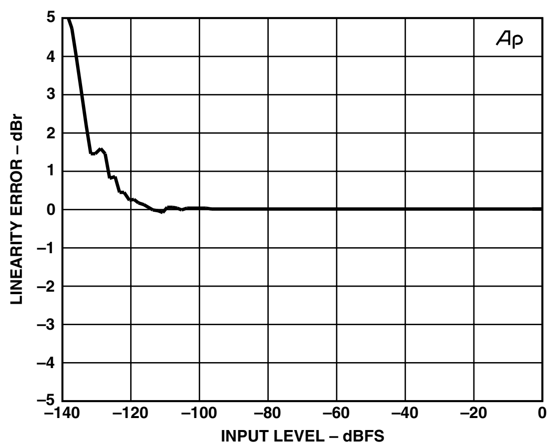
TPC 35. Passband Ripple, 192 kHz:48 kHz



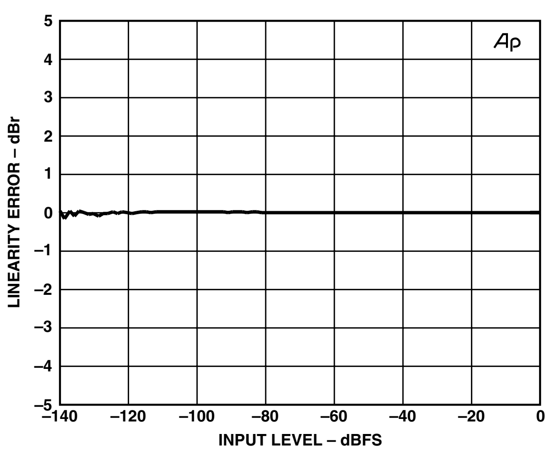
TPC 36. Linearity Error, 48 kHz:48 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



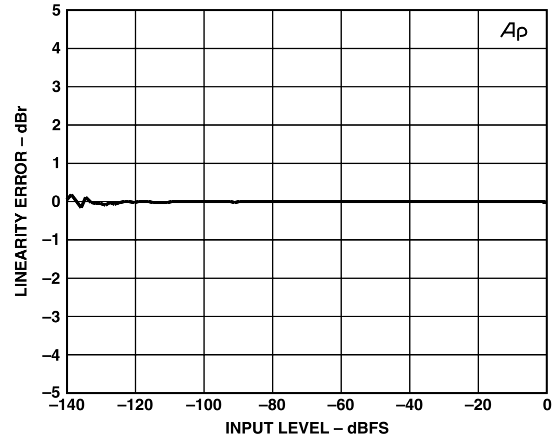
TPC 37. Linearity Error, 48 kHz:44.1 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



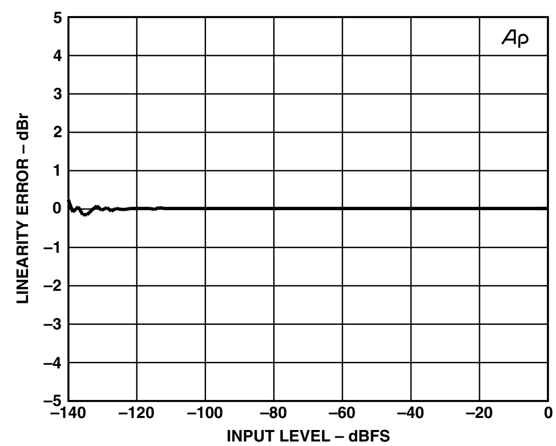
TPC 38. Linearity Error, 96 kHz:48 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



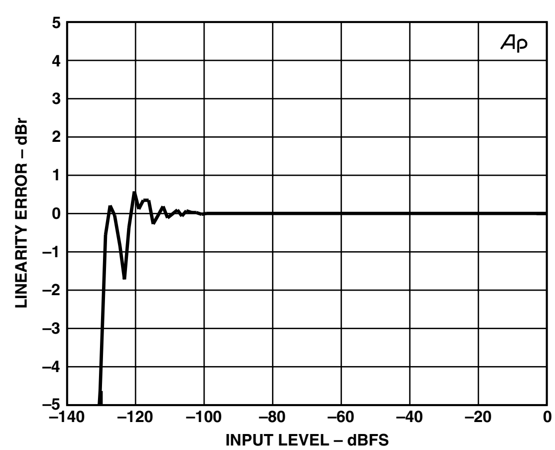
TPC 39. Linearity Error, 44.1 kHz:48 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



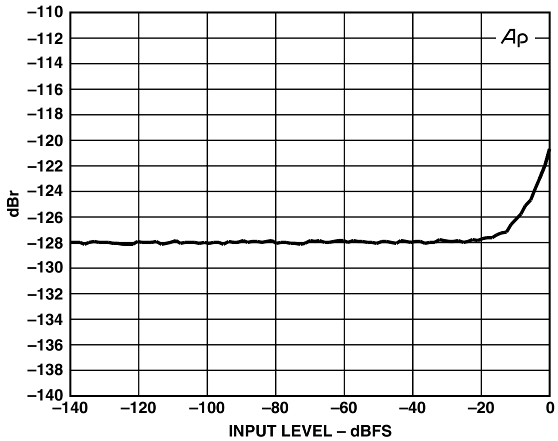
TPC 40. Linearity Error, 48 kHz:96 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



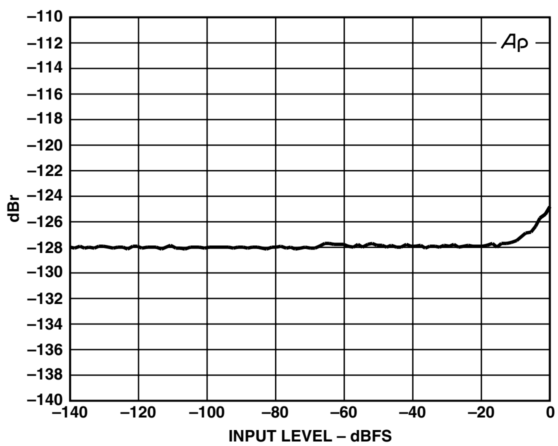
TPC 41. Linearity Error, 44.1 kHz:192 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



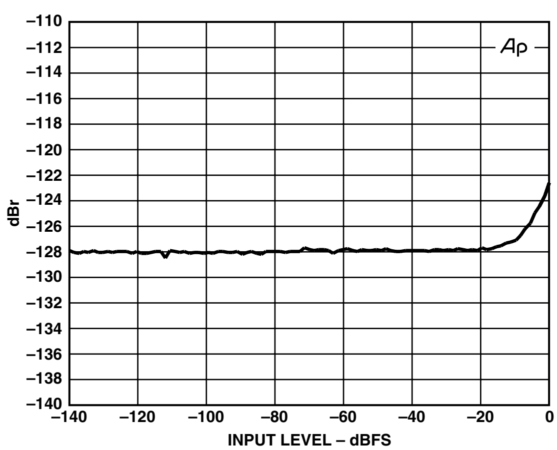
TPC 42. Linearity Error, 192 kHz:44:1 kHz, 0 dBFS to –140 dBFS Input, 200 Hz Tone



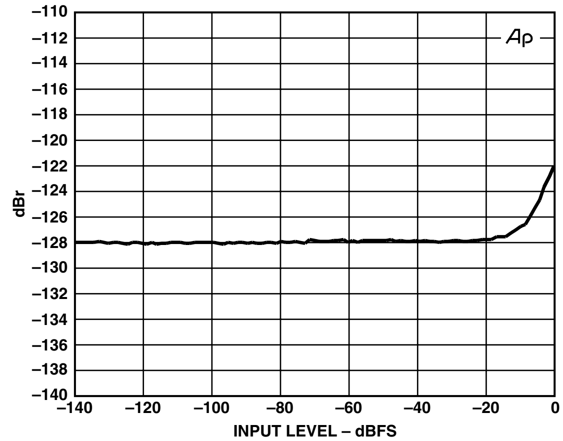
TPC 43. THD + N vs. Input Amplitude, 48 kHz:44.1 kHz, 1 kHz Tone



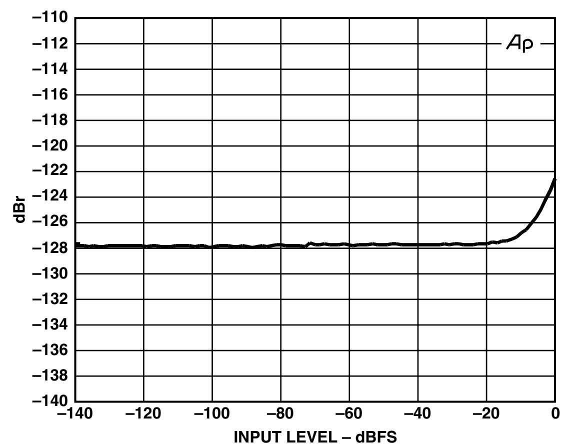
TPC 44. THD + N vs. Input Amplitude, 96 kHz:48 kHz, 1 kHz Tone



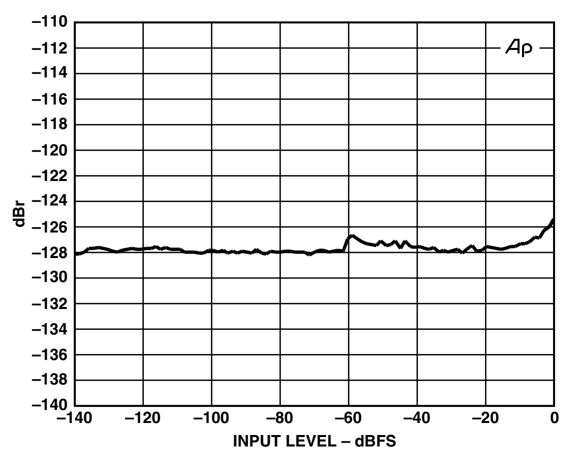
TPC 45. THD + N vs. Input Amplitude, 44.1 kHz:48 kHz, 1 kHz Tone



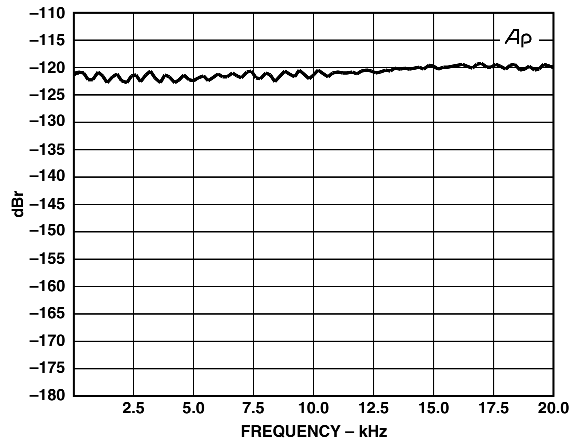
TPC 46. THD + N vs. Input Amplitude, 48 kHz:96 kHz, 1 kHz Tone



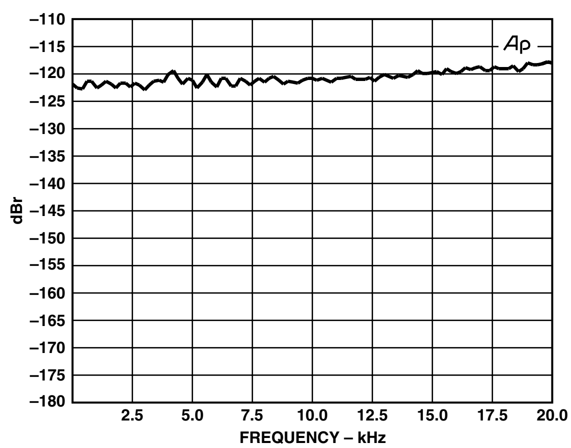
TPC 47. THD + N vs. Input Amplitude, 44.1 kHz:192 kHz, 1 kHz Tone



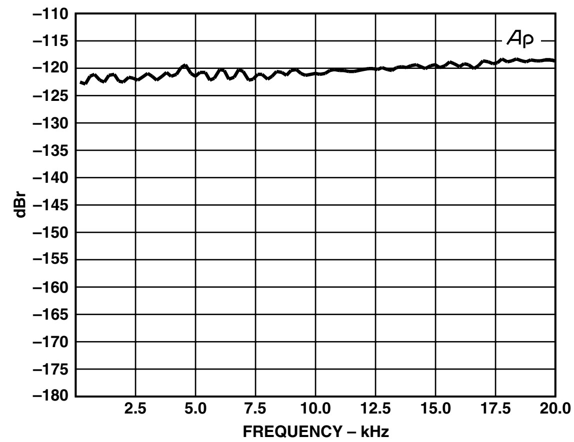
TPC 48. THD + N vs. Input Amplitude, 192 kHz:48 kHz, 1 kHz Tone



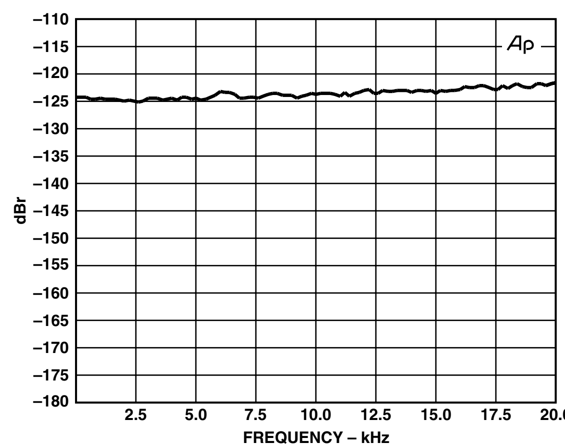
TPC 49. THD + N vs. Frequency Input, 48 kHz:44.1 kHz, 0 dBFS



TPC 50. THD + N vs. Frequency Input, 44.1 kHz:48 kHz, 00 dBFS



TPC 51. THD + N vs. Frequency Input, 48 kHz:96 kHz, 0 dBFS



TPC 52. THD + N vs. Frequency Input, 96 kHz:48 kHz, 0 dBFS

(*Continued from page 1*)

The digital servo loop measures the time difference between input and output sample rates within 5 ps. This is necessary in order to select the correct polyphase filter coefficient The digital servo loop has excellent jitter rejection for both input and output sample rates as well as the master clock. The jitter rejection begins at less than 1 Hz. This requires a long settling time whenever $\overline{\text{RESET}}$ is deasserted or when the input or output sample rate changes. To reduce the settling time, upon deassertion of $\overline{\text{RESET}}$ or a change in a sample rate, the digital servo loop enters the fast settling mode. When the digital servo loop has adequately settled in the fast mode, it switches into the normal or slow settling mode and continues to settle until the time difference measurement between input and output sample rates is within 5 ps. During fast mode, the MUTE_OUT signal is asserted high. Normally, the MUTE_OUT is connected to the MUTE_IN pin. The MUTE_IN signal is used to softly mute the AD1895 upon assertion and softly unmute the AD1895 when it is deasserted.

The sample rate converter of the AD1895 can be bypassed altogether using the bypass mode. In bypass mode, the AD1895's serial input data is directly passed to the serial output port without any dithering. This is useful for passing through nonaudio data or when the input and output sample rates are synchronous to one another and the sample rate ratio is exactly 1 to 1.

The AD1895 is a 3.3 V, 5 V input tolerant part and is available in a 28-lead SSOP SMD package. The AD1895 is 5 V input-tolerant only when the VDD_IO supply pin is supplied with 5 V.

ASRC FUNCTIONAL OVERVIEW

THEORY OF OPERATION

Asynchronous sample rate conversion is converting data from one clock source at some sample rate to another clock source at the same or different sample rate. The simplest approach to asynchronous sample rate conversion is the use of a zero-order hold between two samplers shown in Figure 4. In an asynchronous system T2 is never equal to T1 nor is the ratio between T2 and T1 rational. As a result, samples at f_{S_OUT} will be repeated or dropped producing an error in the resampling process. The frequency domain shows the wide side lobes that result from this error when the sampling of f_{S_OUT} is convolved with the attenuated images from the sin(x)/x nature of the zero-order hold. The images at f_{S_IN}, dc signal images, of the zero-order hold are infinitely attenuated. Since the ratio of T2 to T1 is an irrational number, the error resulting from the resampling at f_{S_OUT} can never be eliminated. However, the error can be significantly reduced through interpolation of the input data at f_{S_IN}. The AD1895 is conceptually interpolated by a factor of 2^{20}.

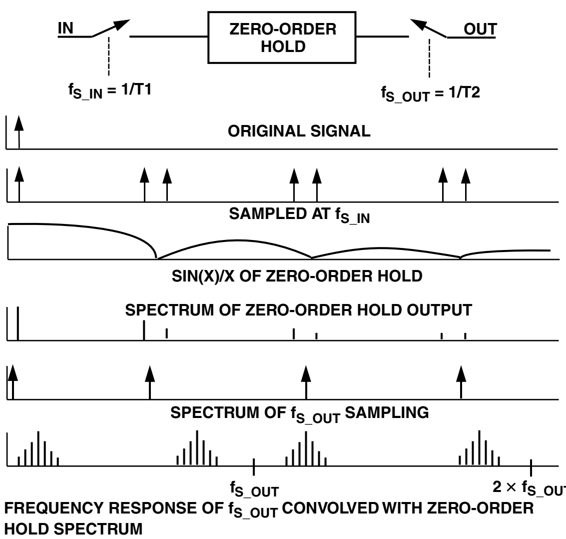


Figure 4. Zero-Order Hold Being Used by f_{S_OUT} to Resample Data from f_{S_IN}

THE CONCEPTUAL HIGH INTERPOLATION MODEL

Interpolation of the input data by a factor of 2^{20} involves placing $(2^{20}-1)$ samples between each f_{S_IN} sample. Figure 5 shows both the time domain and the frequency domain of interpolation by a factor of 2^{20}. Conceptually, interpolation by 2^{20} would involve the steps of zero-stuffing $(2^{20}-1)$ number of samples between each f_{S_IN} sample and convolving this interpolated signal with a digital low-pass filter to suppress the images. In the time domain it can be seen that f_{S_OUT} selects the closest $f_{S\_IN} \times 2^{20}$ sample from the zero-order hold as opposed to the nearest f_{S_IN} sample in the case of no interpolation. This significantly reduces the resampling error.

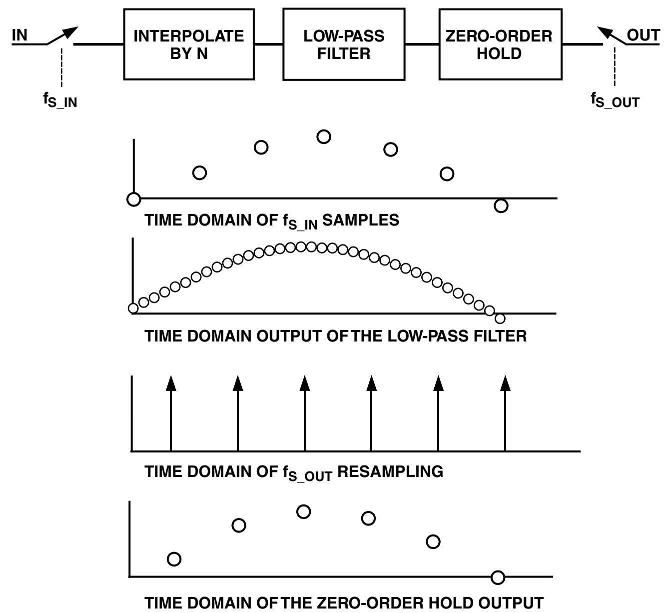


Figure 5. Time Domain of the Interpolation and Resampling

In the frequency domain shown in Figure 6 the interpolation expands the frequency axis of the zero-order hold. The images from the interpolation can be sufficiently attenuated by a good low-pass filter. The images from the zero-order hold are now pushed by a factor of 2^{20} closer to the infinite attenuation point of the zero-order hold, which is $f_{S\_IN} \times 2^{20}$. The images at the zero-order hold are the determining factor for the fidelity of the output at f_{S_OUT}. The worst-case images can be computed from the zero-order hold frequency response, maximum image = $\sin(\pi \times F/f_{S\_INTERP})/(\pi \times F/f_{S\_INTERP})$. F is the frequency of the worst-case image which would be $2^{20} \times f_{S\_IN} \pm f_{S\_IN}/2$, and f_{S_INTERP} is $f_{S\_IN} \times 2^{20}$.

The following worst-case images would appear for f_{S_IN} = 192 kHz:

Image at f_{S_INTERP} – 96 kHz = –125.1 dB
Image at f_{S_INTERP} + 96 kHz = –125.1 dB

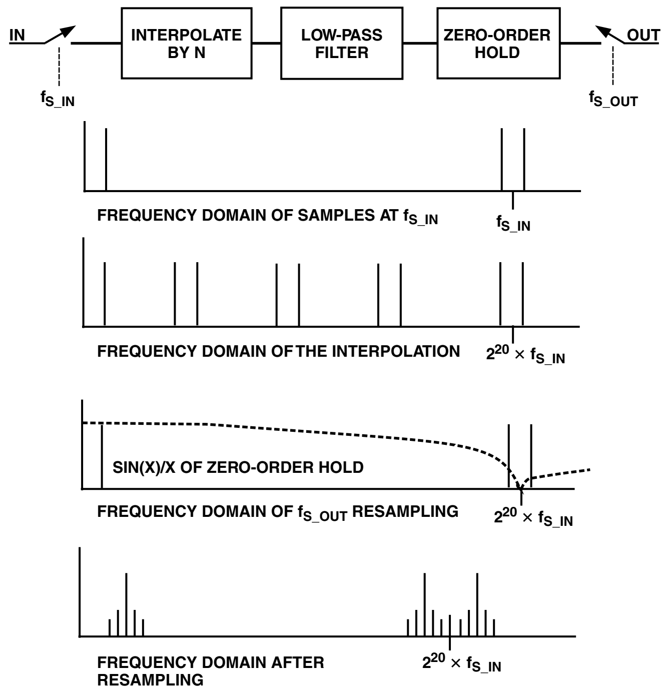


Figure 6. Frequency Domain of the Interpolation and Resampling

HARDWARE MODEL

The output rate of the low-pass filter of Figure 5 would be the interpolation rate, $2^{20} \times 192000$ kHz = 201.3 GHz. Sampling at a rate of 201.3 GHz is clearly impractical, not to mention the number of taps required to calculate each interpolated sample. However, since interpolation by 2^{20} involves zero-stuffing $2^{20}–1$ samples between each f_{S_IN} sample, most of the multiplies in the low-pass FIR filter are by zero. A further reduction can be realized by the fact that since only one interpolated sample is taken at the output at the f_{S_OUT} rate, only one convolution needs to be performed per f_{S_OUT} period instead of 2^{20} convolutions. A 64-tap FIR filter for each f_{S_OUT} sample is sufficient to suppress the images caused by the interpolation.

The difficulty with the above approach is that the correct interpolated sample needs to be selected upon the arrival of f_{S_OUT}. Since there are 2^{20} possible convolutions per f_{S_OUT} period, the arrival of the f_{S_OUT} clock must be measured with an accuracy of 1/201.3 GHz = 4.96 ps. Measuring the f_{S_OUT} period with a clock of 201.3 GHz frequency is clearly impossible; instead, several coarse measurements of the f_{S_OUT} clock period are made and averaged over time.

Another difficulty with the above approach is the number of coefficients required. Since there are 2^{20} possible convolutions with a 64-tap FIR filter, there need to be 2^{20} polyphase coefficients for each tap, which requires a total of 2^{26} coefficients. To reduce the number of coefficients in ROM, the AD1895 stores a small subset of coefficients and performs a high-order interpolation between the stored coefficients. So far the above approach works for the case of $f_{S\_OUT} > f_{S\_IN}$. However, in the case when the output sample rate, f_{S_OUT}, is less than the input sample rate, f_{S_IN}, the ROM starting address, input data and the length of the convolution must be scaled. As the input sample rate rises over the output sample rate, the antialiasing filter's cutoff frequency has to be lowered because the Nyquist frequency of the output samples is less than the Nyquist frequency of the input samples. To move the cutoff frequency of the antialiasing filter, the coefficients are dynamically altered and the length of the convolution is increased by a factor of (f_{S_IN}/f_{S_OUT}). This technique is supported by the Fourier transform property that if f(t) is F(ω), then f(k × t) is F(ω/k). Thus, the range of decimation is simply limited by the size of the RAM.

THE SAMPLE RATE CONVERTER ARCHITECTURE

The architecture of the sample rate converter is shown in Figure 7. The sample rate converter's FIFO block adjusts the left and right input samples and stores them for the FIR filter's convolution cycle. The f_{S_IN} counter provides the write address to the FIFO block and the ramp input to the digital servo loop. The ROM stores the coefficients for the FIR filter convolution and performs a high-order interpolation between the stored coefficients. The sample rate ratio block measures the sample rate for dynamically altering the ROM coefficients and scaling of the FIR filter length as well as the input data. The digital servo loop automatically tracks the f_{S_IN} and f_{S_OUT} sample rates and provides the RAM and ROM start addresses for the start of the FIR filter convolution.

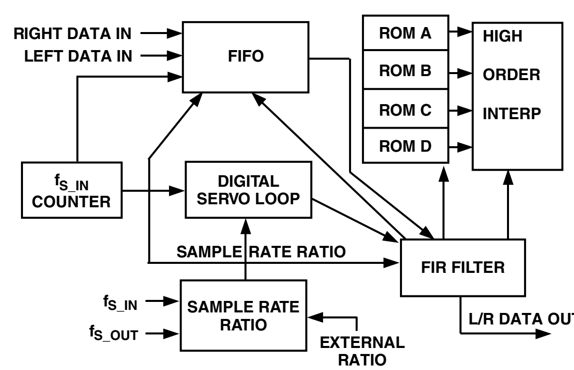


Figure 7. Architecture of the Sample Rate Converter

The FIFO receives the left and right input data and adjusts the amplitude of the data for both the soft muting of the sample rate converter and the scaling of the input data by the sample rate ratio before storing the samples in the RAM. The input data is scaled by the sample rate ratio because as the FIR filter length of the convolution increases, so does the amplitude of the convolution output. To keep the output of the FIR filter from saturating, the input data is scaled down by multiplying it by (f_{S_OUT}/f_{S_IN}) when $f_{S\_OUT} < f_{S\_IN}$. The FIFO also scales the input data for muting and unmuting of the AD1895.

The RAM in the FIFO is 512 words deep for both left and right channels. A small offset of 16 is added to the write address provided by the f_{S_IN} counter to prevent the RAM read pointer from ever overlapping the write address. The maximum decimation rate can be calculated from the RAM word depth as (512–16)/64 taps = 7.75 and a small offset.

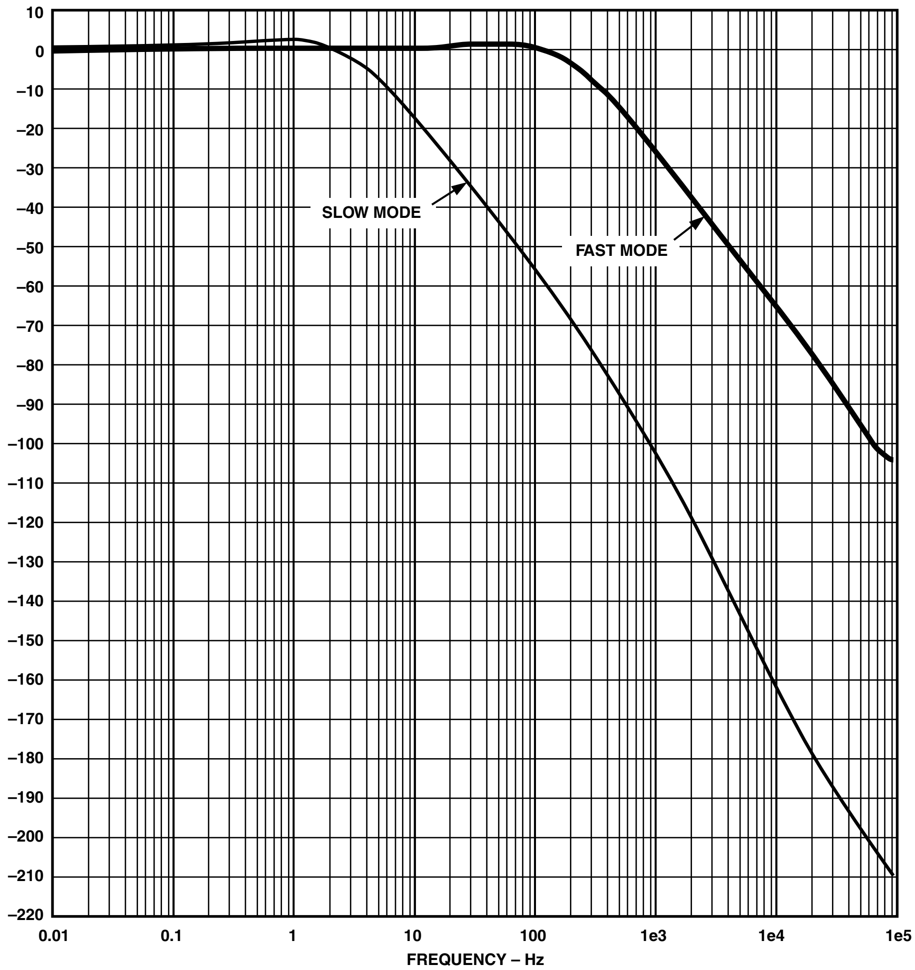


Figure 8. Frequency Response of the Digital Servo Loop. f_{S_IN} is the X-Axis, f_{S_OUT} = 192 kHz, Master Clock Frequency Is 30 MHz

The digital servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter while the ROM is the fractional part. The digital servo loop must be able to provide excellent rejection of jitter on the f_{S_IN} and f_{S_OUT} clocks as well as measure the arrival of the f_{S_OUT} clock within 4.97 ps. The digital servo loop will also divide the fractional part of the ramp output by the ratio of f_{S_IN}/f_{S_OUT} for the case when $f_{S\_IN} > f_{S\_OUT}$, to dynamically alter the ROM coefficients.

The digital servo loop is implemented with a multirate filter. To settle the digital servo loop filter quicker upon start-up or a change in the sample rate, a "fast mode" was added to the filter. When the digital servo loop starts up or the sample rate is changed, the digital servo loop kicks into "fast mode" to adjust and settle on the new sample rate. Upon sensing the digital servo loop settling down to some reasonable value, the digital servo loop will kick into "normal" or "slow mode." During "fast mode" the MUTE_OUT signal of the sample rate converter is asserted to let the user know that they should mute the sample rate converter to avoid any clicks or pops. The frequency response of the digital servo loop for "fast mode" and "slow mode" are shown in Figure 8.

The FIR filter is a 64-tap filter in the case of $f_{S\_OUT} \geq f_{S\_IN}$ and is $(f_{S\_IN}/f_{S\_OUT}) \times 64$ taps for the case when $f_{S\_IN} > f_{S\_OUT}$. The FIR filter performs its convolution by loading in the starting address of the RAM address pointer and the ROM address pointer from the digital servo loop at the start of the f_{S_OUT} period. The FIR filter then steps through the RAM by decrementing its address by 1 for each tap, and the ROM pointer increments its address by the $(f_{S\_OUT}/f_{S\_IN}) \times 2^{20}$ ratio for $f_{S\_IN} > f_{S\_OUT}$ or 2^{20} for $f_{S\_OUT} \geq f_{S\_IN}$. Once the ROM address rolls over, the convolution is completed. The convolution is performed for both the left and right channels, and the multiply accumulate circuit used for the convolution is shared between the channels.

The f_{S_IN}/f_{S_OUT} sample rate ratio circuit is used to dynamically alter the coefficients in the ROM for the case when $f_{S\_IN} > f_{S\_OUT}$. The ratio is calculated by comparing the output of an f_{S_OUT} counter to the output of an f_{S_IN} counter. If $f_{S\_OUT} > f_{S\_IN}$, the ratio is held at one. If $f_{S\_IN} > f_{S\_OUT}$, the sample rate ratio is updated if it is different by more than two f_{S_OUT} periods from the previous f_{S_OUT} to f_{S_IN} comparison. This is done to provide some hysteresis to prevent the filter length from oscillating and causing distortion.

OPERATING FEATURES

$\overline{\text{RESET}}$ and Power Down

When $\overline{\text{RESET}}$ is asserted low, the AD1895 will turn off the master clock input to the AD1895, MCLK_I, initialize all of its internal registers to their default values, and three-state all of the I/O pins. While $\overline{\text{RESET}}$ is active low, the AD1895 is consuming minimum power. For the lowest possible power consumption while $\overline{\text{RESET}}$ is active low, all of the input pins to the AD1895 should be static.

When $\overline{\text{RESET}}$ is deasserted, the AD1895 begins its initialization routine where all locations in the FIFO are initialized to zero, MUTE_OUT is asserted high, and any I/O pins configured as outputs are enabled. The mute control counter, which controls the soft mute attenuation of the input samples, is initialized to maximum attenuation, –127 dB (see Mute Control section).

When asserting $\overline{\text{RESET}}$ and deasserting $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ should be held low for a minimum of 5 MCLK_I cycles. During power-up the $\overline{\text{RESET}}$ should be held low until the power supplies have stabilized.

Power Supply and Voltage Reference

The AD1895 is designed for three-volt operation with five-volt input tolerance on the input pins. VDD_CORE is the three-volt supply that is used to power the core logic of the AD1895 and to drive the output pins. VDD_IO is used to set the input voltage tolerance of the input pins. In order for the input pins to be five-volt input tolerant, VDD_IO must be connected to a five-volt supply. If the input pins do not have to be five-volt input tolerant, then VDD_IO can be connected to VDD_CORE. VDD_IO should never be less than VDD_CORE. VDD_CORE and VDD_IO should be bypassed with 100 nF ceramic chip capacitors, as close to the pins as possible, to minimize power supply and ground bounce caused by inductance in the traces. A bulk aluminium electrolytic capacitor of 47 µF should also be provided on the same PC board as the AD1895.

Digital Filter Group Delay

The filter group delay is given by the equation:

$$GD = \frac{16}{f_{S\_IN}} + \frac{32}{f_{S\_IN}} \text{ seconds for } f_{S\_OUT} > f_{S\_IN}$$

$$GD = \frac{16}{f_{S\_IN}} + \left(\frac{32}{f_{S\_IN}}\right) \times \left(\frac{f_{S\_IN}}{f_{S\_OUT}}\right) \text{ seconds for } f_{S\_OUT} < f_{S\_IN}$$

Mute Control

When the MUTE_IN pin is asserted high, the MUTE_IN control will perform a soft mute by linearly decreasing the input data to the AD1895 FIFO to almost zero, –127 dB attenuation. When MUTE_IN is deasserted low, the MUTE_IN control will linearly decrease the attenuation of the input data to 0 dB. A 12-bit counter, clocked by LRCLK_I is used to control the mute attenuation. Therefore, the time it will take from the assertion of MUTE_IN to –127 dB full mute attenuation is 4096/LRCLK_I seconds. Likewise, the time it will take to reach 0 dB mute attenuation from the deassertion of MUTE_IN is 4096/LRCLK_I seconds.

Upon $\overline{\text{RESET}}$, or a change in the sample rate between LRCLK_I and LRCLK_O, the MUTE_OUT pin will be asserted high. The MUTE_OUT pin will remain asserted high until the digital servo loop's internal fast settling mode has completed. When the digital servo loop has switched to slow settling mode, the MUTE_OUT pin will deassert. While MUTE_OUT is asserted, the MUTE_IN pin should be asserted as well to prevent any major distortion in the audio output samples.

Master Clock

A digital clock connected to the MCLK_I pin or a fundamental or third overtone crystal connected between MCLK_I and MCLK_O can be used to generate the master clock, MCLK_I. The MCLK_I pin can be five-volt input-tolerant just like any of the other AD1895 input pins. A fundamental mode crystal can be inserted between MCLK_I and MCLK_O for master clock frequency generation up to 27 MHz. For master clock frequency generation with a crystal beyond 27 MHz it is recommended that the user use a third overtone crystal and to add an LC filter at the output of MCLK_O to filter out the fundamental, do not notch filter the fundamental. Please refer to your quartz crystal supplier for values for external capacitors and inductor components.

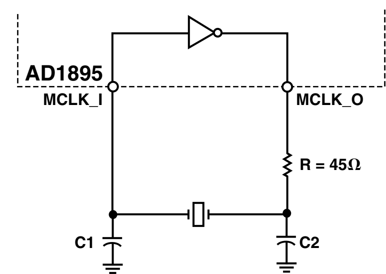


Figure 9a. Fundamental-Mode Circuit Configuration

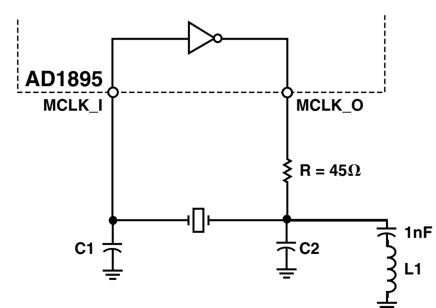


Figure 9b. Third-Overtone Circuit Configuration

There are, of course, maximum and minimum operating frequencies for the AD1895 master clock. The maximum master clock frequency at which the AD1895 is guaranteed to operate is 30 MHz. 30 MHz is more than sufficient to sample rate convert sampling frequencies of 192 kHz + 12%. The minimum required frequency for the master clock generation for the AD1895 depends upon the input and output sample rates. The master clock has to be at least 138 times greater than the maximum input or output sample rate.

Serial Data Ports—Data Format

The serial data input port mode is set by the logic levels on the SMODE_IN_0/1/2 pins. The serial data input port modes available are Left Justified, I²S and Right Justified (RJ), 16, 18, 20, or 24 bits as defined in Table I.

Table I. Serial Data Input Port Mode

SMODE_IN_[0:2]			Interface Format
2	**1**	**0**	
0	0	0	Left Justified
0	0	1	I²S
0	1	0	Undefined
0	1	1	Undefined
1	0	0	Right Justified, 16 Bits
1	0	1	Right Justified, 18 Bits
1	1	0	Right Justified, 20 Bits
1	1	1	Right Justified, 24 Bits

The serial data output port mode is set by the logic levels on the SMODE_OUT_0/1 and WLNGTH_OUT_0/1 pins. The serial mode can be changed to Left Justified, I²S, Right Justified or TDM as defined in the following table. The output word width can be set by using the WLNGTH_OUT_0/1 pins as shown in the Word Width table. When the output word width is less than 24 bits, dither is added to the truncated bits. The Right Justified serial data out mode assumes 64 SCLK_O cycles per frame, divided evenly for left and right.

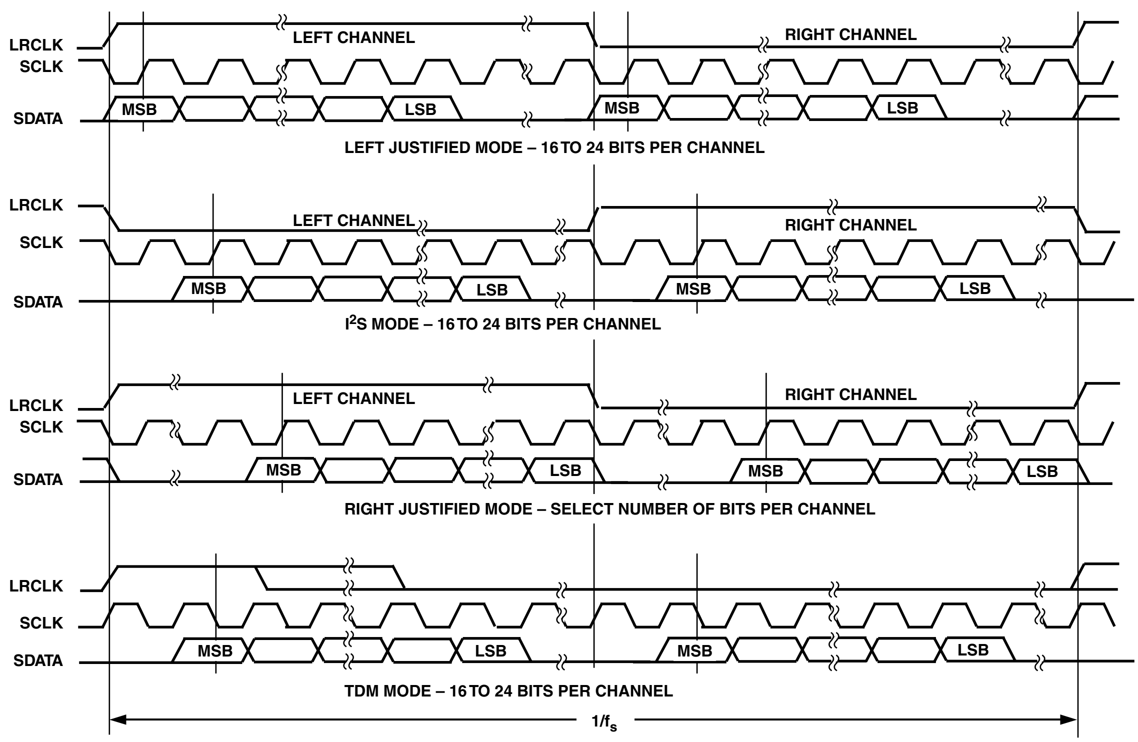
Table II. Serial Data Output Port Mode

SMODE_OUT_[0:2]		Interface Format
1	**0**	
0	0	Left Justified (LJ)
0	1	I²S
1	0	TDM Mode
1	1	Right Justified (RJ)

Table III. Word Width

WLNGTH_OUT_[0:1]		Word Width
1	**0**	
0	0	24 Bits
0	1	20 Bits
1	0	18 Bits
1	1	16 Bits

The following timing diagrams show the serial mode formats.



NOTES:
1. LRCLK NORMALLY OPERATES AT ASSOCIATIVE INPUT OR OUTPUT SAMPLE FREQUENCY (f_S)
2. SCLK FREQUENCY IS NORMALLY 64 × LRCLK EXCEPT FOR TDM MODE WHICH IS N × 64 × f_S, WHERE N = NUMBER OF STEREO CHANNELS IN THE TDM CHAIN, IN MASTER MODE N = 4

Figure 10. Input/Output Serial Data Formats

TDM MODE APPLICATION

In TDM mode, several AD1895s can be daisy-chained together and connected to the serial input port of a SHARC® DSP. The AD1895 contains a 64-bit parallel load shift register. When the LRCLK_O pulse arrives, each AD1895 parallel loads its left and right data into the 64-bit shift register. The input to the shift register is connected to TDM_IN while the output is connected to SDATA_O. By connecting the SDATA_O to the TDM_IN of the next AD1895, a large shift register is created which is clocked by SCLK_O.

The number of AD1895s that can be daisy-chained together is limited by the maximum frequency of SCLK_O, which is about 25 MHz. For example, if the output sample rate, f_S, is 48 kHz, up to eight AD1895s could be connected since $512 \times f_S$ is less than 25 MHz. In Master/TDM Mode, the number of AD1895s that can be daisy-chained is fixed to four.

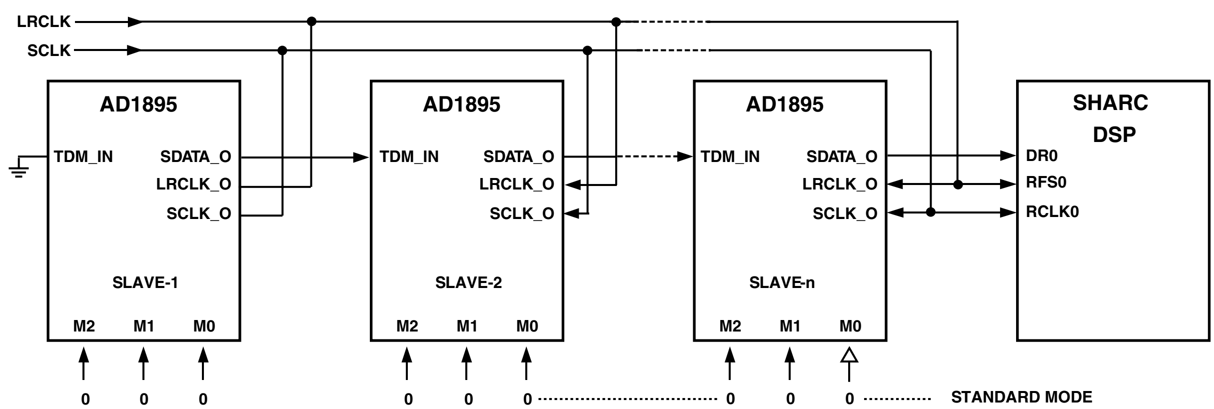


Figure 11. Daisy-Chain Configuration for TDM Mode (All AD1895s Being Clock-Slaves)

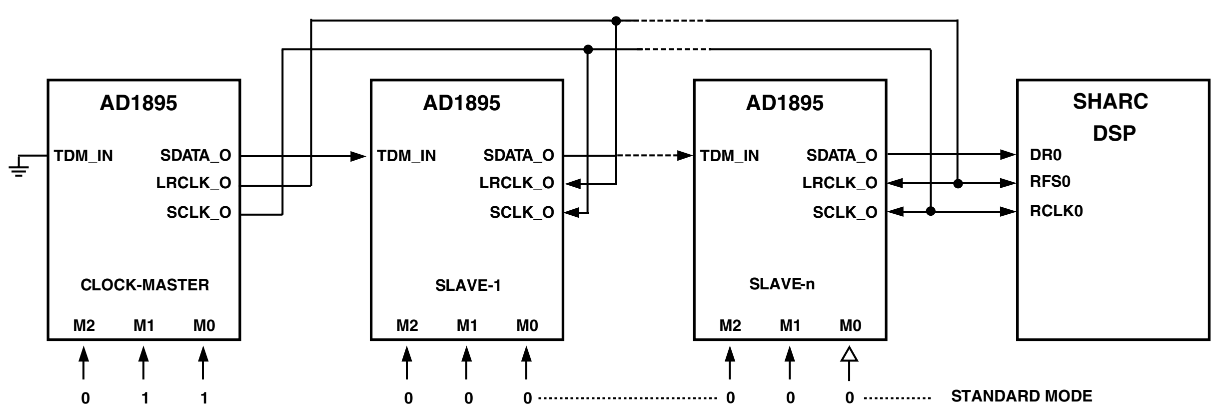


Figure 12. Daisy-Chain Configuration for TDM Mode (First AD1895 Being Clock-Master)

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Serial Data Port Master Clock Modes

Either of the AD1895 serial ports can be configured as a master serial data port. However, only one serial port can be a master while the other has to be a slave. In master mode, the AD1895 requires a $256 \times f_S$, 512 f_S or $768 \times f_S$ master clock (MCLK_I). For a maximum master clock frequency of 30 MHz, the maximum sample rate is limited to 96 kHz. In slave mode, sample rates up to 192 kHz can be handled.

When either of the serial ports is operated in master mode, the master clock is divided down to derive the associated left/right subframe clock (LRCLK) and serial bit clock (SCLK). The master clock frequency can be selected for 256, 512, or 768 times the input or output sample rate. Both the input and output serial ports will support master mode LRCLK and SCLK generation for all serial modes, Left Justified, I^2S, Right Justified, and TDM for the output serial port.

Table IV. Serial Data Port Clock Modes

MMODE_0/1/2			Interface Format
2	**1**	**0**	
0	0	0	Both Serial Ports are in Slave Mode
0	0	1	Output Serial Port is Master with $768 \times f_{S\_OUT}$
0	1	0	Output Serial Port is Master with $512 \times f_{S\_OUT}$
0	1	1	Output Serial Port is Master with $256 \times f_{S\_OUT}$
1	0	0	Undefined
1	0	1	Input Serial Port is Master with $768 \times f_{S\_IN}$
1	1	0	Input Serial Port is Master with $512 \times f_{S\_IN}$
1	1	1	Input Serial Port is Master with $256 \times f_{S\_IN}$

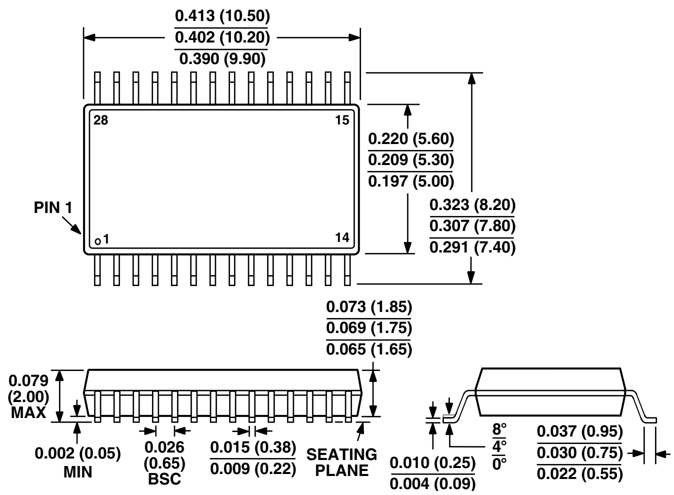
Bypass Mode

When the BYPASS pin is asserted high, the input data bypasses the sample rate converter and is sent directly to the serial output port. Dithering of the output data when the word length is set to less than 24 bits is disabled. This mode is ideal when the input and output sample rates are the same and LRCLK_I and LRCLK_O are synchronous with respect to each other. This mode can also be used for passing through non-AUDIO data since no processing is performed on the input data in this mode.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline Package (SSOP)
(RS-28)



AD1895–Revision History

Location	**Page**
Data Sheet changed from REV. 0 to REV. A.	
Changes to Specifications table	2

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