查询BD7966EKV供应商

Structure : Silicon Monolithic Integrated Circuit
Product Name : Power Driver for car CDs, DVDs

Device Name : **BD7966EKV**

Features :

- Single chip IC with drivers for Act (2 ch) / Loading (3 ch) / Sled (1 ch)
- Providing with 2 ports of control terminals enables controlling ON/OFF of the drivers for Act/Sled
- Built-in 3.3V regulator installed
- Employing the package: HTQFP64V equipped with a radiating metal on the mount side
- A built-in thermal shutdown circuit installed

<Loading Part>
- The LDCTL terminal is used to specify the output voltage.

<Sled Part>
- Supporting 2-phase stepping motors
- Supporting linear input
- PWM driving method achieves a high efficient drive.

<Actuator Part>
- Supporting 2-phase stepping motors
- Supporting linear input

○ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Unit
POWER MOS Power Supply Voltage	SLRNF	12	V
Pre-part and Pow-part Power Supply Voltage	VCC,AVM,LDVM	12	V
Power Dissipation	Pd	1.9*	W
Operating Temperature Range	Topr	-40 to 85	°C
Storage Temperature Range	Tstg	-55 to 150	°C

*ROHM standard board (size: 70×70 [mm], thickness: 1.6 [mm])

○ OPERATING CONDITIONS
(To determine a power supply voltage, the power dissipation must be taken into consideration.)

Parameter	Symbol	MIN	TYP	MAX	Unit
POWER MOS Power Supply Voltage	SLRNF	4.5	8	10	V
Pre-part and Pow-part Power Supply Voltage	VCC,AVM,LDVM	4.5	8	10	V

*VCC ≥ LDVM

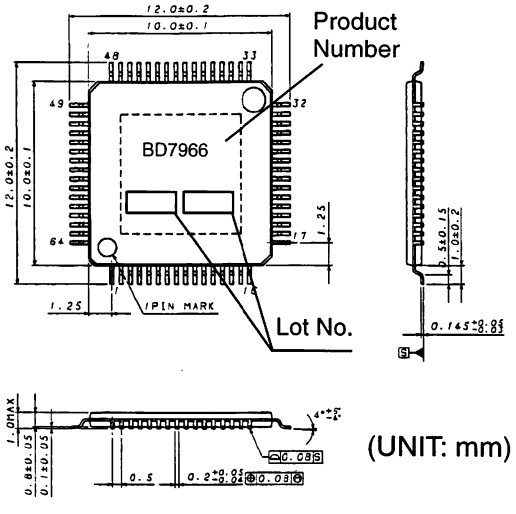
This product has not been checked for the strategic materials (or service) defined in the Foreign Exchange and Foreign Trade Control Low of Japan so that a verification work is required before exporting it.
Not designed for radiation resistance.

O ELECTRIC CHARACTERISTICS

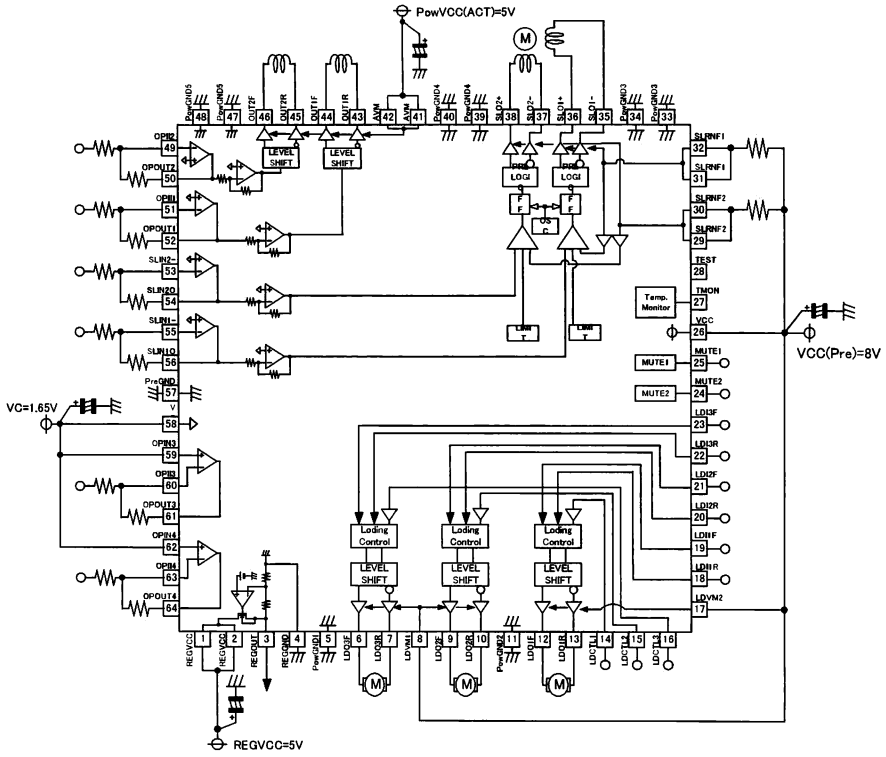
(Ta=25°C, VCC=POWVCC(LD,SL)=8V, AVM=5V, VC=1.65V, SLRNF=0.5Ω, unless otherwise noted.)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Circuit Current						
Quiescent Circuit Current 1	IQ1	-	26.5	38.4	mA	When VCC=REGVOC=PowVCC=8[V]
MUTE Circuit Current 1	IST1	-	19.5	28.3	mA	When VCC=REGVOC=PowVCC=8[V]
Feed Motor Driver Part						
Input Dead Band Width (one side)	VDZSL	5	30	55	MV	
Input/Output Gain	gmSL	0.77	1.0 (0.5)	1.23	A/V (V/V)	SLRNF=0.5Ω
Output ON Resistance (top side)	RONUSL	-	2.4	3.6	Ω	IL=500mA
Output ON Resistance (bottom side)	RONLSL	-	0.7	1.1	Ω	IL=500mA
Output Limit Current	ILIMSL	0.76	0.9 (0.45)	1.04	A (V)	SLRNF=0.5Ω
PWM Frequency	fosc	-	100	-	kHz	
Actuator Driver Part						
Output Offset Voltage	VOFFT	-50	0	50	mV	
Output Saturation Voltage H	VOHFT	-	0.45	0.8	V	IL=500mV
Output Saturation Voltage L	VOLFT	-	0.45	0.8	V	IL=500mV
Voltage Gain	GVFT	10.0	11.5	13.0	dB	
Bias Terminal Inflow Current	IBIAS	-	75	120	µA	VBIAS=2.5V
Operational Amplifier Part						
Input Offset Voltage	VOPOF	-5	0	+5	mV	
Input Bias Current	IOPIB	-	-	300	nA	
Common Mode Input Voltage Range	VOPICM	0.3	-	VCC-1.2	V	
Maximum Output Source Current	ISOURCE	500	800	-	µA	
Maximum Output Sink Current	ISINK	2	-	-	mV	
Slew Rate	SR	-	0.8	-	V/µs	
Loading Driver Part						
Input Terminal Inflow Current	IINL	-	87	130	µA	LDIN=5V
LDCTL Terminal Outflow Current	ILDC1	-	-	0.5	mA	LDCTL=5V
Output Offset Voltage	VOFLD	-	0	-	mV	
Output Saturation Voltage H	VOHLD	-	1.1	1.4	V	IL=500mA
Output Saturation Voltage H	VOLLD	-	0.45	0.8	V	IL=-500mA
Voltage Gain	GVLD	7.5	9.0	10.5	dB	LDCTL=1V
Regulator						
REG Output Voltage	VPEG	3.13	3.3	3.47	V	IL=200mA
MUTE						
Input High-level Voltage	VIH	2.0	-	-	V	
Input Low-level Voltage	VIL	-	-	0.5	V	
Input High-level Current	IIH	-	180	270	uA	VIMUTE=5V
Input Low-level Current	IIL	-10	0	10	uA	VIMUTE=0V

O OUTLINE DIMENSIONS, SYMBOLS



O APPLICATION CIRCUIT DIAGRAM



O PIN Description

No.	Symbol	Description	No.	Symbol	Description
1	REGVCC	Power supply for regulator part PowNMOS	64	OPOUT4	OP output 4
2	REGVCC	Power supply for regulator part PowNMOS	63	OPII4	OP inverted output terminal 4
3	REGOUT	Regulator output	62	OPIN4	OP non-inverted output terminal 4
4	REGGND	Regulator part GND	61	OPOUT3	OP output 3
5	PowGND1	Loading part power GND1	60	OPII3	OP inverted output terminal 3
6	LDO3F	Loading part Ch3 forward output terminal	59	OPIN3	OP non-inverted output terminal 3
7	LDO3R	Loading part Ch3 reverse output terminal	58	VC	Bias input terminal
8	LDVM1	Loading part power supply 1	57	PreGND	Pre part GND
9	LDO2F	Loading part Ch2 forward output terminal	56	SLIN1O	SLIN1 pre-stage OP output
10	LDO2R	Loading part Ch2 reverse output terminal	55	SLIN1-	SLIN1 pre-stage OP inverted input terminal
11	PowGND2	Loading part power GND 2	54	SLIN2O	SLIN2 pre-stage OP output
12	LDO1F	Loading part Ch1 forward output terminal	53	SLIN2-	SLIN2 pre-stage OP inverted input terminal
13	LDO1R	Loading part Ch1 reverse output terminal	52	OPOUT1	BTL part Ch1 pre-stage OP output
14	LDCTL1	Loading part output voltage setting terminal CH1	51	OPII1	BTL part Ch1 pre-stage OP inverted input terminal
15	LDCTL2	Loading part output voltage setting terminal CH2	50	OPOUT2	BTL part Ch2 pre-stage OP output
16	LDCTL3	Loading part output voltage setting terminal CH3	49	OPII2	BTL part Ch2 pre-stage OP inverted input terminal
17	LDVM2	Loading part power supply 2	48	PowGND5	Actuator part power GND5
18	LDI1R	Loading part Ch1 reverse input terminal	47	PowGND5	Actuator part power GND5
19	LDI1F	Loading part Ch1 forward input terminal	46	OUT2F	BTL part Ch2 non-inverted output terminal
20	LDI2R	Loading part Ch2 reverse input terminal	45	OUT2R	BTL part Ch2 inverted output terminal
21	LDI2F	Loading part Ch2 forward input terminal	44	OUT1F	BTL part Ch1 non-inverted output terminal
22	LDI3R	Loading part Ch3 reverse input terminal	43	OUT1R	BTL part Ch1 inverted output terminal
23	LDI3F	Loading part Ch3 forward input terminal	42	AVM	Actuator part power supply
24	MUTE2	MUTE terminal 2	41	AVM	Actuator part power supply
25	MUTE1	MUTE terminal 1	40	PowGND	Actuator part power GND4
26	VCC	Pre part power supply	39	PowGND	Actuator part power GND4
27	TMON	Temperature monitor	38	SLO2+	Feed part Ch2 positive output terminal
28	TEST	TEST	37	SLO2-	Feed part Ch2 negative output terminal
29	SLRNF2	Feed part current detection terminal 2	36	SLO1+	Feed part Ch1 positive output terminal
30	SLRNF2	Feed part current detection terminal 2	35	SLO1-	Feed part Ch1 negative output terminal
31	SLRNF1	Feed part current detection terminal 1	34	PowGND3	Feed part power GND3
32	SLRNF1	Feed part current detection terminal 1	33	PowGND3	Feed part power GND3

O CAUTIONS ON USE

(1) Bypass Capacitor
Between the power supplies, connect a bypass capacitor (0.1μF) closely to the IC pins. At the position close to the power part power supply terminal, the capacitor having a large capacitance and a small ESR (approx. 10μF) should be attached in order to reduce the impedance of the power supply.

(2) Short-circuit between output-power supply, output-GND, or output terminals
Short-circuits between output pin-VCC, output pin-GND, or output terminals (load short) must be avoided. Make sure that the ICs are installed on the board in proper directions. Mounting the ICs in improper directions may damage them or produce smoke.

(3) TEST terminal
The TEST terminal is pulled down inside the IC, so that it should be set open or shorted to GND for use.

(4) About absolute maximum ratings
Exceeding the absolute maximum ratings, such as the applied voltage or the operating temperature range, may cause permanent device damage. As these cases cannot be limited to the broken short mode or the open mode, if a special mode where the absolute maximum ratings may be exceeded is assumed, it is recommended to take mechanical safety measures such as attaching fuses.

(5) About power supply lines
As a measure against the back current regenerated by a counter electromotive force of the motor, a capacitor to be used as a regenerated-current path can be installed between the power supply and GND and its capacitance value should be determined after careful check that any problems, for example, a leak capacitance of the electrolytic capacitor at low temperature, are not found in various characteristics.

(6) About GND potential
The electric potential of the GND terminal must be kept lowest in the circuitry at any operation states.

(7) About thermal design
With consideration of the power dissipation (Pd) under conditions of actual use, a thermal design provided with an enough margin should be done.

(8) About operations in a strong electric field
When used in a strong electric field, note that a malfunction may occur.

(9) ASO
When using this IC, the output Tr must be set not to exceed the values specified in the absolute maximum ratings and ASO.

(10) Thermal shutdown circuit (Thermal shutdown: TSD)
This IC incorporates a thermal shutdown circuit (TSD circuit). When the chip temperature reaches the value shown below, the coil output to the motor will be set to open.
The thermal shutdown circuit is designed only to shut off the IC from a thermal runaway and not intended to protect or guarantee the entire IC functions.
Therefore, users cannot assume that the TSD circuit once activated can be used continuously in the subsequent operations.

TSD ON Temperature [°C] (typ.)	Hysteresis Temperature [°C] (typ.)
175	25

(11) About earth wiring patterns
When a small signal GND and a large current GND are provided, it is recommended that the large current GND pattern and the small signal GND pattern should be separated and grounded at a single point of the reference point of the set in order to prevent the voltage of the small signal GND from being affected by a voltage change caused by the resistance of the pattern wiring and the large current. Make sure that the GND wiring patterns of the external components will not change, too.

(12) This IC is a monolithic IC which has a P^+ isolations and P substrate to isolate elements each other. This P layer and an N layer in each element form a PN junction to construct various parasitic elements. Due to the IC structure, the parasitic elements are inevitably created by the potential relationship. Activation of the parasitic elements can cause interference between circuits and may result in a malfunction or, consequently, a fatal damage. Therefore, make sure that the IC must not be used under conditions that may activate the parasitic elements, for example, applying the lower voltage than

the ground level (GND, P substrate) to the input terminals.
In addition, do not apply the voltage to input terminals without applying the power supply voltage to the IC. Also while applying the power supply voltage, the voltage of each input terminal must not be over the power supply voltage, or within the guaranteed values in the electric characteristics.

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