TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

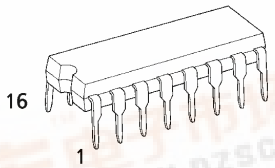
TC74HC597AP, TC74HC597AF

8 – BIT LATCH / SHIFT REGISTER

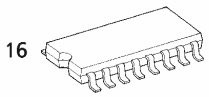
The TC74HC597A is a high speed CMOS 8-BIT PARALLEL-IN / SERIAL-IN SERIAL-OUT LATCH / SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of an 8-bit data register feeding an 8-bit shift register. The parallel data on the A~H inputs is stored in the input register on the positive going transition of RCK. When the $\overline{SLOAD}$ input is held low, the input register data is passed into the shift registers. When $\overline{SLOAD}$ input is held high, the serial data input (SI) is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK. A direct clear input ($\overline{SCLR}$) sets the 8-bit shift register to zoro.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

- High Speed ····· f_{MAX} = 60MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA (Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS597

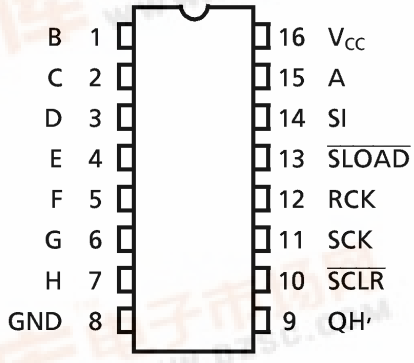


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S. R. is celeared to "L"
X	X	H	L	X	Input register data is stored into S. R.
L	↓	H	H	X	First stage of S. R. become "L". Other stages store the data of previous stage, respectively.
H	↓	H	H	X	First stage of S. R. become "H". Other stages store the data of previous stage, respectively.
X	↑	H	H	X	State of S. R. is not changed.
X	X	X	X	↓	Input data on A~H line is stored into input register.
X	X	X	X	↑	Storage register stage is not changed.

X : Don't Care

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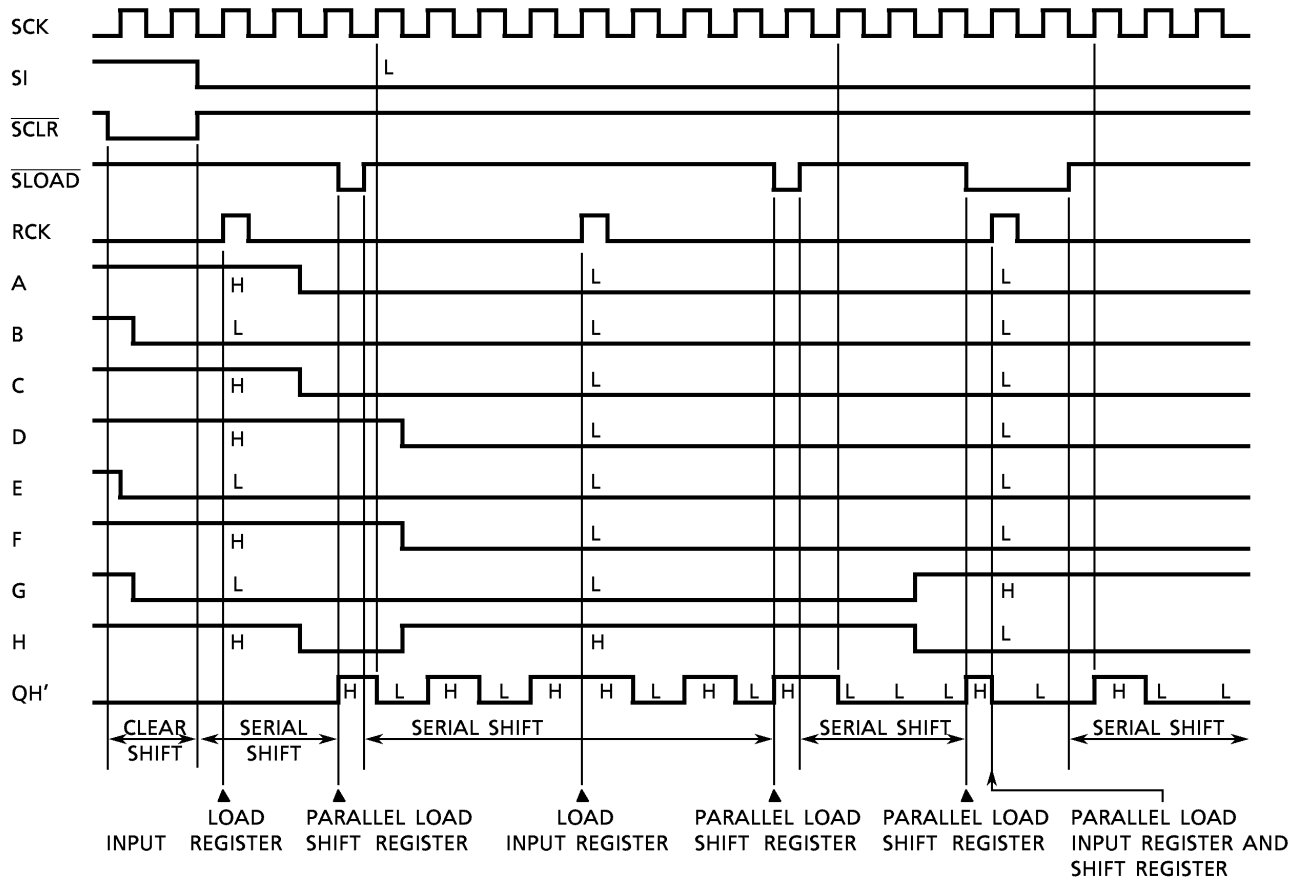
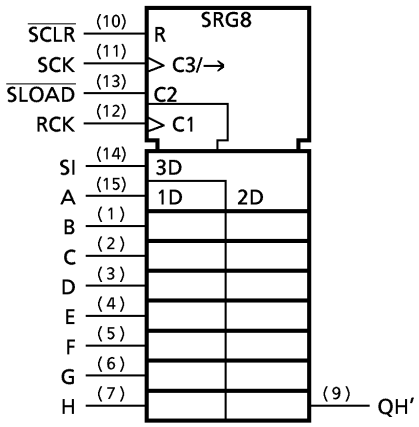
TIMING CHART



IEC LOGIC SYMBOL



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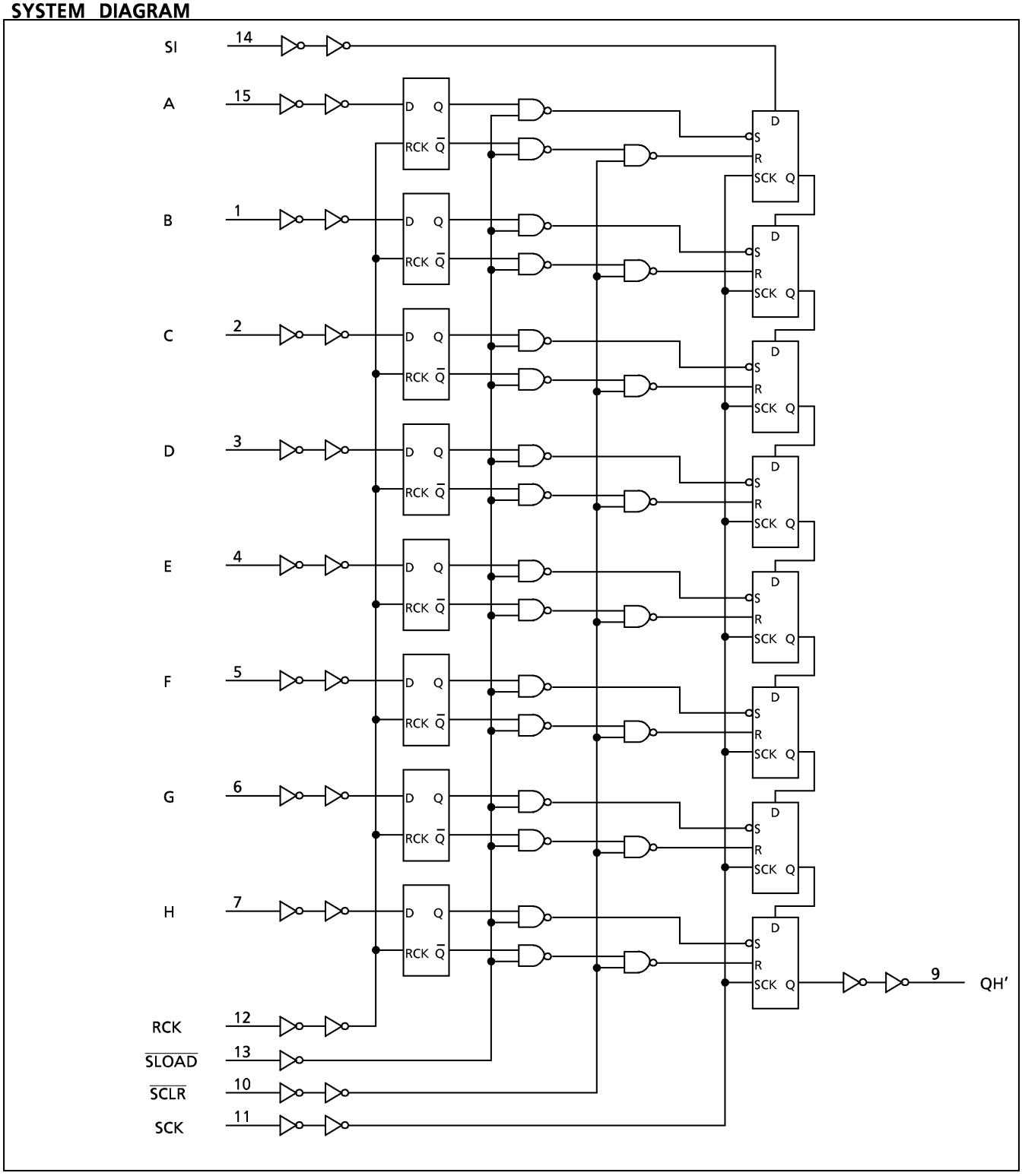
SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor of −10mW/°C should be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0 4.5 6.0	− − −	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Minimum Pulse Width ($\overline{SLOAD}$)	$t_{W(L)}$		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Minimum Set-up Time (RCK − $\overline{SLOAD}$)	t_s		2.0 4.5 6.0	− − −	100 20 17	125 25 21	
Minimum Set-up Time (SI − SCK)	t_s		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Minimum Set-up Time (PI − RCK)	t_s		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Minimum Hold Time	t_h		2.0 4.5 6.0	− − −	0 0 0	0 0 0	
Minimum Removal Time ($\overline{SCLR}$, $\overline{SLOAD}$)	t_{rem}		2.0 4.5 6.0	− − −	75 15 13	95 19 16	
Clock Frequency	f		2.0 4.5 6.0	− − −	6 30 35	5 24 28	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	5	8	ns
Propagation Delay Time (SCK − QH')	t_{pLH} t_{pHL}		−	16	25	
Propagation Delay Time ($\overline{SCLR}$ − QH')	t_{pHL}		−	20	32	
Propagation Delay Time ($\overline{SLOAD}$ − QH')	t_{pLH} t_{pHL}		−	18	30	
Propagation Delay Time (RCK − QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$ = "L"	−	25	37	
Clock Frequency	f_{MAX}		30	59	−	MHz

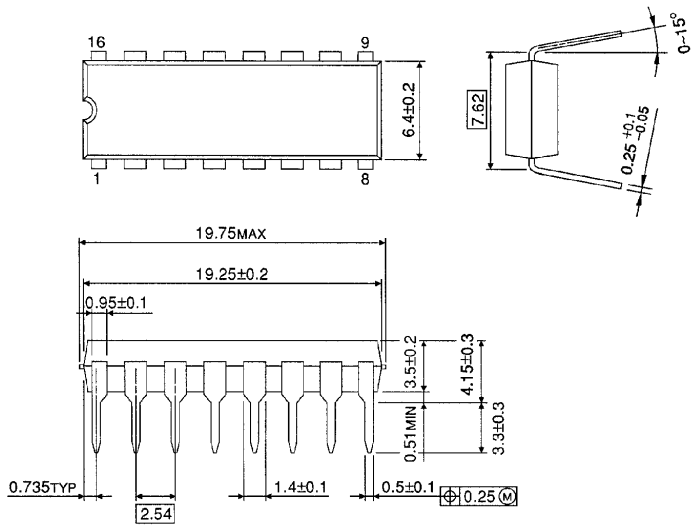
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	− − −	32 8 7	75 15 13	− − −	95 19 16	ns
Propagation Delay Time (SCK−QH')	t_{pLH} t_{pHL}		2.0 4.5 6.0	− − −	78 20 16	145 29 25	− − −	180 36 31	
Propagation Delay Time ($\overline{SCLR}$−QH')	t_{pHL}		2.0 4.5 6.0	− − −	90 24 20	175 35 30	− − −	220 44 37	
Propagation Delay Time ($\overline{SLOAD}$−QH')	t_{pLH} t_{pHL}		2.0 4.5 6.0	− − −	80 22 18	175 35 30	− − −	220 44 37	
Propagation Delay Time (RCK−QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$ = "L"	2.0 4.5 6.0	− − −	112 30 24	210 42 36	− − −	265 53 45	
Maximum Clock Frequency	f_{MAX}		2.0 4.5 6.0	6 30 35	12 48 50	− − −	5 24 28	− − −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	60	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

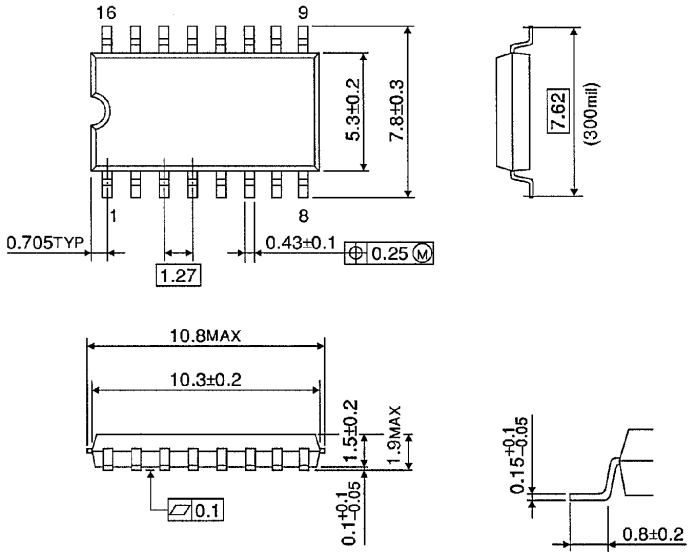
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)