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FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12536-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89940 Series

MB89943/P945/PV940

■ OUTLINE

The MB89940 series is specially designed for automotive instrumentation applications. It features a combination of two PWM pulse generators and four high-drive-current outputs for controlling a stepping motor. It also contains two analog inputs, two PWM pulse generators and 10-digit LCD controller/driver for various sensor/indicator devices. The MB89940 series is manufactured with high performance CMOS technologies and packaged in a 48-pin QFP.

■ FEATURES

- 8-bit core CPU; 4 MHz system clock (8 MHz external, 500 ns instruction cycle)
- 21-bit watchdog timer
- Clock generator/controller
- 16-bit interval timer
- Two PWM pulse generators with four high-drive-current outputs
- Two-channel 8-bit A/D converter
- Three external interrupt
- Low supply voltage reset
- External voltage monitor interrupt
- Two more PWM pulse generators for controlling indicator devices
- 4-common 17-segment LCD driver/controller
- Package; 48-pin plastic QFP, 48-pin ceramic MQFP

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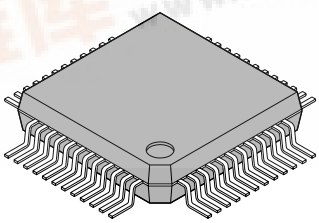
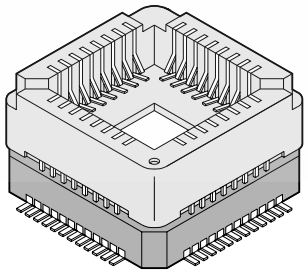
■ PACKAGE

48-pin Plastic QFP



(FPT-48P-M16)

48-pin Ceramic MQFP



(MQP-48C-P01)

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- 5.0 V single power supply (V_{PP} required for MB89P945)
- 0.8 µm CMOS technology (MB89PV940 and MB89P945)
- 0.5 µm CMOS technology (MB89943)
- On-chip voltage regulator for internal 3.0 V power supply (MB89943)

■ PRODUCT LINEUP

Part number / Item	MB89943	MB89P945	MB89PV940
Classification	Mass-produced products (mask ROM products)	One-time PROM	Piggyback
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM)	32 K × 8 bits (external on piggyback)
RAM size	512 × 8 bits		1 K × 8 bits
CPU functions	The number of instructions: 136 Instruction cycle: 0.5 µs*1@8 MHz Interrupt response time: 4.0 µs*1@8 MHz Multiply instruction time: 19 instruction cycles Divide instruction time: 21 instruction cycles Direct addressing memory-to/from-register data transfer: 7 instruction cycles		
Ports	Output: 5-bit N-ch open-drain Input/Output: Two 8-bit CMOS schmitt I/Os and 8-bit CMOS I/Os		
Timebase timer	21 bits Interrupt interval: 1 ms, 4.1 ms, 32.8 ms or 524.3 ms		
8-bit/16-bit timer	Can be used as two 8-bit timers or one 16-bit timer Operation clock: 1 µs, 16 µs, 256 µs or external *1		
Watchdog Reset	Reset interval: Approx. 524 ms to 1049 ms		
Stepping motor controller	Two 8-bit PWM pulse generators Synchronized 4-channel high current output Operation clock: 250 ns, 500 ns, 1 µs or 4 µs*1		
8-bit PWM timers	Two 8-bit PWM timers		
External interrupt	3 channels, selective positive edge or negative edge trigger		
A/D converter	8-bit resolution, two-channel input Conversion time: 44 instruction cycles for A/D conversion, 12 instruction cycles for sense mode operation		
LCD controller	4-common and 17-segment outputs Number of outputs programmable		
Low supply voltage reset	Autonomous reset when low supply voltage Reset voltage: 3.3 V, 3.6 V, 4.0 V		
External voltage monitor interrupt	Interrupts when voltage at external pin is lower than the reference voltage		
Standby modes	Stop mode and sleep mode		
Operating voltage*2	3.5 V to 5.5 V		

(Continued)

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Part number / Item	MB89943	MB89P945	MB89PV940
Process	CMOS		
External EPROM			MBM27C256A-20TVM

*1: Execution times and clock cycle times are dependent on the use of MCU.
*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.") In the case of the MB89PV940, the voltage varies with the vestrictions of the EPROM for use.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89943 MB89P945	MB89PV940
FPT-48P-M16	○	×
MQP-48C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Prior to evaluating/developing the software for the MB89940 series, please check the differences between the product types.

- RAM/ROM configurations are dependent on the product type.
- If the bottom address of the stack is set to the upper limit of the RAM address, it should be relocated when changing the product type.

2. Power Dissipation

- For the piggyback product, add the power dissipation of the EEPROM on the piggyback.
- The power dissipation differs between the product types.

3. Technology

The mask ROM product is fabricated with a 0.5 µm CMOS technology whereas the other products with 0.8 µm CMOS technology.

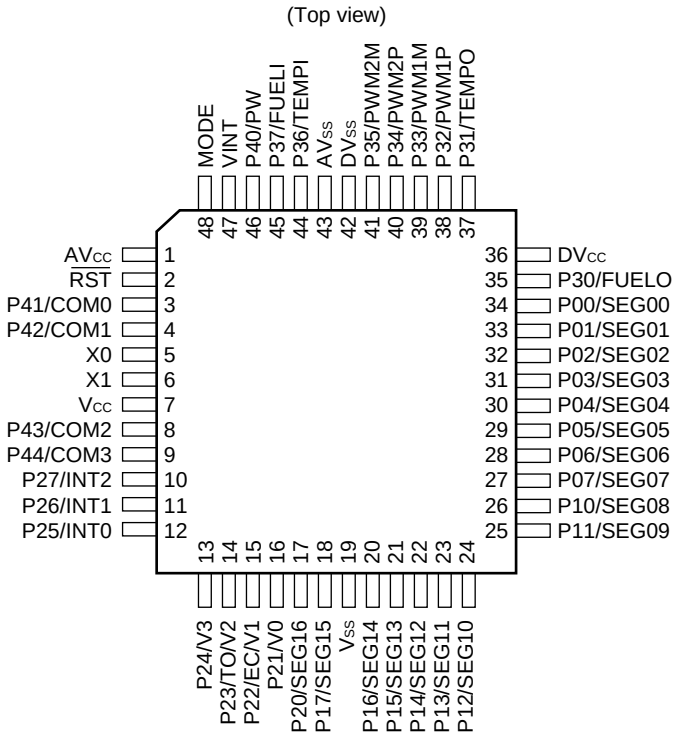
Also the mask ROM product contains the on-chip voltage regulator for the internal 3.0 power supply. For details, refer to *MB89940 Series Hardware Manual*.

4. Mask Option

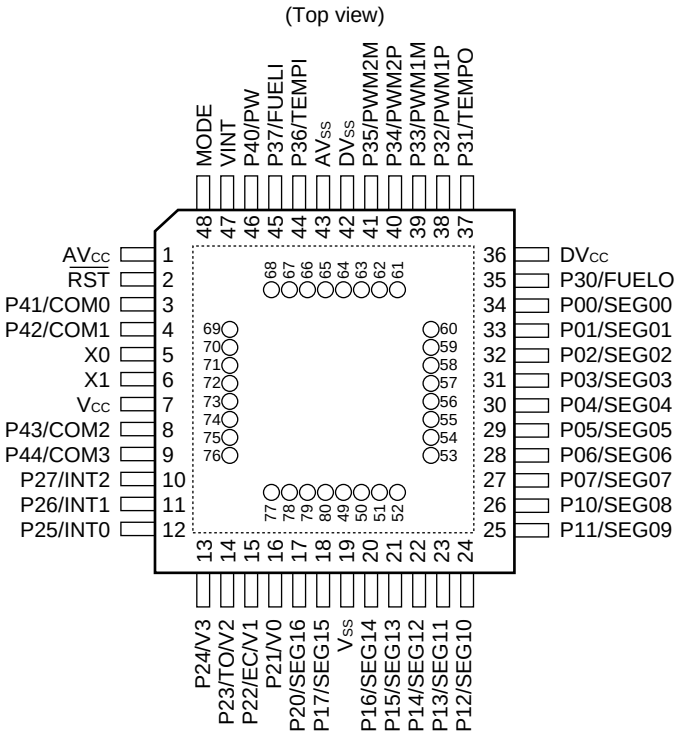
Functions that can be selected as options and how to designate these options vary by the product.
Before using options check section “■ Mask Options.”

- No options are available for the piggyback product.
- The power-on reset and reset output options are always activated with the mask ROM product.
- Pull-up option must not be specified with the pins used as LCD outputs.

■ PIN ASSIGNMENT



(FPT-48P-M16)



(MQP-48C-P01)

- **Pin assignment on package top (MB89PV940 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	A15	57	N.C.	65	O4	73	OE
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	CE	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{SS}	72	N.C.	80	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
5	5	X0	A	These pins are used for crystal oscillation. X0 and X1 can be directly connected to a crystal oscillator. When the oscillation clock is provided to X0 externally, X1 should be left open.
6	6	X1		
48	48	MODE	B	The mode input is used for entering the MPU into the test mode. In user applications, MODE is connected to V_{SS}.
2	2	$\overline{RST}$	C	Applying a reset pulse to this pin forces the MPU to enter the initial state. $\overline{RST}$ is active low and drives low state when an internal reset occurs. Reset pulses of the duration less than the minimum pulse width may cause the MCU to enter undefined states.
34 to 27	34 to 27	P00/SEG00 to P07/SEG07	H	These pins have two functions. Their functions can be switched between Port 0 and LCD segment signal outputs by setting the internal registers of the LCD controller.
26 to 20, 18	26 to 20, 18	P10/SEG08 to P17/SEG15	J	These pins have two functions. Their functions can be switched between Port 1 and LCD segment signal outputs by setting the internal registers of the LCD controller.
17	17	P20/SEG15	I	This pin can be used as the bit 0 of Port 2 or an LCD segment signal output by setting the internal register of the LCD controller.
16	16	P21/V0	F	This pin is the bit 1 of Port 2. This pin can also be used for an external LCD bias voltage input.
15	15	P22/EC/V1	F	This pin can be used as the bit 2 of Port 2 or the external clock input for the interval timer. This pin can also be used for an external LCD bias voltage input.
14	14	P23/TO/V2	F	This pin can be used as the bit 3 of Port 2 or the output for the interval timer. Its function can be switched by setting the internal register of the interval timer. This pin can also be used for an external LCD bias voltage input.
13	13	P24/V3	F	This pin can be used as the bit 4 of Port 2 or an external LCD bias voltage input.
12, 11, 10	12, 11, 10	P25/INT0 to P27/INT2	E	These pins are used for Port 2. They can also be used for external interrupt inputs.
35	35	P30/FUELO	D	This pin can be used for the bit 0 of Port 3 or the output from PWM3. The function of this pin can be switched by setting the internal register of PWM3.

*1: FPT-48P-M16
*2: MQP-48C-P01

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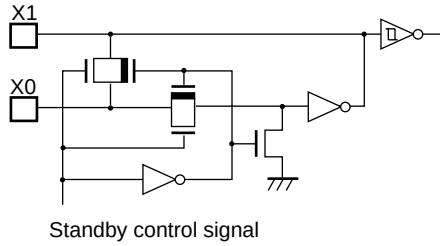
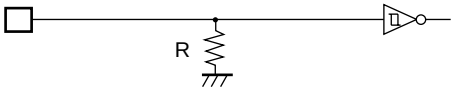
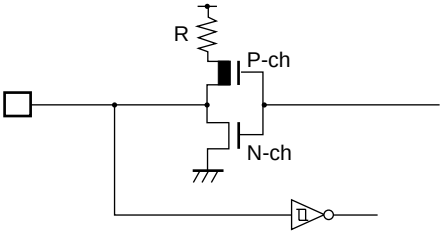
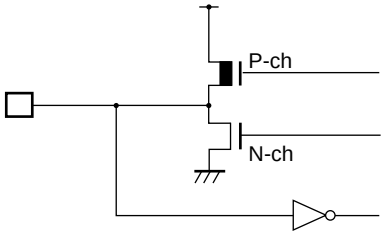
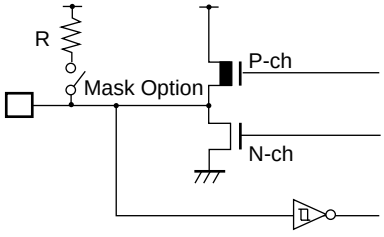
Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
37	37	P31/TEMPO	G	This pin can be used for the bit 1 of Port 3 or the output from PWM4. The function of this pin can be switched by setting the internal register of PWM4. This output has a high drive-current capability.
38, 39	38, 39	P32/PWM1P, P33/PWM1M	G	These pins are the pair of high-current driver outputs for one of two motor coils. They can be also used for the bits 2 and 3 of Port 3 by setting the internal register of the stepper motor controller.
40, 41	40, 41	P34/PWM2P, P35/PWM2M	G	These pins are the pair of high-current driver outputs for one of two motor coils. They can be also used for the bits 4 and 5 of Port 3 by setting the internal register of the stepper motor controller.
44	44	P36/TEMPI	M	This analog input is connected to channel 1 of the A/D converter. It can also be used for the bit 6 of Port 3 when this A/D input enable register bit is set to ‘0’.
45	45	P37/FUELI	M	This analog input is connected to channel 0 of the A/D converter. It can also be used for the bit 7 of Port 3 when this A/D input enable register bit is set to ‘0’.
46	46	P40/PW	L	This pin has two functions. When this pin is used as an open-drain output of Port 4, the external voltage monitor reset should be in the power down mode. When it is used as the PW input of external voltage monitor reset, the corresponding bit of the port data register should be set to ‘1’.
3, 4 8, 9	3, 4 8, 9	P41/COM0 to P44/COM3	K	These pins are the LCD common signal outputs. When LCD is not used, these pins can be also used for Port 4.
47	47	VINT	—	An external capacitor should be connected to this pin for stabilizing the internal 3.0 V power supply. For MB89PV940 and MB89P945, this pin should be left open.
7	7	V_{CC}	—	V_{CC}
19	19	V_{SS}	—	V_{SS}
1	1	AV_{CC}	—	The power supply pin for the analog circuit The same voltage should be applied as V_{CC}.
43	43	AV_{SS}	—	The power supply pin for the analog circuit The same voltage should be applied as V_{SS}.
36	36	DV_{CC}	—	The dedicated power supply pin for the high-current driver output The same voltage should be applied as V_{CC}.
42	42	DV_{SS}	—	The dedicated power supply pin for the high-current driver output The same voltage should be applied as V_{SS}.

*1: FPT-48P-M16
*2: MQP-48C-P01

- **External EPROM pins (MB89PV940 only)**

Pin no.	Pin name	I/O	Function
49 50 51 52 53 54 55 58 59 60	A15 A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
61 62 63 65 66 67 68 69	O1 O2 O3 O4 O5 O6 O7 O8	I	Data input pins
70	CE	O	ROM chip enable pin Outputs “H” during standby.
71	A10	O	Address output pin
73	OE	O	ROM output enable pin Outputs “L” at all times.
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pin
80	V_{CC}	O	EPROM power supply pin
64	V_{SS}	O	Power supply (GND) pin
56 57 72 74	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillator I/O With feedback resistor of approx. 2 MΩ.
B		• Schmitt-trigger input (Pull-down resistance only for MB89943)
C		• Open-drain output with pull-up resistor (Approx. 50 kΩ). • Schmitt-trigger input • Hysteresis input
D		• CMOS I/O
E		• CMOS I/O (Schmitt trigger) • Pull-up resistor optional

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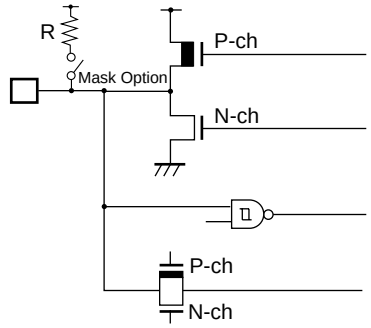
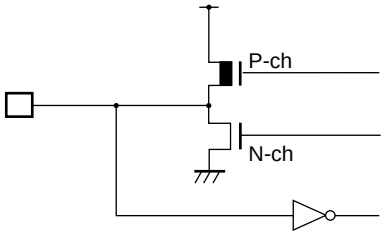
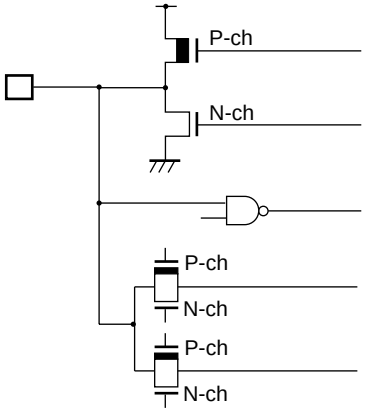
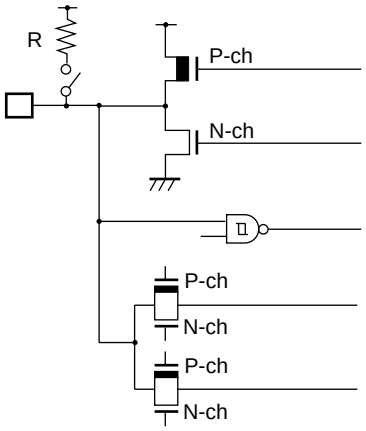
Type	Circuit	Remarks
F		• CMOS I/O (Schmitt trigger) • External bias input • Pull-up resistor optional
G		• CMOS I/O (High output current)
H		• CMOS I/O • LCD controller/driver output
I		• CMOS I/O • LCD controller/driver output • Pull-up resistor optional • Hysteresis input

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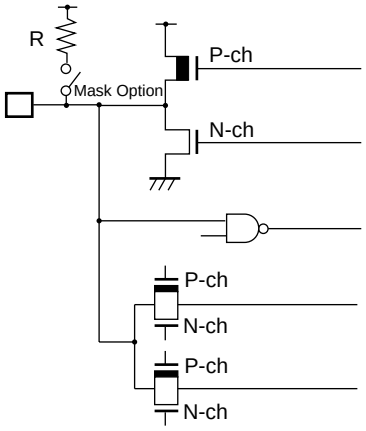
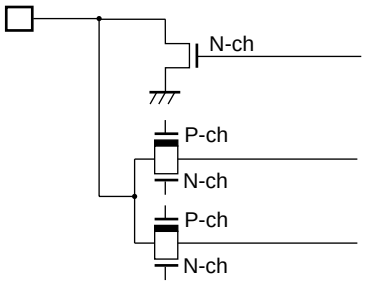
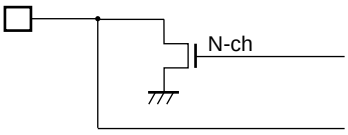
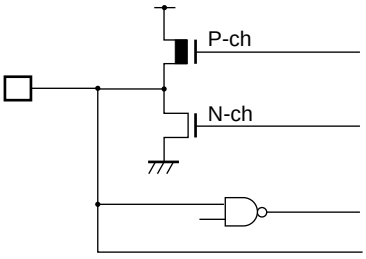
Type	Circuit	Remarks
J		• CMOS I/O • LCD controller/driver output • Pull-up resistor optional (Except P11/SEG09, P10/SEG08)
K		• N-ch open-drain output • LCD controller/driver output
L		• N-ch open-drain output • Analog input
M		• CMOS I/O • Analog input

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

The VINT pin of MB89PV940 and MB89P945 is the only exception.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

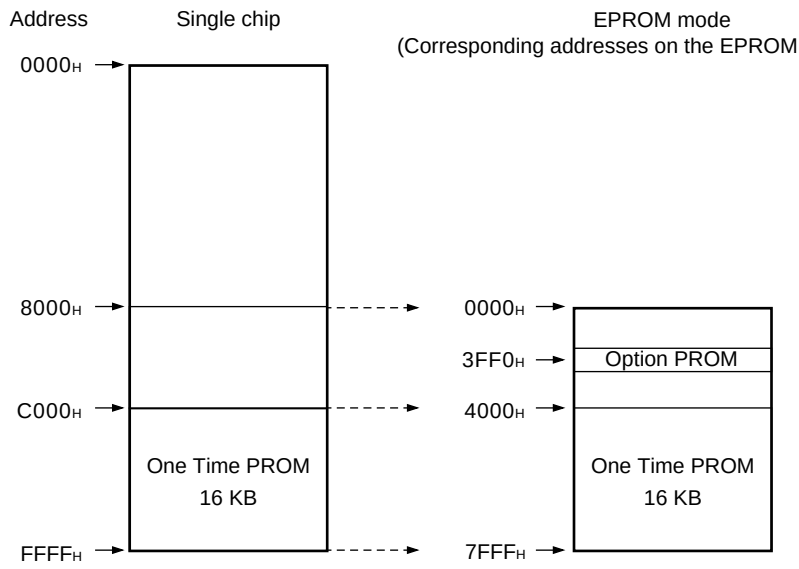
Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

■ PROGRAMMING TO THE EPROM ON THE MB89P945

1. Programming MB89P945

Using the EPROM adapter (provided by Fujitsu) and a standard EPROM programmer, user-defined data can be written into the OTPROM and option PROM. The EPROM programmer should be set to MB27C256A-20TVM and electro-signature mode should not be used. When programming the data, the internal addresses are mapped as follows.

2. Memory Space

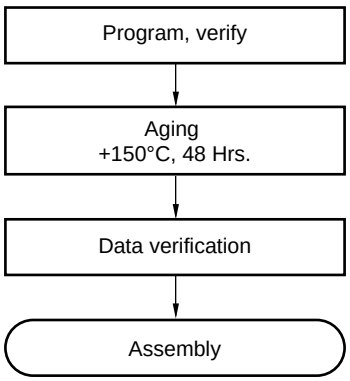


3. EPROM Programmer Socket Adapter

Please contact Fujitsu for socket adapters for the MB89P945 and the EPROM on the MB89PV940.

4. Screening MB89P945

It is recommended that high-temperature aging is performed on the MB89P945 prior to the assembly.



5. Setting OTPROM Options

For MB89P945, mask options are described in the internal option PROM area. The table below shows the bit map of the option PROM. The option data can be written by a standard EPROM programmer.

- **OTPROM option bit map**

PROM Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Unused	Unused	Unused	Reserved	Reset output 1: Active 0: Inactive	Power-on reset 1: Active 0: Inactive	Oscillation stabilization time 11: 2^{18} Tosc 10: 2^{17} Tosc 01: 2^{14} Tosc	
3FF1H	P17 Pull-up 1: Inactive 0: Active	P16 Pull-up 1: Inactive 0: Active	P15 Pull-up 1: Inactive 0: Active	P14 Pull-up 1: Inactive 0: Active	P13 Pull-up 1: Inactive 0: Active	P12 Pull-up 1: Inactive 0: Active	Unused	Unused
3FF2H	P27 Pull-up 1: Inactive 0: Active	P26 Pull-up 1: Inactive 0: Active	P25 Pull-up 1: Inactive 0: Active	P24 Pull-up 1: Inactive 0: Active	P23 Pull-up 1: Inactive 0: Active	P22 Pull-up 1: Inactive 0: Active	P21 Pull-up 1: Inactive 0: Active	P20 Pull-up 1: Inactive 0: Active
3FF3H	Unused	Unused	Unused	Low volt. PDX bit	Low volt. S1 bit	Low volt. S0 bit	Low volt. LVE bit	Low volt. 1: Register active 0: Option active
3FF4H	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused
3FF5H	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused
3FF6H	Unused	Unused	Unused	Unused	Unused	Unused	Unused	Unused

Notes: Default values are all ‘1’.
Tosc: One oscillation clock cycle time
When the bit 0 of “3FF3H” is “0”, it activates the option setting for the Low Voltage Reset Control register. When this option is activated, software setting in the register has no effect.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

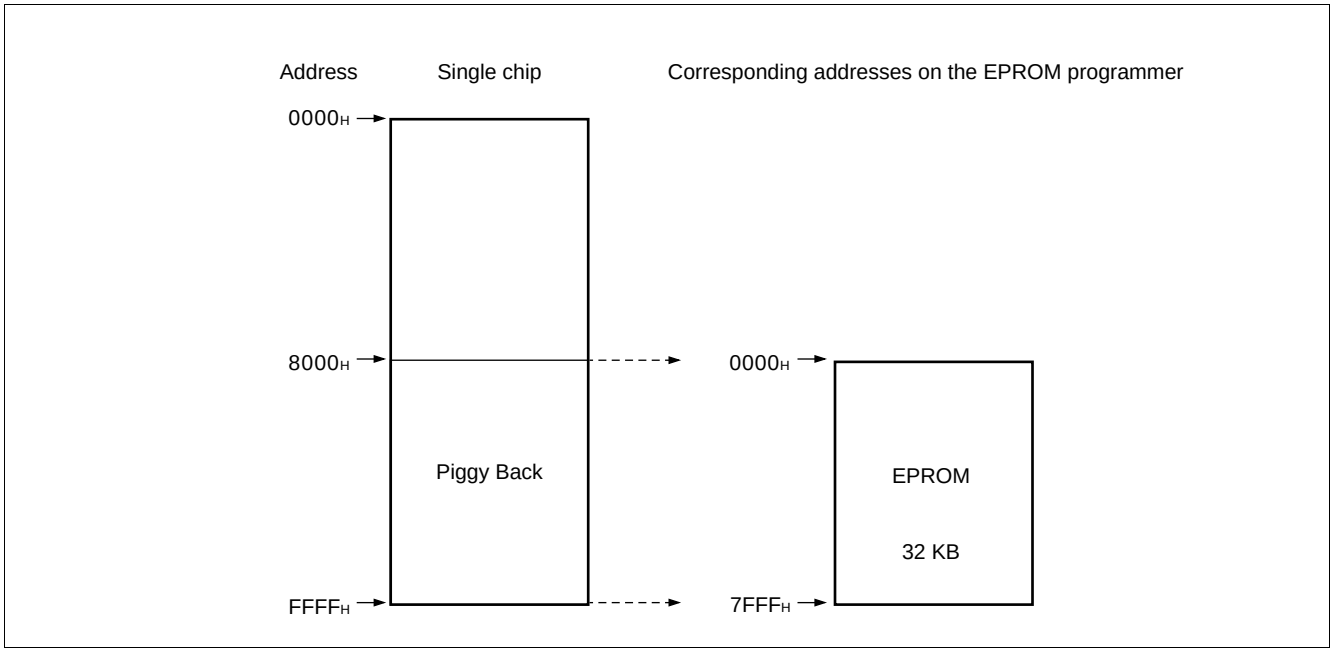
MBM27C256A-20TVM

2. Programming Socket Adapter

Please consult Fujitsu.

3. Memory Space

The memory space of the piggyback EPROM is mapped onto the internal memory space as shown in the figure below.

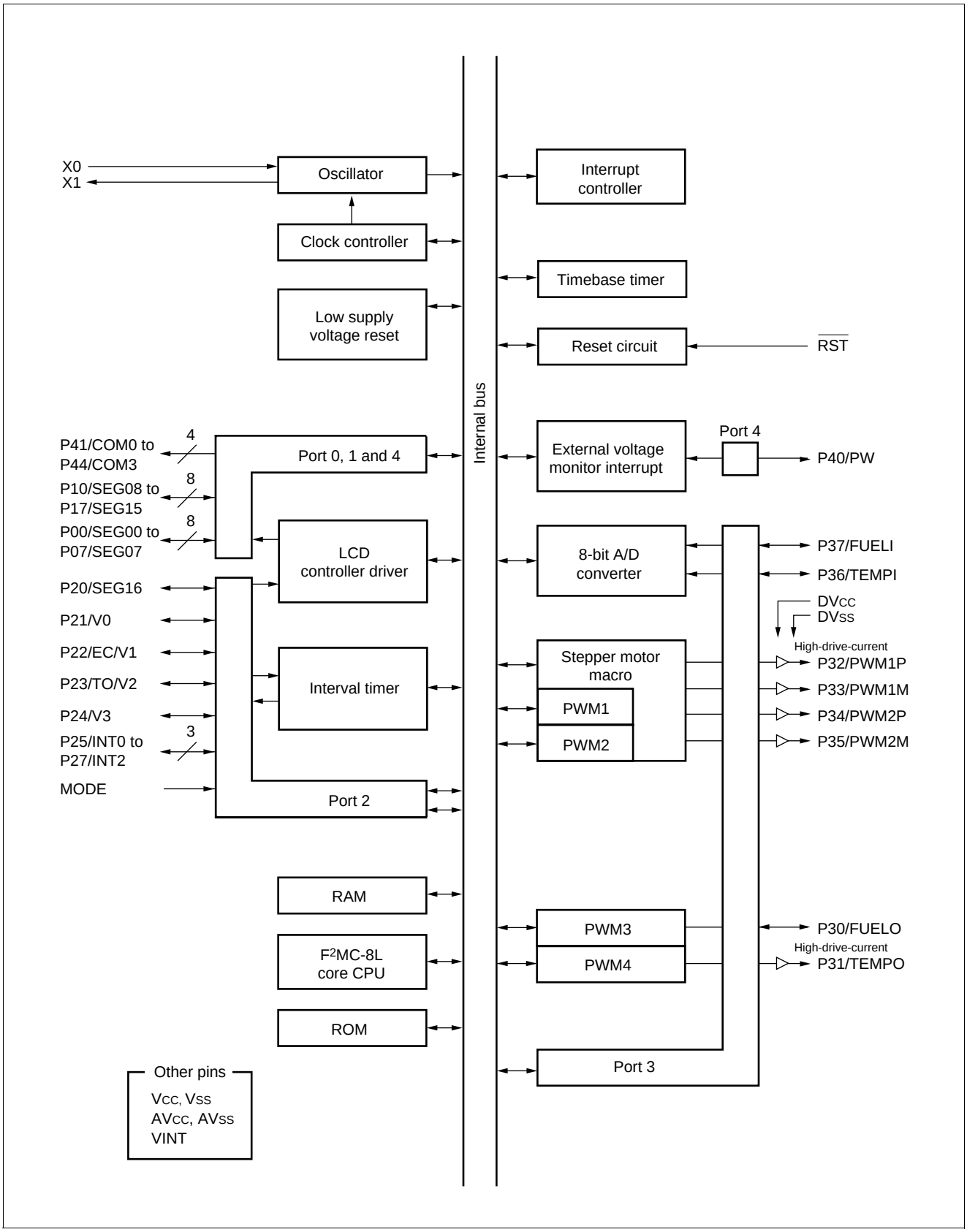


For EPROM devices suitable for MB89PV940, please consult Fujitsu.

4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A-20TVM.
(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.
(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

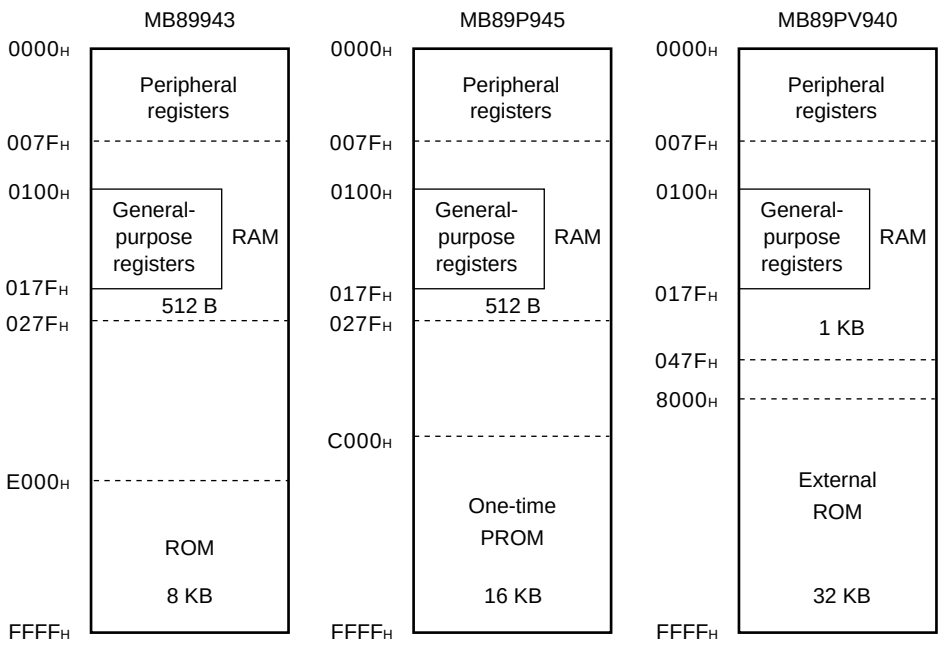


■ CPU CORE

1. Memory Space

The MB89940 Series has a memory space of 64 Kbytes. All peripheral registers, RAM and ROM areas are mapped onto the 0000_H to $FFFF_H$ range. The peripheral registers address below $007F_H$ and the RAM addresses the range 0080_H to $027F_H$ (0080_H to $047F_H$ for MB89PV940). A part of this RAM area is also assigned as the general-purpose registers. The ROM addresses above $E000_H$. The One-Time PROM addresses the range above $C000_H$. The external ROM for the piggy sample addresses the range above 8000_H. The reset vector, interrupt vectors and vectors for vector-call instructions are stored in the highest addresses of the memory space.

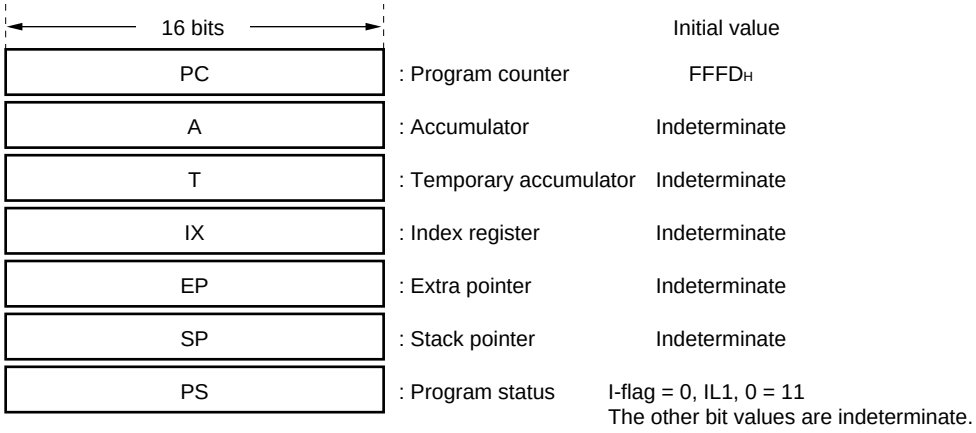
Memory Space



2. Registers

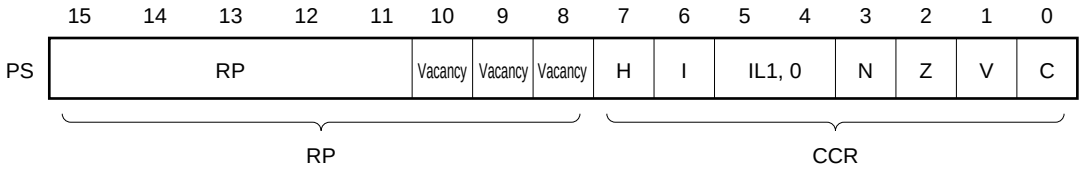
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



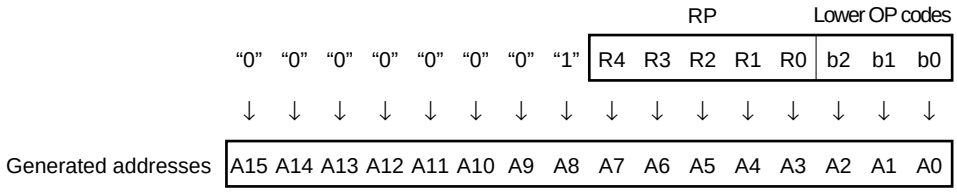
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' otherwise.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on '2' overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to '1' to the shift-out value in the case of a shift instruction.

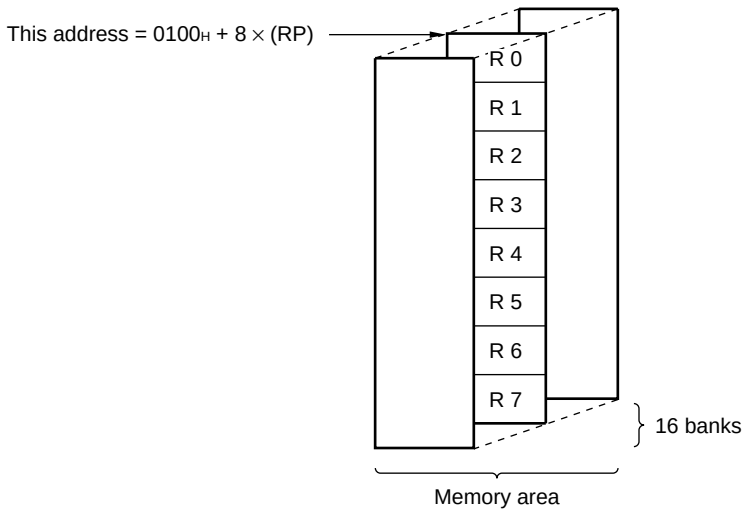
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89943 (RAM 512 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size. Up to a total of 32 banks can be used on other than the MB89943.

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	PDD0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	PDD1	Port 1 data direction register
04_H to 06_H			Vacancy
07_H	(R/W)	SCC	System clock control register
08_H	(R/W)	SMC	Standby mode control register
09_H	(R/W)	WDTC	Watchdog timer control register
$0A_H$	(R/W)	TBTC	Timebase timer control register
$0B_H$	(R/W)	LVRC	Low voltage reset control
$0C_H$	(R/W)	PDR2	Port 2 data register
$0D_H$	(W)	PDD2	Port 2 data direction register
$0E_H$	(R/W)	PDR3	Port 3 data register
$0F_H$	(W)	PDD3	Port 3 data direction register
10_H	(R/W)	PDR4	Port 4 data register
11_H	(R/W)	ADE	Port 3 A/D input enable register
12_H to 17_H			Vacancy
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$ to $1F_H$			Vacancy
20_H	(R/W)	ADC1	A/D converter control register 1
21_H	(R/W)	ADC2	A/D converter control register 2
22_H	(R/W)	ADCD	A/D converter data register
23_H	(R/W)	CNTR	PWM control register
24_H	(W)	COMP1	PWM1 compare register
25_H			Vacancy
26_H	(W)	COMP2	PWM2 compare register
27_H	(R/W)	SELR1	PWM1 select register
28_H	(R/W)	SELR2	PWM2 select register
29_H	(R/W)	CNTR3	PWM3 control register
$2A_H$	(W)	COMP3	PWM3 compare register
$2B_H$	(R/W)	CNTR4	PWM4 control register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
$2C_H$	(W)	COMP4	PWM4 compare register
$2D_H$	(R/W)	SELT	Selector test register
$2E_H$	(R/W)	PFC	Power fail control register
$2F_H$	(R/W)	EIR1	External interrupt control 1 register
30_H	(R/W)	EIR2	External interrupt control 2 register
31_H to $5F_H$			Vacancy
60_H to 68_H	(R/W)	VRAM	Display data RAM
69_H to 71_H			Vacancy
72_H	(R/W)	LCR1	LCD controller/driver register
73_H	(R/W)	LCR2	LCD controller/driver 2 register
74_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.5	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.5	V	Should not exceed V_{CC}
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.5	V	Should not exceed V_{CC}
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P31 to P35 and P41 to P44
	V_{I2}	V_{SS} – 0.3	DV_{CC} + 0.3	V	P31 to P35
	V_{I3}	V_{SS} – 0.3	V_{SS} + 6.5	V	P41 to P44 MB89PV940/945
	V_{I4}	V_{SS} – 0.3	V_{CC} + 0.3	V	P41 to P44 MB89943
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P31 to P35 and P41 to P44
	V_{O2}	V_{SS} – 0.3	DV_{CC} + 0.3	V	P31 to P35
	V_{O3}	V_{SS} – 0.3	V_{SS} + 6.5	V	P41 to P44 MB89PV940/945
	V_{O4}	V_{SS} – 0.3	V_{CC} + 0.3	V	P41 to P44 MB89943
“L” level maximum output current	V_{OL}	—	20	mA	Except P31 to P35
		—	50	mA	P31 to P35
“L” level average output current	V_{OLAV}	—	4	mA	Except P31 to P35
		—	40	mA	P31 to P35
“L” level total maximum output current	$V_{OLTOTALMAX}$	—	100	mA	Except P31 to P35
		—	200	mA	P31 to P35
“L” level total average output current	$V_{OLTOTALAV}$	—	40	mA	Except P31 to P35
		—	100	mA	P31 to P35
“H” level maximum output current	V_{OH}	—	–20	mA	Except P31 to P35
		—	–50	mA	P31 to P35
“H” level average output current	V_{OHAV}	—	–4	mA	Except P31 to P35
		—	–40	mA	P31 to P35
“H” level total maximum output current	$V_{OHTOTALMAX}$	—	–50	mA	Except P31 to P35
		—	–200	mA	P31 to P35
“H” level total average output current	$V_{OHTOTALAV}$	—	–20	mA	Except P31 to P35
		—	–100	mA	P31 to P35
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{CC} = V_{CC} = DV_{CC} = 5.0 V, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Operating supply voltage range	V_{CC} AV_{CC} DV_{CC}	3.5	—	5.5	V	
RAM data retention supply voltage range	V_{CC} AV_{CC} DV_{CC}	3.0	—	5.5	V	
Operating temperature range	T_A	–40	—	+85	°C	

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(AV_{CC} = V_{CC} = DV_{CC} = 5.0 V, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17 P30 to P37, P40 to P47	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MODE, P20 to P27	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17 P30 to P37, P40 to P47	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MODE, P20 to P27	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P41 to P44	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	MB89PV940/945
	V_{D3}	P41 to P44	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	MB89943
"H" level output voltage	V_{OH}	P10 to P17, P20 to P27, P30, P36, P37	I_{OH} = –2.0 mA	4.0	—	—	V	
	V_{OH2}	P31 to P36	I_{OH} = –30 V_{CC} = DV_{CC}	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL}	P10 to P17, P20 to P27, P30, P36, P37, P40 to P44	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P31 to P36	I_{OL} = 30 mA V_{SS} = DV_{SS}	—	—	0.5	V	

(Continued)

(Continued)

(AV_{CC} = V_{CC} = DV_{CC} = 5.0 V, V_{SS} = AV_{SS} = DV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input leakage current	I_{IL1}	MODE, P10 to P17, P20 to P27, P30 to P37, P40 to P44	0.0 V< V_I < V_{CC}, V_{CC} = DV_{CC}	–5	—	+5	µA	Without pull-up option
Pull-up resistance	R_{PULL}	$\overline{RST}$, P12 to P17, P20 to P27	—	25	50	100	kΩ	With pull-up option
LCD internal bias voltage resister	R_{LCD}	V0-V1, V1-V2, V2-V3	—	50	100	200	kΩ	
Power supply current	I_{CC}	V_{CC}	F_C = 8 MHz, t_{inst}* = 0.5 µs I_{CC} = I(V_{CC}) + I(DV_{CC})	—	12	20	mA	MB89PV940
				—	12	20	mA	MB89943, MB89P945
	I_{CCS}		F_C = 8 MHz t_{inst}* = 0.5 µs I_{CCS} = I(V_{CC}) + I(DV_{CC}) in Sleep mode	—	3	7	mA	
	I_{CCH}		In Stop mode T_A = 25°C I_{CCH} = I(V_{CC}) + I(DV_{CC})	—	5	10	µA	
	I_A	AV_{CC}	F_C = 8 MHz I_A = I(AV_{CC}) A/D in operation	—	6	8	mA	
	I_{AH}		F_C = 8 MHz I_{AH} = I(AV_{CC}) A/D stopped	—	5	10	µA	
Input capacitance	C_{IN}	—	f = 1 MHz	—	10	—	pF	
External capacitor at VINT	C_{VINT}	—	—	—	0.1	—	µF	MB89943 only

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

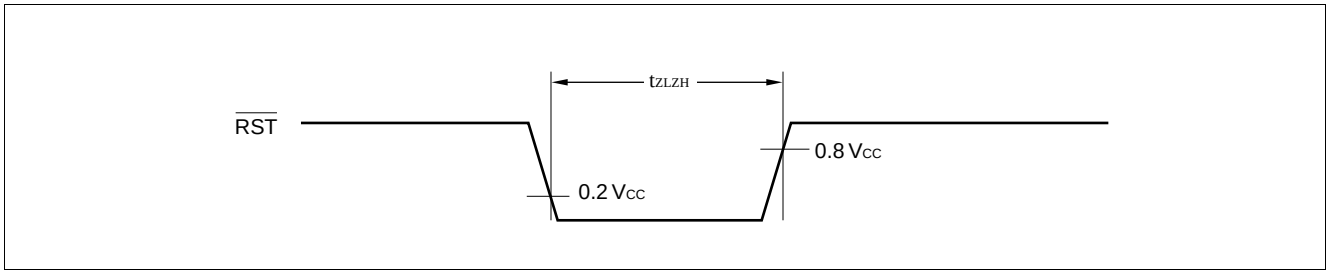
4. AC Characteristics

(1) Reset Timing

(AV_{SS} = V_{SS} = DV_{SS}, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ “L” pulse width	t_{ZLZH}	—	16 t_{HCYL}	—	ns	

t_{HCYL}: One oscillation clock cycle time



If power-on reset option is not activated, the external reset signal must be kept asserted until the oscillation is stabilized.

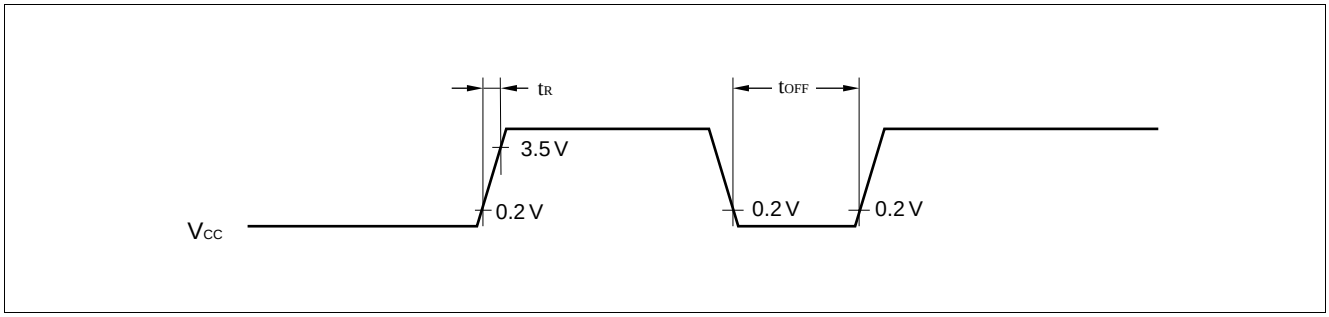
(2) Power-on Profile

($AV_{SS} = V_{SS} = DV_{SS}$, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply voltage rising time	t_R	—	—	50	ms	MB89PV940, MB89P945
Power supply voltage rising time	t_R	—	—	$2^{19}\,t_{HCYL}$	ns	MB89943
Power-off minimum period	t_{OFF}	—	1	—	ms	

t_{HCYL}: One oscillation clock cycle time

Note: Power supply voltage should reach the minimum operation voltage within the specified default duration of the oscillation stabilization time.

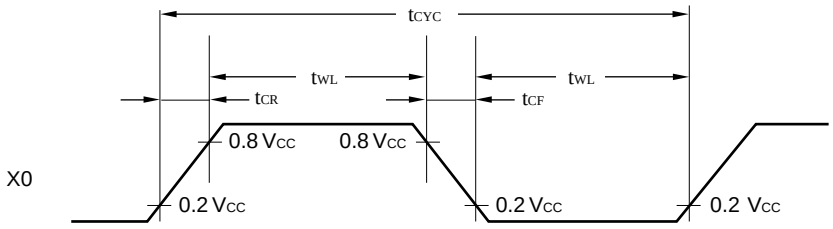


(3) Clock Timing

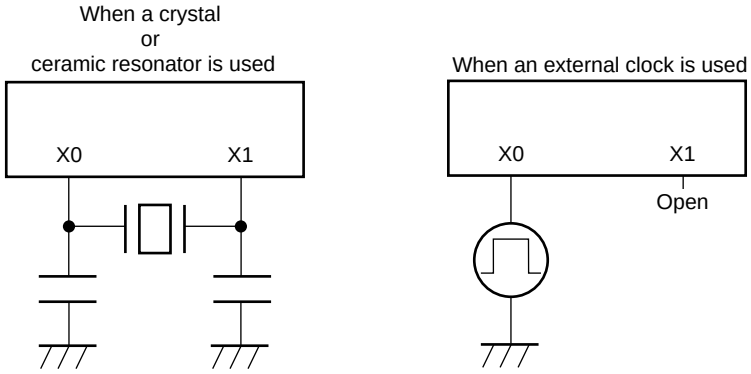
($AV_{SS} = V_{SS} = DV_{SS}$, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Clock frequency	F_C	—	1	8	MHz	
Clock cycle time	t_{CYC}		1000	125	ns	
Input clock pulse width	t_{WH} t_{WL}		20	—	ns	
Input clock rising/falling time	t_{CR} t_{CF}		—	10	ns	

X0 and X1 Timing and Conditions



Clock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_C, 8/F_C, 16/F_C, 64/F_C	µs	(4/F_C) t_{inst} = 0.5 µs when operating at F_C = 8 MHz

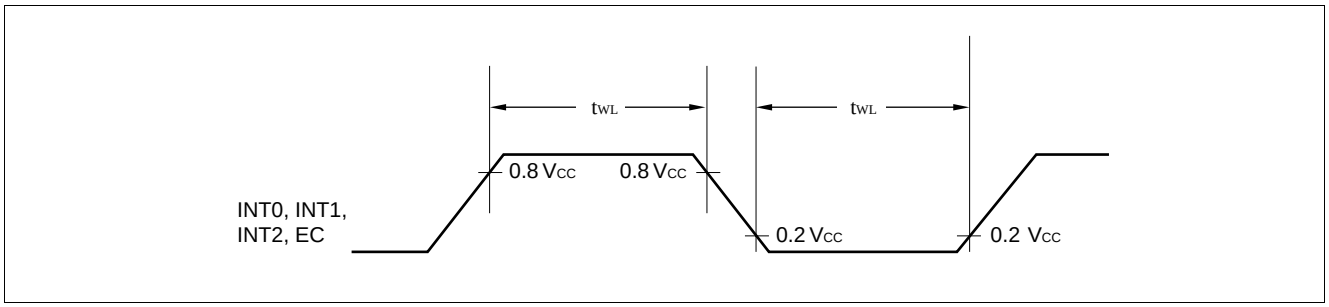
Note: When operating at 8 MHz, the cycle varies with the set execution time.

(5) Peripheral Input Timing

(AV_{SS} = V_{SS}= DV_{SS}, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width	t_{WH}	INT0, INT1, INT2, EC	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width	t_{WL}	INT0, INT1, INT2, EC	2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

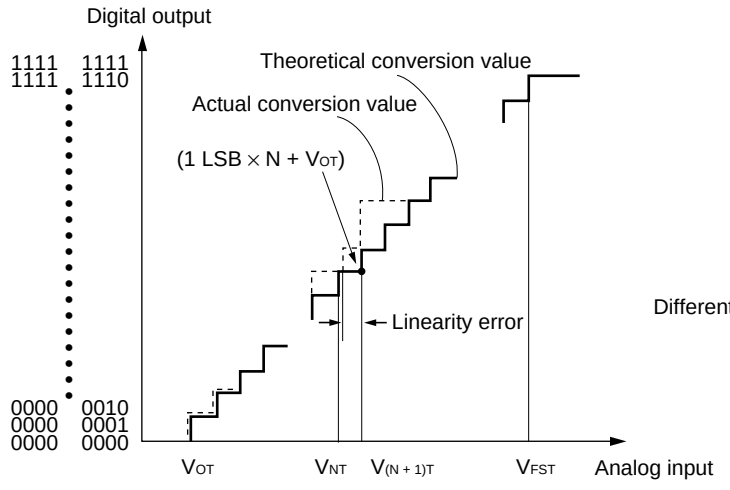
($AV_{SS} = V_{SS} = DV_{SS}$, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error				—	—	±1.5	LSB	
Linearlity error				—	—	±1.0	LSB	
Differential linearlity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.0 LSB	V	MB89PV940/P945
				AV_{SS} + 5/8 LSB	AV_{SS} + 7/8 LSB	AV_{SS} + 11/8 LSB	V	MB89943
Full-scale transition voltage	V_{FST}			AV_{CC} – 3.0 LSB	AV_{CC} – 1.5 LSB	AV_{CC}	V	MB89PV940/P945
				AV_{CC} – 13/8 LSB	AV_{CC} – 9/8 LSB	AV_{CC} – 7/8 LSB	V	MB89943
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time				—	—	44 t_{inst}*	µs	MB89PV940/P945
				—	—	52 t_{inst}*	µs	MB89943
Analog input current	I_{AIN}			—	—	10	µA	
Analog input voltage range	—			0	—	AV_{CC}	V	

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 8, analog voltage can be divided into $2^8 = 256$.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



$$1\ \text{LSB} = \frac{\text{AVR}}{256}$$

$$\text{Linearity error} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

$$\text{Total error} = \frac{V_{NT} - (1\ \text{LSB} \times N + 1\ \text{LSB})}{1\ \text{LSB}}$$

7. Notes on Using A/D Converter

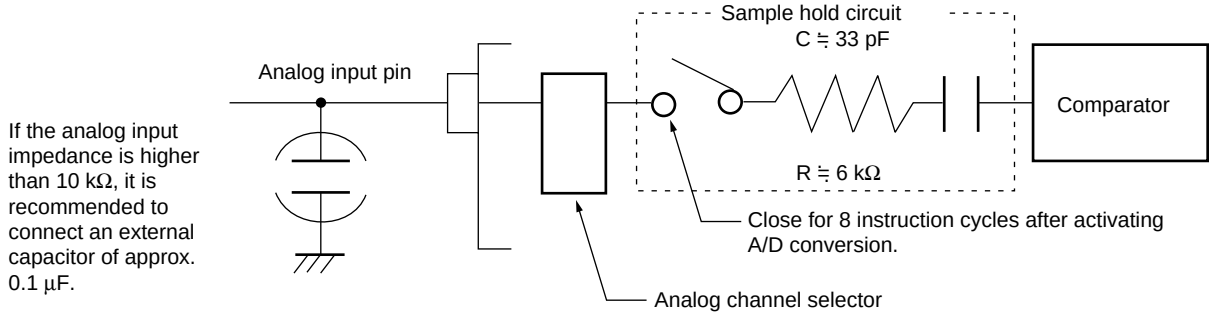
- **Input impedance of the analog input pins**

  The A/D converter used for the MB89940 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

Analog Input Equivalent Circuit



- **Error**

  The smaller the | AV_{CC} – AV_{SS} |, the greater the error would become relatively.

8. Low Supply Voltage Reset Electrical Characteristics

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Reset voltage	V_{DL1}	3.0	3.6	V	When the voltage is dropping. Refer to the register definition.
	V_{DL2}	3.3	3.9	V	
	V_{DL3}	3.7	4.3	V	
Hysteresis of reset voltage	V_{HYS}	0.1	—	V	When the voltage is recovering.
Delay time to reset	t_D	—	2.0	µs	
Supply voltage slew rate	dV/dt	—	0.1	V/µs	

9. External Voltage Monitor Interrupt Electrical Characteristics

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Reference voltage	V_{REF}	1.18	1.38	V	
Delay time to interrupt	T_D	—	2.0	µs	Refer to the register definition.
Input slew rate	dV/dt	—	0.1	V/µs	

■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic:	Assembler notation of an instruction
~:	The number of instructions
#:	The number of bytes
Operation:	Operation of an instruction
TL, TH, AH:	A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following: • "–" indicates no change. • dH is the 8 upper bits of operation description data. • AL and AH must become the contents of AL and AH prior to the instruction executed. • 00 becomes 00.
N, Z, V, C:	An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.
OP code:	Code of an instruction. If an instruction is more than one code, it is written according to the following rule: Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

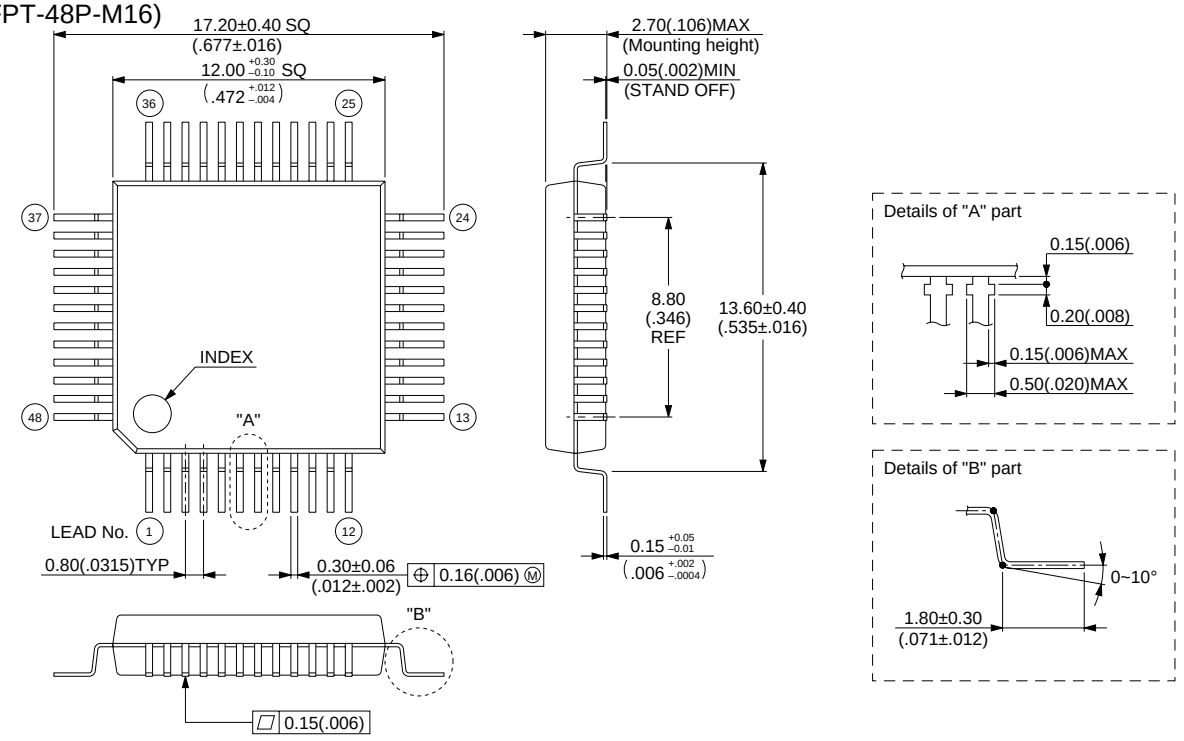
No.	Part number	MB89943	MB89P945	MB89PV940
	Specifying procedure	Specify when ordering masking	Set with EPROM Programmer	Setting not possible
1	Pull-up resistors P12 to P17, P20 to P27	Selectable per pin (P20 and P12 to P17 must be set to without pull-up resistor when they are used as LCD outputs.)	Can be set per pin	Fixed to without pull-up resistor
2	Power-on reset With power-on reset Without power-on reset	Fixed to with power-on reset	Setting possible	Fixed to with power-on reset
3	Main clock oscillation stabilization time selection (when operating at 8 MHz) Approx. $2^{18}/F_C$ (Approx. 32.8 ms) Approx. $2^{17}/F_C$ (Approx. 16.4 ms) Approx. $2^{14}/F_C$ (Approx. 2.0 ms)	Selectable	Setting possible	Fixed to approx. $2^{18}/F_C$ (Approx. 32.8 ms)
4	Reset pin output With reset output Without reset output	Fixed to with reset output	Setting possible	Fixed to with reset output

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89943PF MB89P945PF	48-pin Plastic QFP (FPT-40P-M16)	
MB89PV940CF	48-pin Ceramic MQFP (MQP-48C-P01)	

■ PACKAGE DIMENSION

48-pin Plastic QFP
(FPT-48P-M16)



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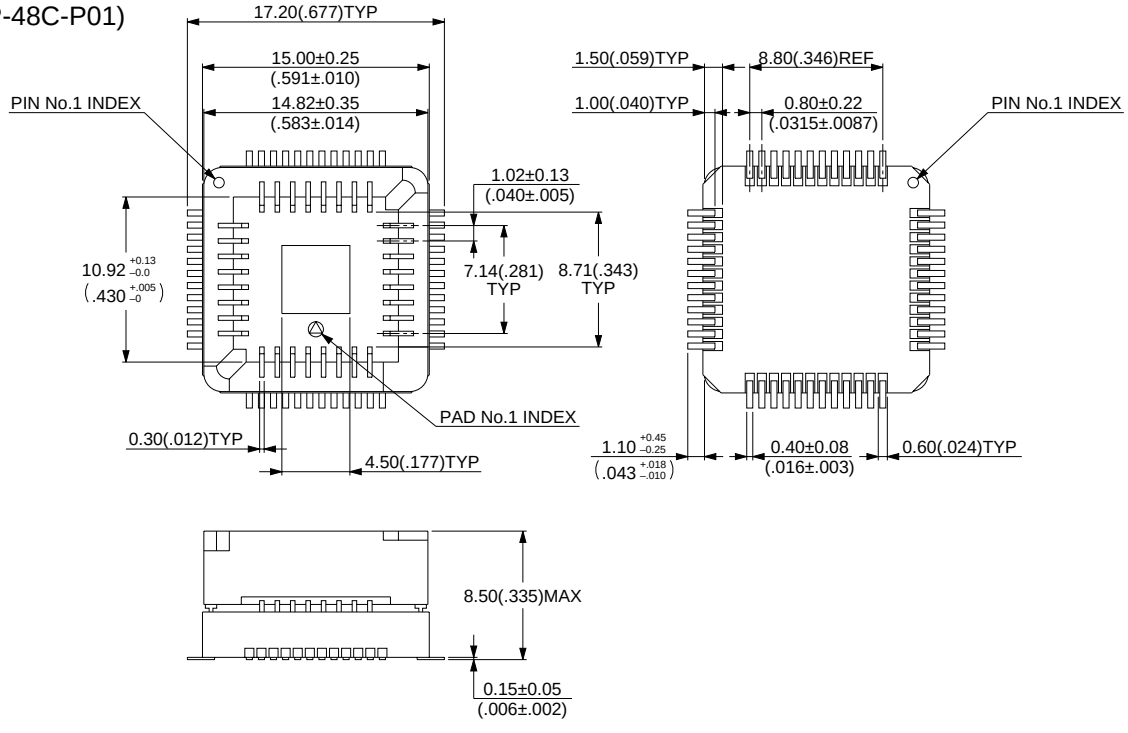
Dimensions in mm (inches)

48-pin Ceramic MQFP
(MQP-48C-P01)



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Dimensions in mm (inches)

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