

FEATURES

- **Wide Input Range: 4V to 36V**
- **Overvoltage Shutdown Protects Circuit Through 70V Transients**
- **2.6A Output Switching Regulator with Internal Power Switch**
- **Dual, Low Dropout, Linear Regulator Controllers with Programmable Current Limit**
- Tracking/Soft-Start Inputs and Power Good Output Simplify Soft-Start and Supply Sequencing
- Uses Small Inductors and Ceramic Capacitors
- $V_{OUT(MIN)} = 0.75V$ (Buck and LDOs)
- Adjustable 250kHz to 2.5MHz Switching Frequency
- Accurate Enable Threshold Allows User Programmable Undervoltage Lockout
- Options for Clock Synchronization (LT3694) or Clock Output to Enable Synchronization to Other Switching Regulators (LT3694-1)
- Thermally Enhanced 28-Lead 4mm × 5mm QFN and 20-Lead TSSOP Packages

APPLICATIONS

- Automotive
- Industrial
- DSL and Cable Modems
- Distributed Power Regulation
- Wall Transformer Regulation

DESCRIPTION

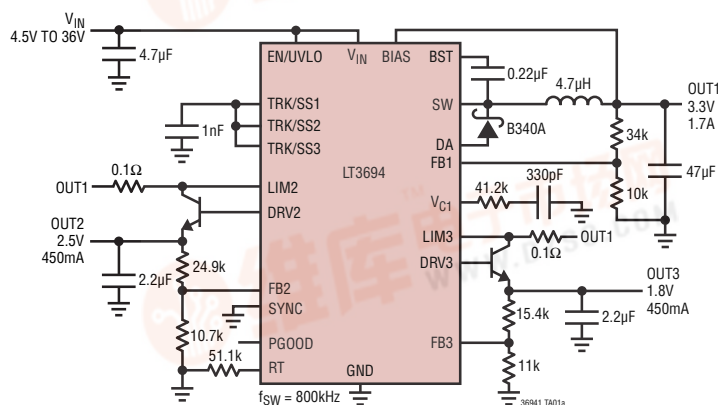
The LT[®]3694/LT3694-1 are monolithic, current mode DC/DC converters with dual, low dropout regulator controllers. The switching converter is a step-down converter capable of generating up to 2.6A at its output. Each regulator has independent track/soft-start circuits simplifying power supply sequencing and interfacing with micro-controllers and DSPs.

The switching frequency is set with a single resistor with a range of 250kHz to 2.5MHz. The high switching frequency permits the use of small inductors and ceramic capacitors leading to very small triple output solutions. The constant-switching frequency, combined with low impedance ceramic capacitors, results in low, predictable output ripple. Protection circuitry senses the current in the power switch and external Schottky catch diode to protect the LT3694 against short-circuit conditions. Frequency foldback and thermal shutdown provide additional protection.

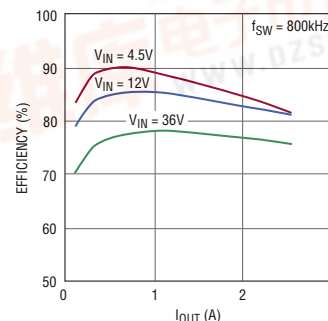
With its wide input voltage range of 4V to 36V, the LT3694 regulates a broad array of power sources from 4-cell batteries and 5V logic rails to unregulated wall transformers, lead acid batteries and distributed power supplies. The LT3694 can be synchronized to an external clock with the SYNC pin while the LT3694-1 offers a CLKOUT pin allowing other DC/DC converters to synchronize to the LT3694-1 clock.

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TYPICAL APPLICATION



Efficiency at $V_{OUT} = 3.3V$



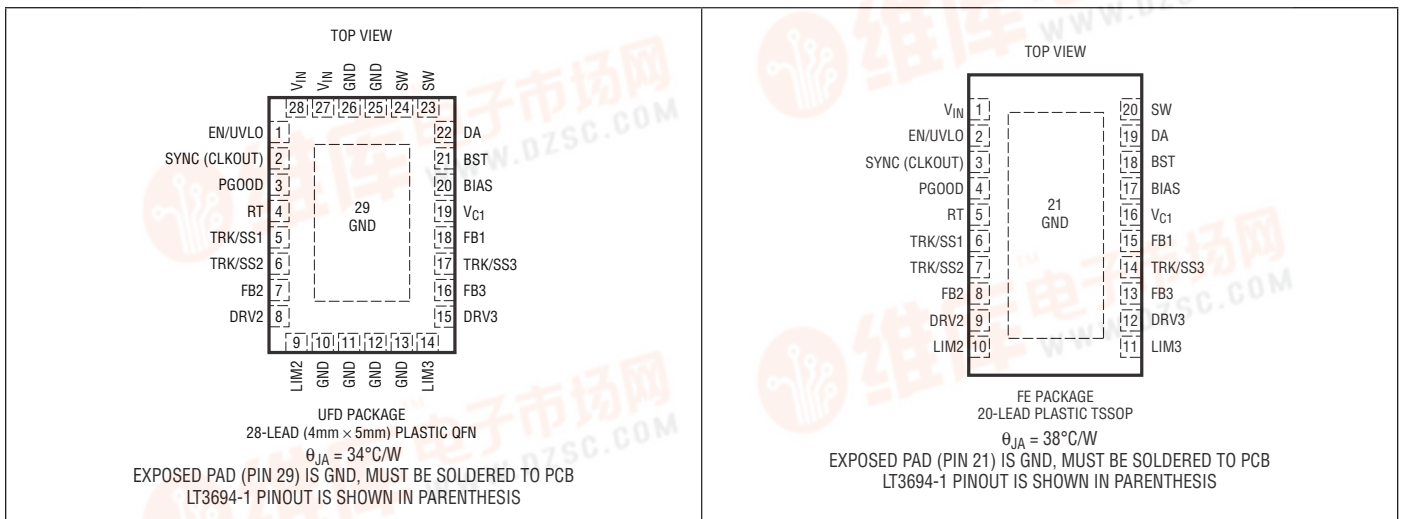
LT3694/LT3694-1

查閱 LT3694 規格書

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} , EN/UVLO (Note 6).....	-0.3V to 70V	Operating Junction Temperature Range (Notes 2 and 5)	
BST	55V	LT3694E.....	-40°C to 125°C
BST Above SW	25V	LT3694I.....	-40°C to 125°C
PGOOD.....	16V	Storage Temperature Range.....	-65°C to 150°C
TRK/SS, V_C , FB, RT, SYNC Pins.....	6V	Lead Temperature (Soldering, 10 Sec)	
BIAS, LIM2, LIM3 Pins	7V	(TSSOP Only)	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3694EUFD#PBF	LT3694EUFD#TRPBF	3694	28-Lead (4mm x 5mm) Plastic QFN	-40°C to 125°C
LT3694IUFD#PBF	LT3694IUFD#TRPBF	3694	28-Lead (4mm x 5mm) Plastic QFN	-40°C to 125°C
LT3694EFE#PBF	LT3694EFE#TRPBF	LT3694FE	20-Lead Plastic eTSSOP	-40°C to 125°C
LT3694IFE#PBF	LT3694IFE#TRPBF	LT3694FE	20-Lead Plastic eTSSOP	-40°C to 125°C
LT3694-1EUFD#PBF	LT3694-1EUFD#TRPBF	36941	28-Lead (4mm x 5mm) Plastic QFN	-40°C to 125°C
LT3694-1IUFD#PBF	LT3694-1IUFD#TRPBF	36941	28-Lead (4mm x 5mm) Plastic QFN	-40°C to 125°C
LT3694-1EFE#PBF	LT3694-1EFE#TRPBF	LT3694FE-1	20-Lead Plastic eTSSOP	-40°C to 125°C
LT3694-1IFE#PBF	LT3694-1IFE#TRPBF	LT3694FE-1	20-Lead Plastic eTSSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{BIAS} = 3\text{V}$, unless otherwise noted. (Notes 2, 9)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Internal Undervoltage Lockout		●	3.5	3.8	4	V
Overshoot Shutdown Threshold		●	36	38	40	V
Input Quiescent Current	Not Switching			1	2	mA
Bias Quiescent Current	Not Switching			2	3.5	mA
Shutdown Current	$V_{EN/UVLO} = 0.1\text{V}$			0.1	2	μA
EN/UVLO Threshold, Bias On			350	500		mV
EN/UVLO Threshold, Switching On		●	1.16	1.2	1.23	V
Reference Voltage Line Regulation	$5\text{V} < V_{IN} < 36\text{V}$			0.01		%/V
Switching Frequency	$R_T = 40.2\text{K}$	●	0.9	1.0	1.1	MHz
V_{IH} , SYNC		●	1.5			V
V_{IL} , SYNC		●			0.35	V
V_{OH} , CLKOUT	$I_{CLKOUT} = -50\mu\text{A}$	●	1.6		2.6	V
V_{OL} , CLKOUT	$I_{CLKOUT} = 50\mu\text{A}$	●			0.3	V
PGOOD Output Voltage Low	$I_{PGOOD} = 250\mu\text{A}$			0.2	0.4	V
PGOOD Leakage	$V_{PGOOD} = 2\text{V}$			10	1000	nA
PGOOD Threshold (Relative to V_{FB})	(Note 8)		86	90	94	%
Switching Regulator						
Feedback Pin Voltage		●	735	750	765	mV
Feedback Pin Bias Current		●		-50	-500	nA
Error Amplifier Transconductance				350		μS
Error Amplifier Voltage Gain				600		V/V
TRK/SS Pull-Up Current			-2	-3	-4	μA
TRK/SS Threshold to Start Switching			35	50	70	mV
V_{C1} Source Current	$V_C = 0.6\text{V}$			-20		μA
V_{C1} Sink Current	$V_C = 0.6\text{V}$			28		μA
V_{C1} Clamp Voltage				2		V
V_{C1} Switching Threshold				0.75		V
V_{C1} to Switch Current Gain				3.6		A/V
Switch Leakage Current	$V_{IN} = 36\text{V}$			0.01	10	μA
Minimum Boost Voltage Above Switch	(Note 4)			1.8	2.5	V
Switch Current Limit (Note 3)	(Note 3) 10% Duty Cycle	●	3.5	4.9	6	A
Switch V_{CESAT}	$I_{SW1} = 3\text{A}$			600		mV
BST Operating Current	$I_{SW1} = 3\text{A}$			60		mA
V_F , BST Diode	$I_{BST} = 100\text{mA}$			0.8		V
I_L BST Diode	$V_{BST} - V_{BIAS} = 36\text{V}$			1		μA
DA Current Limit		●	2.6	3.6	4.5	A
Minimum Switch Off-Time		●			140	ns

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{BIAS} = 3\text{V}$, unless otherwise noted. (Notes 2, 9)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator						
Feedback Pin Voltage		●	735	750	765	mV
Feedback Pin Bias Current		●		-50	-500	nA
Error Amplifier Voltage Gain				2800		
TRK/SS Pull-Up Current			-2	-3	-4	μA
TRK/SS Threshold to Shut Down LDO			35	50	70	mV
Line Regulation	$5\text{V} < V_{IN} < 36\text{V}$			0.025		%/V
Load Regulation	I_{DRV} From 0.1mA to 10mA			0.5		mV/mA
Base Drive		●	10	15	20	mA
Current Limit Threshold		●	47	60	70	mV
Short-Circuit Current Limit Threshold	$V_{FB} = 0$		22	26	30	mV
Minimum BIAS to DRV Voltage (Note 7)	$I_{DRV} = 10\text{mA}$	●		0.3	0.9	V
Minimum V_{IN} to DRV Voltage	$I_{DRV} = 10\text{mA}$	●		2.0	2.3	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3694E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the -40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3694I is guaranteed to meet performance specifications from -40°C to 125°C junction temperature.

Note 3: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

Note 4: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating range when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

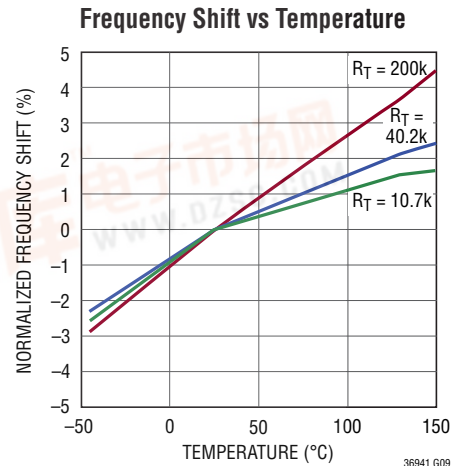
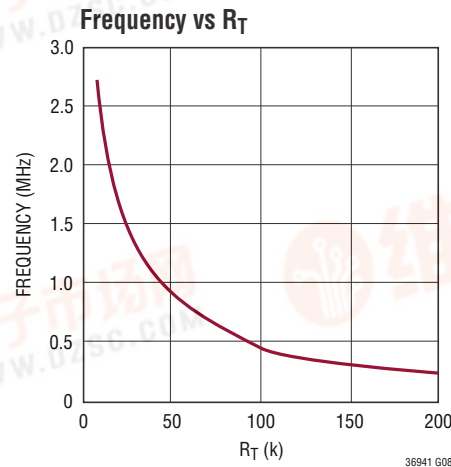
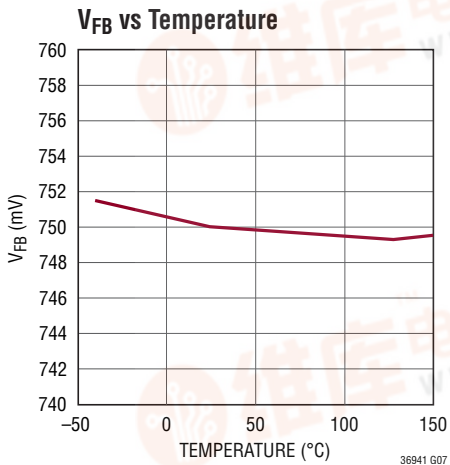
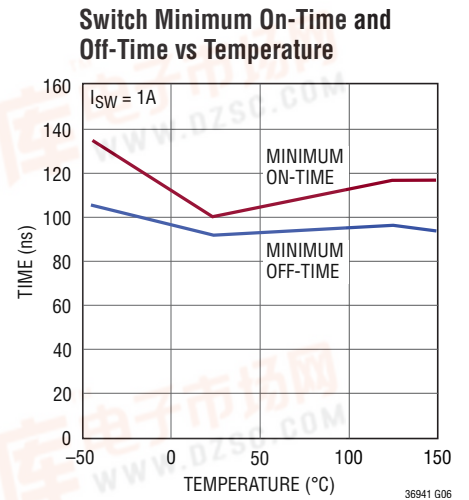
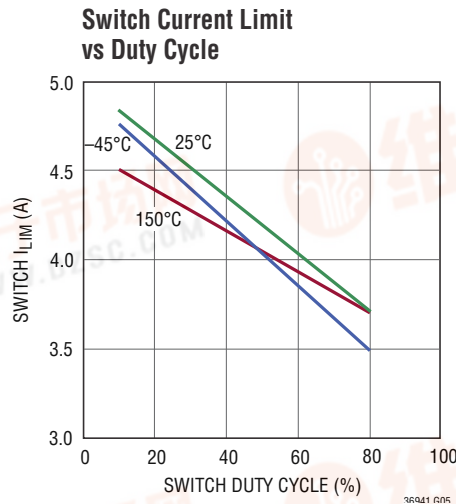
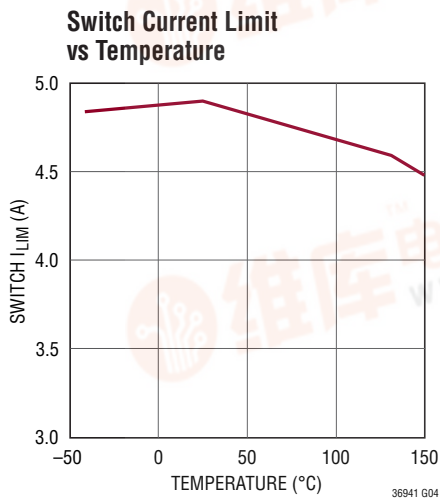
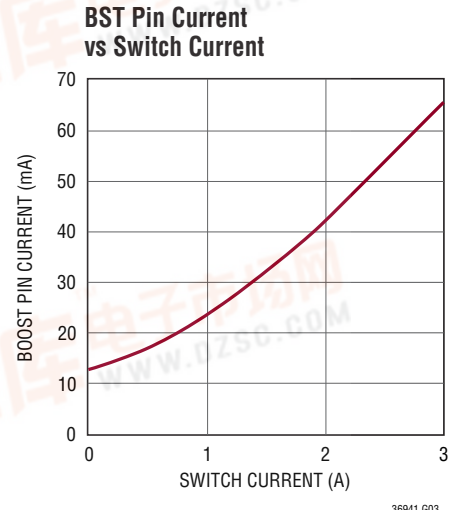
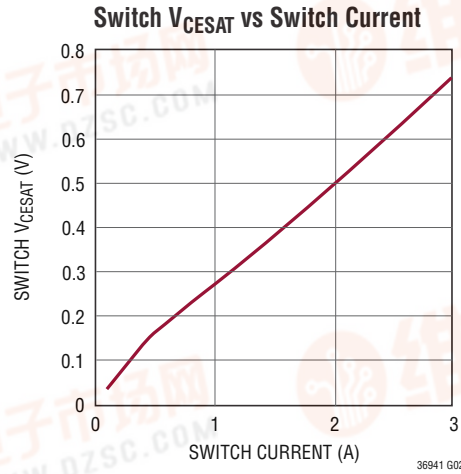
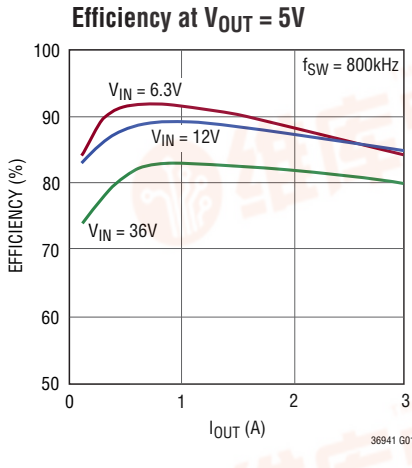
Note 6: Absolute Maximum Voltage at V_{IN} and EN/UVLO pins is 70V for non-repetitive, 1 second transients and 36V for continuous operation.

Note 7: The LDO will function if the BIAS to DRV differential is not met, but the base drive current will be drawn from V_{IN} instead of BIAS.

Note 8: The PGOOD pin will pull low when the voltage on any of the three FB pins is lower than the PGOOD threshold value.

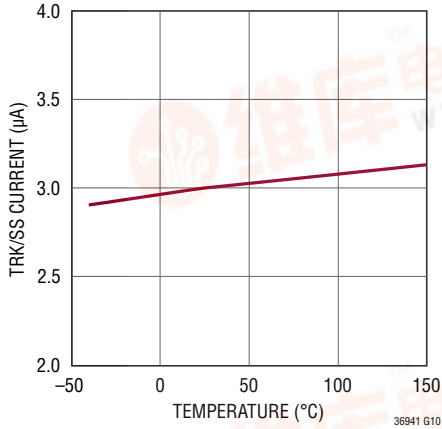
Note 9: Positive currents flow into pins, negative currents flow out of pins. Minimum and maximum values refer to absolute values.

TYPICAL PERFORMANCE CHARACTERISTICS $V_{IN} = 12V$, $T_A = 25^\circ C$, unless otherwise noted.



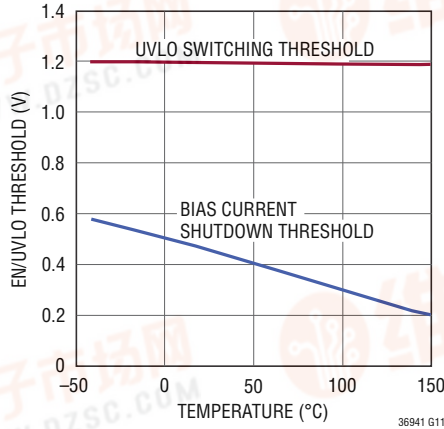
TYPICAL PERFORMANCE CHARACTERISTICS $V_{IN} = 12V$, $T_A = 25^\circ C$, unless otherwise noted.

I_{TRK/SS} vs Temperature



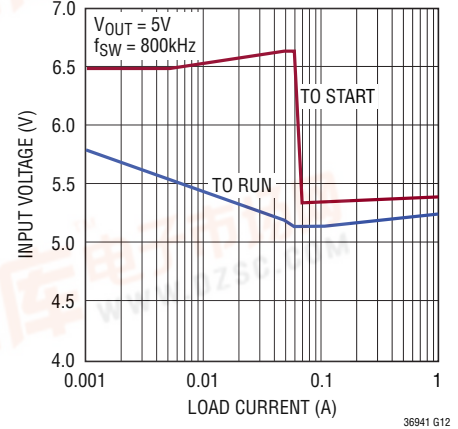
36941 G10

EN/UVLO Thresholds vs Temperature



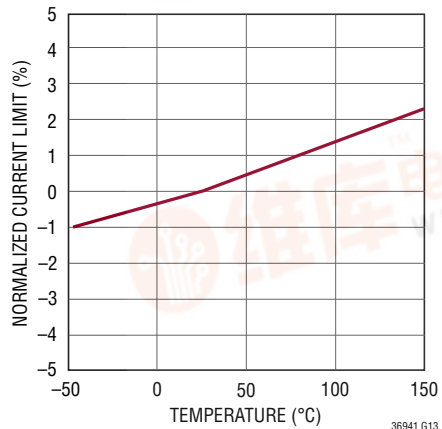
36941 G11

Minimum Input Voltage vs Load Current (V_{IN} to Start)



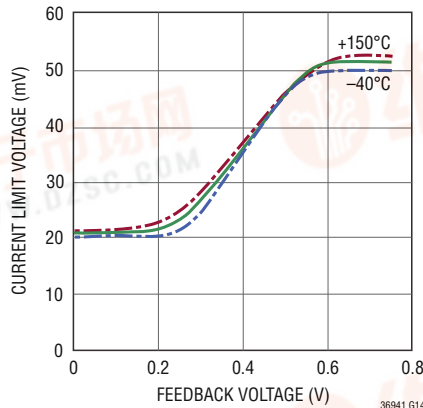
36941 G12

LDO Current Limit vs Temperature



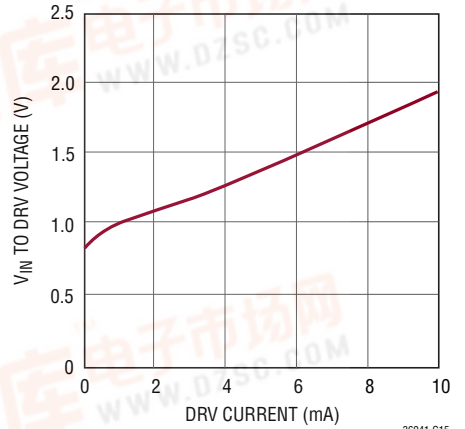
36941 G13

LDO Current Limit vs V_{FB} (Foldback)



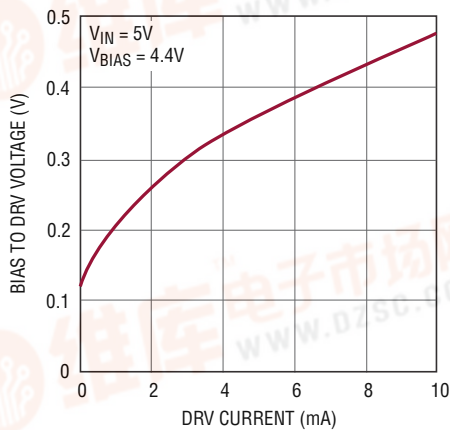
36941 G14

LDO Minimum V_{IN} to DRV Voltage vs DRV Current



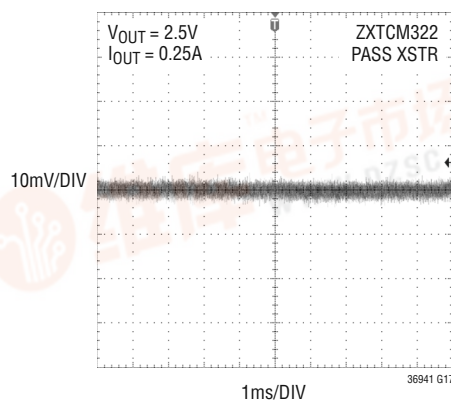
36941 G15

LDO Minimum BIAS to DRV Voltage vs DRV Current



36941 G16

10Hz to 100kHz LDO Output Noise



36941 G17

PIN FUNCTIONS (FE/UFD)

V_{IN} (Pin 1/Pins 27, 28): The V_{IN} pin supplies power to the internal switch of the 2.6A regulator and to the LT3694's internal reference and start-up circuitry. This pin must be locally bypassed.

EN/UVLO (Pin 2/Pin 1): The EN/UVLO pin is used to shut down the LT3694. It can be driven from a logic level or used as an undervoltage lockout by connecting a resistor divider from V_{IN}.

CLKOUT (Pin 3/Pin 2): Digital Clock Output. The CLKOUT pin allows synchronization of other switching regulators (LT3694-1 only).

SYNC (Pin 3/Pin 2): Frequency Synchronization Input. Connect a frequency source to this input if synchronization is desired. Connect SYNC to ground if not used (LT3694 only).

PGOOD (Pin 4/Pin 3): Open Collector Output. PGOOD is pulled low when any of the three regulators drops out of regulation ($V_{FB} < 90\%$ of nominal value).

RT (Pin 5/Pin 4): The RT pin requires a resistor to ground to set the operating frequency of the LT3694. If synchronizing the LT3694 to an external clock, the resistor should be set to program the frequency at least 20% below the synchronization frequency.

TRK/SS1, TRK/SS2, TRK/SS3 (Pins 6, 7, 14/Pins 5, 6, 17): The TRK/SS pins allow a regulator to track the output of another regulator. When the TRK/SS pin is below 0.75V, the FB pin regulates to the TRK/SS voltage. This pin can also be used as a soft-start by connecting a capacitor from TRK/SS to ground. The TRK/SS pins should be left open if neither feature is used.

FB1, FB2, FB3 (Pins 15, 8, 13/Pins 18, 7, 16): Negative Inputs of the Error Amplifiers. The LT3694 regulates each feedback pin to the lesser of 0.75V or the corresponding TRK/SS pin voltage. Connect the feedback resistor divider taps to these pins.

DRV2, DRV3 (Pins 9, 12/Pins 8, 15): The DRV pins provide the base drive for the external NPN transistors

for the LDO regulators. The DRV pins can provide up to 6V of base drive.

LIM2, LIM3 (Pins 10, 11/Pins 9, 14): The LIM pins provide current limiting on the LDO pass transistors by sensing a voltage on an external sense resistor connected to the BIAS pin. These pins should be connected to BIAS if this function is not used.

GND (Pins 10, 11, 12, 13, 25, 26) UFD Package Only: Power and Signal Ground.

V_{C1} (Pin 16/Pin 19): Output of the Internal Error Amp. The voltage on this pin controls the peak switch current. This pin is normally used to compensate the control loop. The switching regulator can be shut down by pulling the V_{C1} pin to ground with an NMOS or NPN transistor.

BIAS (Pin 17/Pin 20): The BIAS pin supplies the current to the LT3694's internal regulator and boost circuits. This must be connected to a voltage source above 3V, usually to V_{OUT1}. The LDO pass transistor base current will also come from the BIAS pin if it is at least 1.8V above the LDO output.

BST (Pin 18/Pin 21): The BST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.

DA (Pin 19/Pin 22): The DA pin senses the catch diode current to prevent excessive inductor current in output overload or short-circuit conditions.

SW (Pin 20/Pins 23, 24): Output of the Internal Power Switch. Connect this pin to the inductor and switching diode.

Exposed Pad (Pin 21/Pin 29): Ground. The underside Exposed Pad metal of the package provides both electrical contact to ground and a conductive thermal path to the printed circuit board. The Exposed Pad must be soldered to a grounded pad on the circuit board for proper operation.

BLOCK DIAGRAM

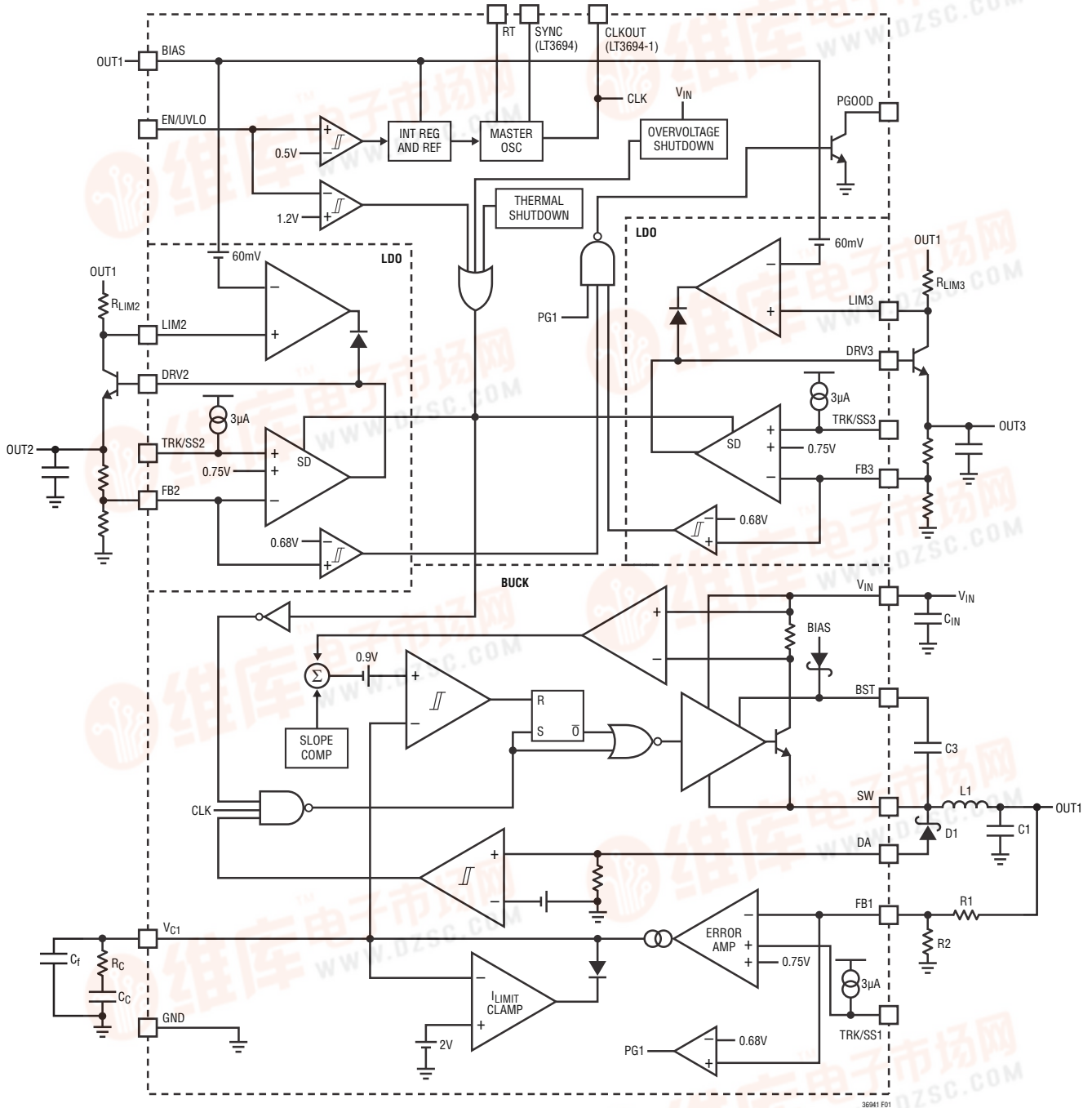


Figure 1. LT3694 Block Diagram with Typical External Components

OPERATION

Unless specifically noted, this data sheet refers to both the LT3694 and the LT3694-1 generically as the LT3694.

The LT3694 is a constant-frequency, current mode, buck regulator with an internal power switch plus two low dropout linear regulator controllers. The three regulators share common circuitry including input source, voltage reference, undervoltage lockout, and enable, but are otherwise independent. Operation can be best understood by referring to the Block Diagram (Figure 1).

If the EN/UVLO pin is below 0.35V (min), the LT3694 is shut down and draws $<2\mu\text{A}$ from the input source tied to $V_{\text{IN}1}$. If the EN/UVLO pin is driven above 0.5V (typ), the internal bias circuits turn on, including the internal regulator, reference and master oscillator. The switching regulator will only begin to operate when the EN/UVLO pin reaches $>1.20\text{V}$ (typ). The EN/UVLO pin can be driven from a logic gate or can be used as an undervoltage lockout by using a resistor divider to V_{IN} .

The switcher is a current mode regulator. Instead of directly modulating the duty cycle of the power switch, the feedback loop controls the peak current in the switch during each cycle. Compared to voltage mode control, current mode control improves loop dynamics and provides cycle-by-cycle current limit.

A pulse from the oscillator sets the RS flip-flop and turns on the internal NPN bipolar power switch. Current in the switch and the external inductor begins to increase. When this current exceeds a level determined by the voltage at $V_{\text{C}1}$, the current comparator resets the RS flip-flop, turning off the switch. The current in the inductor flows through the external, Schottky, catch diode, and begins to decrease. The cycle begins again at the next pulse from the oscillator. In this way, the voltage on the $V_{\text{C}1}$ pin controls

the current through the inductor to the output. The internal error amplifier regulates the output voltage by continually adjusting the $V_{\text{C}1}$ pin voltage. The threshold for switching on the $V_{\text{C}1}$ pin is 0.75V and an active clamp of 2V limits the output current.

Overcurrent protection is provided by the DA comparator. The DA comparator senses the catch diode current and will delay the switch-on cycle if the diode current is too high at the beginning of a cycle.

The TRK/SS pins override the 0.75V reference for the FB pins when the TRK/SS pins are below 0.75V. This allows either coincident or ratiometric supply tracking on start-up as well as a soft-start capability.

The switch driver operates either from V_{IN} or from the BST pin. An external capacitor is used to generate a voltage at the BST pin that is higher than the input supply. This allows the driver to saturate the internal bipolar NPN power switch for efficient operation.

The BIAS pin allows the internal circuitry to draw its current from a voltage supply lower than V_{IN} , reducing power dissipation and increasing efficiency. If the voltage on the BIAS pin falls below 2.7V, then its quiescent current will flow from V_{IN} .

The LDO regulator uses an external NPN pass transistor to form a linear regulator. The loop is internally compensated to be stable with a minimum load capacitance of 2.2 μF . The LDO also has a foldback current limiter available to protect the external transistor under overload conditions.

The overvoltage detection shuts down the LT3694 if the input voltage goes above 38V. This will prevent the switch from turning on under high voltage conditions and allows the LT3694 to survive transient input voltages up to 70V.

APPLICATIONS INFORMATION

STEP DOWN SWITCHING REGULATOR

Feedback Resistor Network

The output voltage is programmed with a resistor divider (refer to the Block Diagram in Figure 1) between the output and the FB pin. Choose the resistors according to:

$$R1=R2\left(\frac{V_{OUT}}{750mV}-1\right)$$

The parallel combination of R1 and R2 should be 10k or less to avoid bias current errors.

Input Overvoltage Lockout

An important feature of the LT3694 is the ability to survive transient surges on the input voltage of up to 70V. This is accomplished by shutting off the regulators to keep this high voltage off the critical components. The overvoltage lockout trips when the input voltage exceeds 38V.

Input Voltage Range

The minimum operating voltage is determined either by the LT3694's internal undervoltage lockout or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltage:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW} + V_F}$$

where V_F is the forward voltage drop of the catch diode and V_{SW} is the voltage drop of the internal switch (~0.3V at maximum load). This leads to a minimum input voltage of:

$$V_{IN(MINCF)} = \frac{V_{OUT} + V_F}{DC_{MAX(CF)}} - V_F + V_{SW}$$

The duty cycle is the fraction of time that the internal switch is on during a clock cycle. The maximum duty cycle for constant-frequency operation given by $DC_{MAX(CF)} = 1 - t_{OFF(MIN)} \cdot f_{SW}$. However, unlike most fixed frequency regulators, the LT3694 will not switch off at the end of

each clock cycle if there is sufficient voltage across the boost capacitor (C3 in Figure 1) to fully saturate the output switch. A forced switch off for a minimum time will only occur at the end of a clock cycle when the boost capacitor needs to be recharged. This operation has the same effect as lowering the clock frequency for a fixed off time, resulting in a higher duty cycle and lower minimum input voltage. The resultant duty cycle depends on the charging times of the boost capacitor and can be approximated by the following equation:

$$DC_{MAX} = \frac{B}{B+1}$$

where B is the output current divided by the typical boost current from the BST Pin Current vs Switch Current curve in the Typical Performance Characteristics section.

The maximum voltage, V_{IN} , for constant-frequency operation is determined by the minimum duty cycle DC_{MIN} :

$$V_{IN(MAXCF)} = \frac{V_{OUT} + V_F}{DC_{MIN}} - V_F + V_{SW}$$

with $DC_{MIN} = t_{ON(MIN)} \cdot f_{SW}$

Thus, both the maximum and minimum input voltages for constant-frequency operation are a function of the switching frequency and output voltage. Therefore, the maximum switching frequency must be set to a value that accommodates the input and output voltage parameters and must meet both of the following criteria:

$$f_{MAX1} = \left(\frac{V_{OUT} + V_F}{V_{IN(MAXCF)} - V_{SW} + V_F} \right) \cdot \frac{1}{t_{ON(MIN)}}$$

$$f_{MAX2} = \left(1 - \frac{V_{OUT} + V_F}{V_{IN(MINCF)} - V_{SW} + V_F} \right) \cdot \frac{1}{t_{OFF(MIN)}}$$

The values of $t_{ON(MIN)}$ and $t_{OFF(MIN)}$ are functions of I_{SW} and temperature (see chart in the Typical Performance Characteristics section). Worst-case values for switch currents greater than 0.5A are $t_{ON(MIN)} = 130ns$ and

APPLICATIONS INFORMATION

$t_{OFF(MIN)} = 140ns$. f_{MAX1} is the frequency at which the minimum duty cycle is exceeded. The regulator will skip ON pulses in order to reduce the overall duty cycle at frequencies above f_{MAX1} . It will continue to regulate but with increased inductor current and greatly increased output ripple. The increased peak inductor current in pulse-skipping will also stress the switch transistor at high voltages and high switching frequency. f_{MAX2} is the frequency at which the maximum duty cycle is exceeded. If there is sufficient charge on the BST capacitor, the regulator will skip OFF periods to increase the overall duty cycle at frequencies above f_{MAX2} . It will continue to regulate but will not have constant-frequency operation.

Note that the restriction on the operating input voltage refers to steady-state limits to keep the output in regulation in constant-frequency mode; the circuit will tolerate input voltage transients up to the absolute maximum rating.

Switching Frequency

Once the upper limit for the switching frequency is found from the duty cycle requirements, the frequency may be chosen below the upper limit. Lower frequencies result in lower switching losses, but require larger inductors and capacitors. The user must decide the best trade-off. The switching frequency is set by a resistor connected from the R_T pin to ground, or by forcing a clock signal into the SYNC pin (LT3694 only). The LT3694 applies a voltage of 0.75V across this resistor and uses the current to set the oscillator speed. The switching frequency is given by the following formula:

$$f_{sw} = \frac{49.8}{R_T + 8.8}$$

where f_{sw} is in MHz and R_T is in $k\Omega$. The formula is accurate within $\pm 2\%$ over the frequency range. Table 1 shows the typical measured value of R_T for several common switching frequencies.

Table 1: R_T for Common Frequencies

SWITCHING FREQUENCY (MHz)	R_T (k)
0.25	193
0.5	90.2
0.75	56.6
1	40.2
1.25	30.5
1.5	23.8
1.75	19.6
2	16.0
2.25	13.5
2.5	11.4

For external clocks applied to the SYNC pin (LT3694 only), the circuit will support V_H logic levels from 1.8V to 5V CMOS or TTL. The duty cycle needs a minimum on time of 100ns and a minimum off time of 100ns. When operating in sync mode, R_T should be set to provide a frequency at least 20% below the minimum sync frequency.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_F}{1.25A \cdot f}$$

where f is the switching frequency in MHz, L is the inductor value in μH , V_{OUT} is the output voltage and V_F is the catch diode voltage drop.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3694 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3694 will deliver depends on the switch current limit, the inductor value and the input and output voltages. When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1 - DC) \frac{V_{OUT} + V_F}{L \cdot f}$$

APPLICATIONS INFORMATION

where f is the switching frequency of the LT3694 and L is the value of the inductor. The peak inductor and switch current is:

$$I_{SWPK} = I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3694's switch current limit, I_{LIM} . I_{LIM} is at least 3.5A at low duty cycles (0.1) and decreases linearly to 2.8A at DC = 0.8.

The minimum inductance can now be calculated as:

$$L_{MIN} = \frac{1 - DC_{MIN}}{2 \cdot f} \cdot \frac{V_{OUT} + V_F}{I_{LIM} - I_{OUT}}$$

However, it's generally better to use an inductor larger than the minimum value. The minimum inductor has large ripple currents which increase core losses and require large output capacitors to keep output voltage ripple low. Select an inductor greater than L_{MIN} that keeps the ripple current below 30% of I_{LIM} .

For input voltages greater than 30V, use an inductor with a saturation current of 6A or greater and an inductance value of 3.3μH or greater.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be greater than I_{LPK} . For highest efficiency, the series resistance (DCR) should be less than 0.1Ω. Table 2 lists several vendors and types that are suitable.

Table 2. Inductors

SERIES	INDUCTANCE RANGE (μH)	CURRENT RANGE (A)	MANUFACTURER
WE-HC	1 to 6.5	6 to 15	Würth Elektronik www.we-online.com
MSS1048	0.8 to 8	4 to 8	Coilcraft www.coilcraft.com
CDRH103R	0.8 to 10	2.8 to 8.3	Sumida www.sumida.com
VLF	2.2 to 10	3.8 to 7.7	TDK www.component.tdk.com
IHLP-2525CZ-11	1 to 10	2.5 to 9.5	Vishay www.vishay.com

This analysis is valid for continuous mode operation ($I_{OUT} > I_{LIM}/2$). For details of maximum output current in

discontinuous mode operation, see the Linear Technology Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations. This minimum inductance is:

$$L_{MIN} = \frac{(V_{OUT} + V_F)}{2A \cdot f_{SW}}$$

with L_{MIN} in μH and f_{SW} in MHz. A detailed discussion of subharmonic oscillations can be found in the Linear Technology Application Note 19.

Input Capacitor Selection

Bypass the input of the LT3694 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7μF to 22μF ceramic capacitor is adequate to bypass the LT3694 and will easily handle the ripple current. Use a 22μF capacitor with f_{SW} between 250kHz and 800kHz. Use a 10μF capacitor with f_{SW} between 800kHz and 1.6MHz. Use a 4.7μF capacitor above 1.6MHz. Always check for sufficient margin by reducing the capacitor value until the dropout increases by >500mV. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a lower performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3694 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 10μF capacitor is capable of this task, but only if it is placed close to the LT3694 and the catch diode (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3694. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3694 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3694's maximum input voltage rating. See Linear Technology Application Note 88 for more details.

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Output Capacitor Selection

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order to satisfy transient loads and stabilize the LT3694's control loop. Because the LT3694 operates at a high frequency, minimal output capacitance is necessary. In addition, the control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

Output ripple can be estimated with the following equations:

$$V_{\text{RIPPLE}} = \frac{\Delta I_L}{8 \cdot f \cdot C_{\text{OUT}}} \quad ; \text{ Ceramic}$$

$$V_{\text{RIPPLE}} = \Delta I_L \cdot \text{ESR} \quad ; \text{ Electrolytic}$$

where ΔI_L is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low so the RMS current rating of the output capacitor is usually not of concern. It can be estimated with the formula:

$$I_{\text{C(RMS)}} = \frac{\Delta I_L}{\sqrt{12}}$$

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor transfers to the output, the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{\text{OUT}} > 10 \cdot L \cdot \left(\frac{I_{\text{LIM}}}{V_{\text{OUT}}} \right)^2$$

The low ESR and small size of ceramic capacitors make them the preferred type for LT3694 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT} , this loss may be unacceptable. Use X7R and X5R types instead.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Surge rated tantalum capacitors or low ESR, organic, electrolytic capacitors intended for power supply use are suitable. Choose a capacitor with a sufficiently low ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 3 lists several capacitor vendors.

Table 3. Low ESR Surface Mount Capacitors

SERIES	TYPE	MANUFACTURER
	Ceramic	Taiyo Yuden www.t-yuden.com
TPM, TPS	Ceramic, Tantalum	AVX www.avx.com
T494, T495, T510, T520, T525, T530, A700	Ceramic, Tantalum, Tantalum Organic Polymer, Aluminum Organic Polymer	Kemet www.kemet.com
POSCAP, OS-CON	Tantalum Organic Polymer, Aluminum Organic Polymer	Sanyo www.sanyo.com
SP-CAP	Ceramic, Aluminum Organic Polymer	Panasonic www.panasonic.com
	Ceramic	TDK www.tdk.com

Diode Selection

The catch diode (D1 from Figure 1) conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{\text{D(AVG)}} = I_{\text{OUT}} \cdot \frac{V_{\text{IN}} - V_{\text{OUT}}}{V_{\text{IN}}}$$

Consider a diode with a larger current rating than $I_{\text{D(AVG)}}$ when the part must survive a shorted output. The DA pin monitors the current in the diode and prevents the switch from turning on at the beginning of a charge cycle if the diode current is above the DA limit. Therefore, under overload conditions, the average diode current will increase to the average of the switch current limit and the DA current limit.

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Peak reverse voltage is equal to the regulator input voltage, so use a diode with a reverse voltage rating greater than the maximum input voltage. The internal OVLO can protect the diode from excessive reverse voltage by shutting down the regulator if the input voltage exceeds 38V. Table 4 lists several Schottky diodes and their manufacturers.

Table 4. Schottky Diodes (40V, 3A)

PART NUMBER	V _f at 3A (V)	OUTLINE	MANUFACTURER
MBRS340	0.5	SMC	ON Semiconductor
MBRD340	0.6	D-PAK	www.onsemi.com
B340	0.5	SMC	Diodes, Inc.
SMB340	0.5	Powermite 3	www.diodes.com
CMSH3-40	0.5	SMC	Central Semiconductor
CSDH3-40	0.65	D-PAK	www.centralsemi.com

Frequency Compensation

The LT3694 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3694 does not require the ESR of the output capacitor for stability, so the user is free to employ ceramic capacitors to achieve low output ripple and small circuit size. Frequency compensation is provided by the components tied to the V_C pin, as shown in Figure 2. Generally a capacitor (C_C) and a resistor (R_C) in series to ground are used. In addition, there may be lower value capacitor in parallel. This capacitor (C_F) is not part of the loop compensation but is used to filter noise at the switching frequency, and is required only if a phase-lead capacitor (C_{PL}) is used or if the output capacitor (C1) has high ESR.

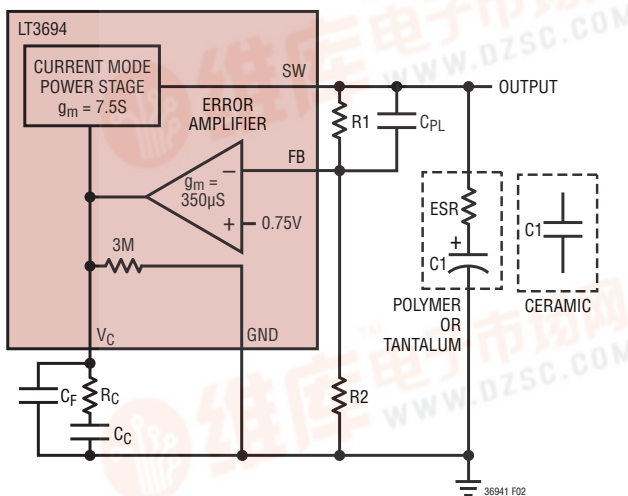


Figure 2. Model for Loop Response

Loop compensation determines the stability and transient performance. The best values for the compensation network depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load. Figure 2 shows an equivalent circuit for the LT3694 control loop. The error amplifier is a transconductance amplifier with finite output impedance.

The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_{C1} pin. Note that the output capacitor integrates this current, and that the capacitor on the V_{C1} pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the output capacitor ESR or from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response.

Figure 3 shows the transient response when the load current steps from 1A to 2.6A and back to 1A.

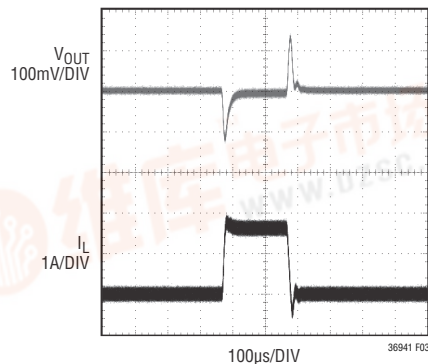


Figure 3. Transient Load Response of the LT3694 Front Page Application as the Load Current Is Stepped from 1A to 2.6A. V_{OUT} = 3.3V

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BST and BIAS Pin Considerations

Capacitor C3 and the internal boost Schottky diode (see the Block Diagram in Figure 1) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.22 μ F capacitor will work well. Figure 4 shows three ways to arrange the boost circuit. The BST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of 3V and above, the standard circuit (Figure 4a) is best. For outputs between 2.8V and 3V, use a 1 μ F boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage while using the internal boost diode. For reliable BST pin operation with 2.5V outputs, use a good external Schottky diode (such as the ON Semi MBR0540), and a 1 μ F boost capacitor (see Figure 4b). For lower output voltages, the BIAS pin can be tied to the input (Figure 4c), or to another supply greater than 2.8V. Tying BIAS to V_{IN} reduces the maximum input voltage to 7V. The circuit in Figure 4a is more efficient because the BST pin current and BIAS pin

quiescent current comes from a lower voltage source. One must also ensure that the maximum voltage ratings of the BST and BIAS pins are not exceeded. The minimum operating voltage of an LT3694 application is limited by the minimum input voltage (4V) and by the maximum duty cycle as outlined in a previous section. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3694 is turned on with its EN/UVLO or TRK/SS pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 5 shows a plot of input voltage to start and to run as a function of load current. In many cases the discharged output capacitor

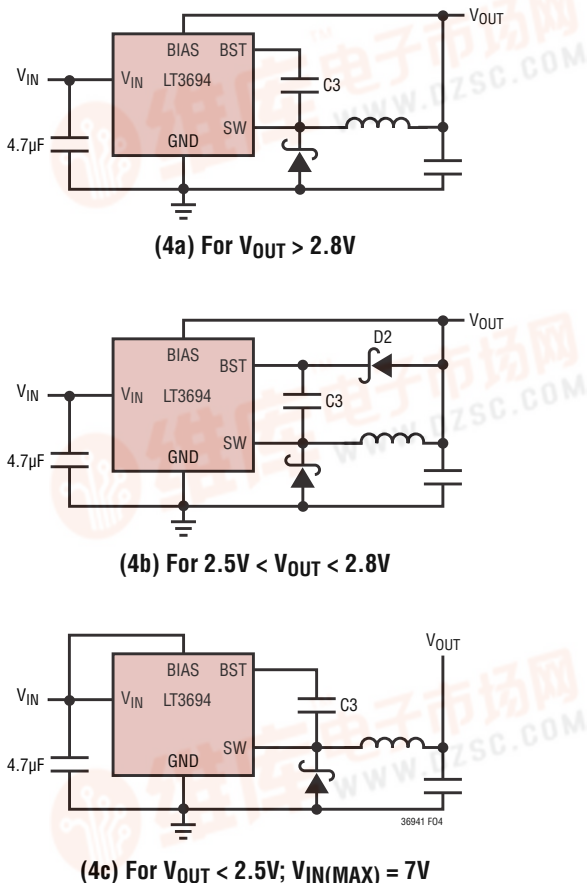


Figure 4. Three Circuits for Generating the Boost Voltage

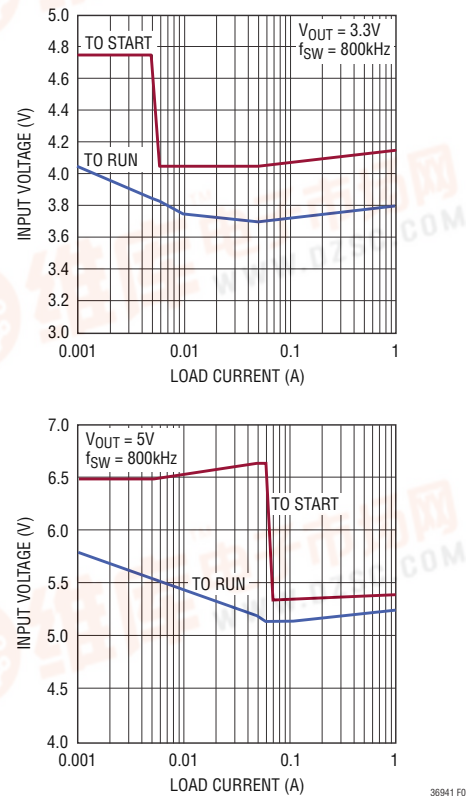


Figure 5. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

APPLICATIONS INFORMATION

will present a load to the switcher, which will allow it to start. The plots show the worst-case situation in which V_{IN} is ramping very slowly. For lower start-up voltage, the boost diode can be tied to V_{IN} , however, this restricts the input range to one-half of the absolute maximum rating of the BST pin.

At light loads, the inductor current becomes discontinuous and the effective duty cycle can be very high. This reduces the minimum input voltage to approximately 300mV above V_{OUT} . At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3694, requiring a higher input voltage to maintain regulation.

Internal Undervoltage Lockout

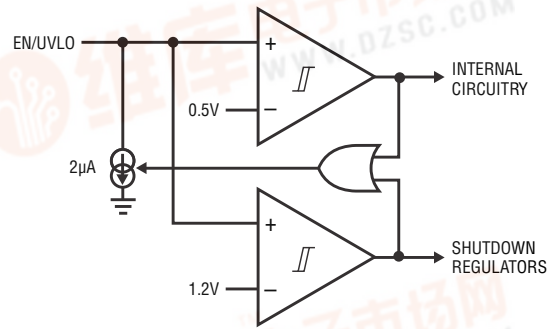
The LT3694 features an internal undervoltage lockout that will shut off all three regulators if the input voltage drops too low to maintain regulation of the internal circuitry. This lockout trips when V_{IN} drops below 3.8V (typ).

Enable and Programmable Undervoltage Lockout

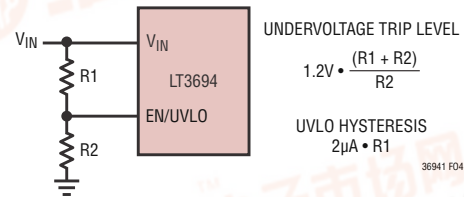
The EN/UVLO pin provides both logic enable and programmable undervoltage lockout functions. There are two thresholds on the EN/UVLO pin. The first threshold is at 500mV (typ). When EN/UVLO is below this threshold, the LT3694 is in complete shutdown and the quiescent current drops below 2μA.

Once EN/UVLO climbs above the first threshold, the internal circuitry of the LT3694 is turned on but the switching regulator and LDOs remain shut off. A 2μA current sink on the EN/UVLO pin is activated to provide hysteresis for the programmable undervoltage function.

The second threshold is an accurate 1.2V derived from the internal reference. When EN/UVLO is above the second threshold, the regulators turn on and the 2μA current sink turns off. This allows an accurate programmable UVLO function by placing a resistor divider between V_{IN} , EN/UVLO and ground. Figure 6a shows the EN/UVLO block diagram and Figure 6b shows connections for the programmable UVLO function.



(6a) EN/UVLO Block Diagram



(6b) Programmable UVLO Application

Figure 6. Programmable UVLO Application

The trip level is set by the resistor ratio:

$$V_{IN(UVTRIP)} = 1.2V \left(\frac{R1 + R2}{R2} \right)$$

The hysteresis is set by R1:

$$V_{IN(UVHYS)} = 2\mu A \cdot R1$$

The EN/UVLO pin may be driven with a logic output if the programmable UVLO is not needed. The requirements for the logic output are a low output voltage less than 0.35V (to insure low current shutdown) and a high output voltage greater than 1.25V.

Low Dropout Regulator

Each low dropout regulator comprises an error amp, loop compensation and a base drive amp. It uses the same 0.75V reference as the switching regulators. It requires an external NPN pass transistor and 2.2μF of output capacitance for stability.

The dropout characteristics will be determined by the pass transistor. The collector-emitter saturation characteristics

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PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 9 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3694's V_{IN} , DA, and SW pins, the catch diode (D1) and the input capacitor (C_{IN}). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BST nodes should be as small as possible. Finally, keep the FB and V_C nodes small

so that the ground traces will shield them from the SW and BST nodes.

The exposed pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the top side ground plane as much as possible, and add thermal vias under and near the LT3694 to additional ground planes within the circuit board and on the bottom side.

High Temperature Considerations

The PCB must provide heat sinking to keep the LT3694 cool. The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these lay-

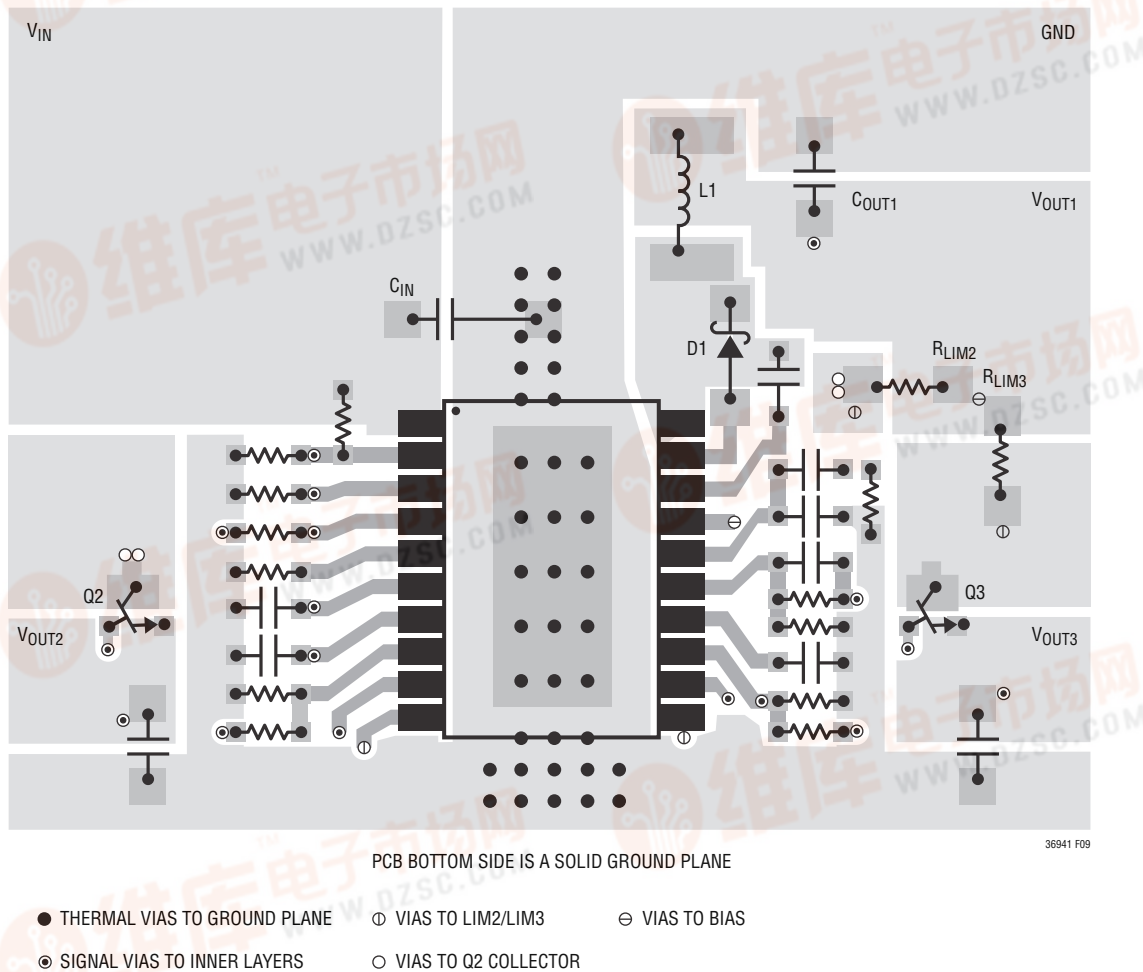


Figure 9. A Good PCB Layout Ensures Proper, Low EMI Operation

APPLICATIONS INFORMATION

ers will spread the heat dissipated by the LT3694. Place additional vias to reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to $\theta_{JA} = 34^{\circ}\text{C}/\text{W}$ (UFD) or $\theta_{JA} = 38^{\circ}\text{C}/\text{W}$ (FE20). With 100 LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance.

Because of the large output current capability of the LT3694, it is possible to dissipate enough heat to raise the junction temperature beyond the absolute maximum. When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches $T_{J(\text{MAX})}$.

Power dissipation within the LT3694 can be estimated by calculating the total power loss from an efficiency

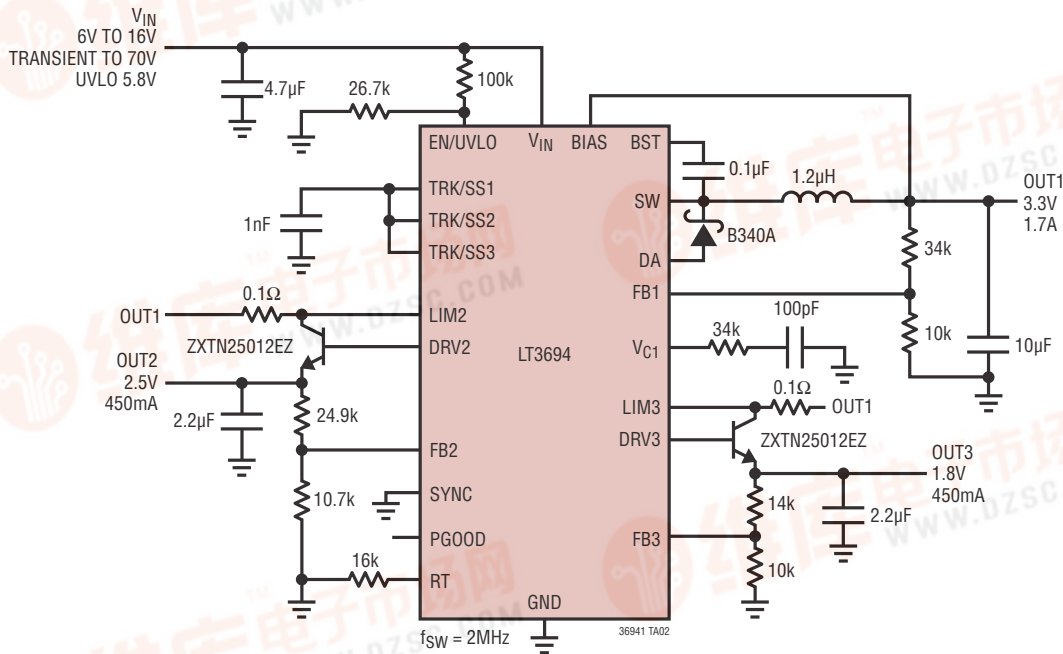
measurement and subtracting the catch diode loss and inductor loss. The die temperature is calculated by multiplying the LT3694 power dissipation by the thermal resistance from junction-to-ambient. Keep in mind other heat sources—such as the catch diode, inductor and LDO pass transistors.

Other Linear Technology Publications

Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

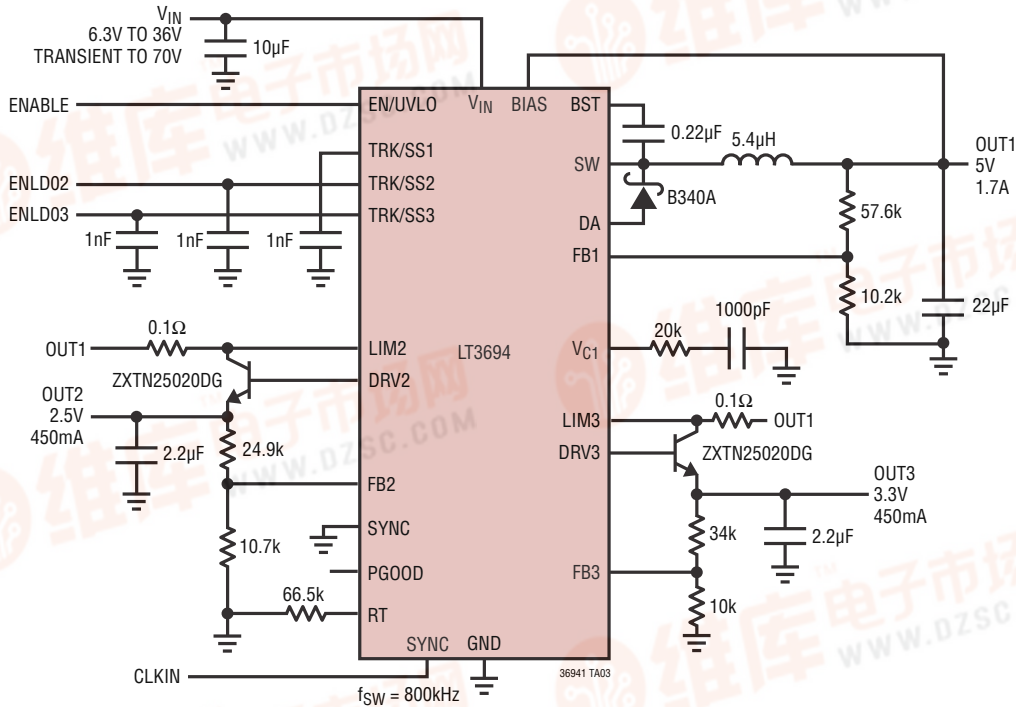
TYPICAL APPLICATIONS

Automotive Input Range (6V to 16V) to 3.3V, 2.5V, 1.8V

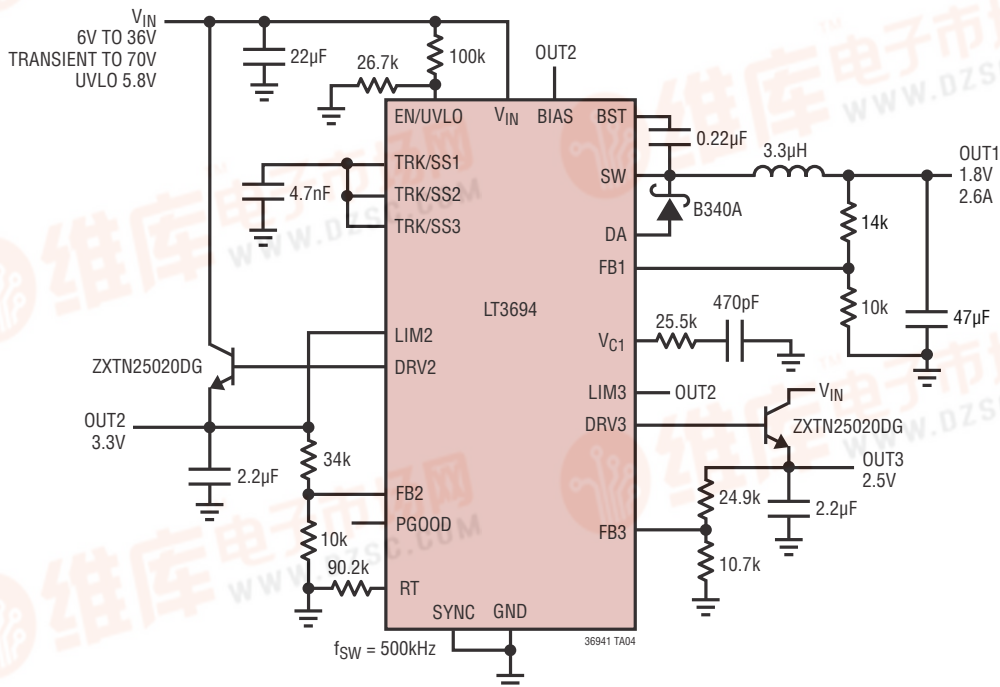


TYPICAL APPLICATIONS

Wide Input Range to (6.3V to 36V) to 5V, 3.3V, 2.5V With Independent On/Off Control of the LDOs



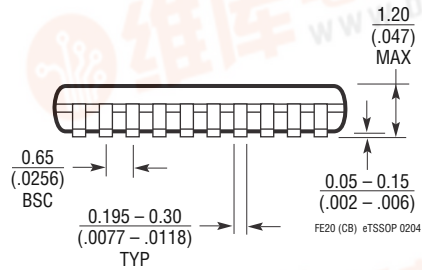
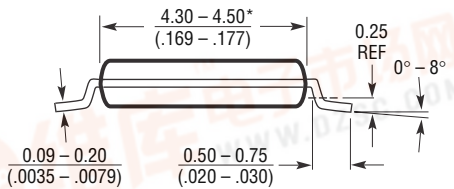
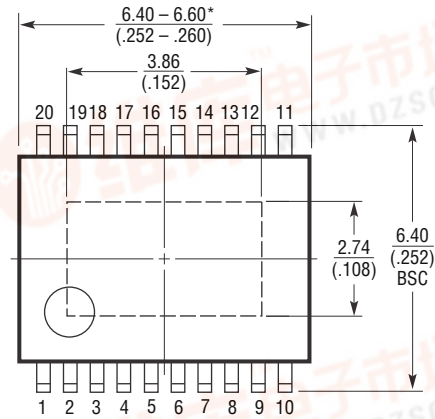
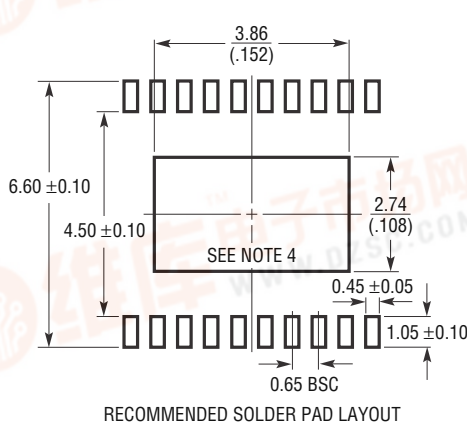
Wide Input Range (6V to 36V) to 1.8V, 2.5V and 3.3V



THE LDO OUTPUT CURRENT CAPABILITY IS LIMITED BY THE POWER DISSIPATION OF THE NPN PASS TRANSISTORS

PACKAGE DESCRIPTION

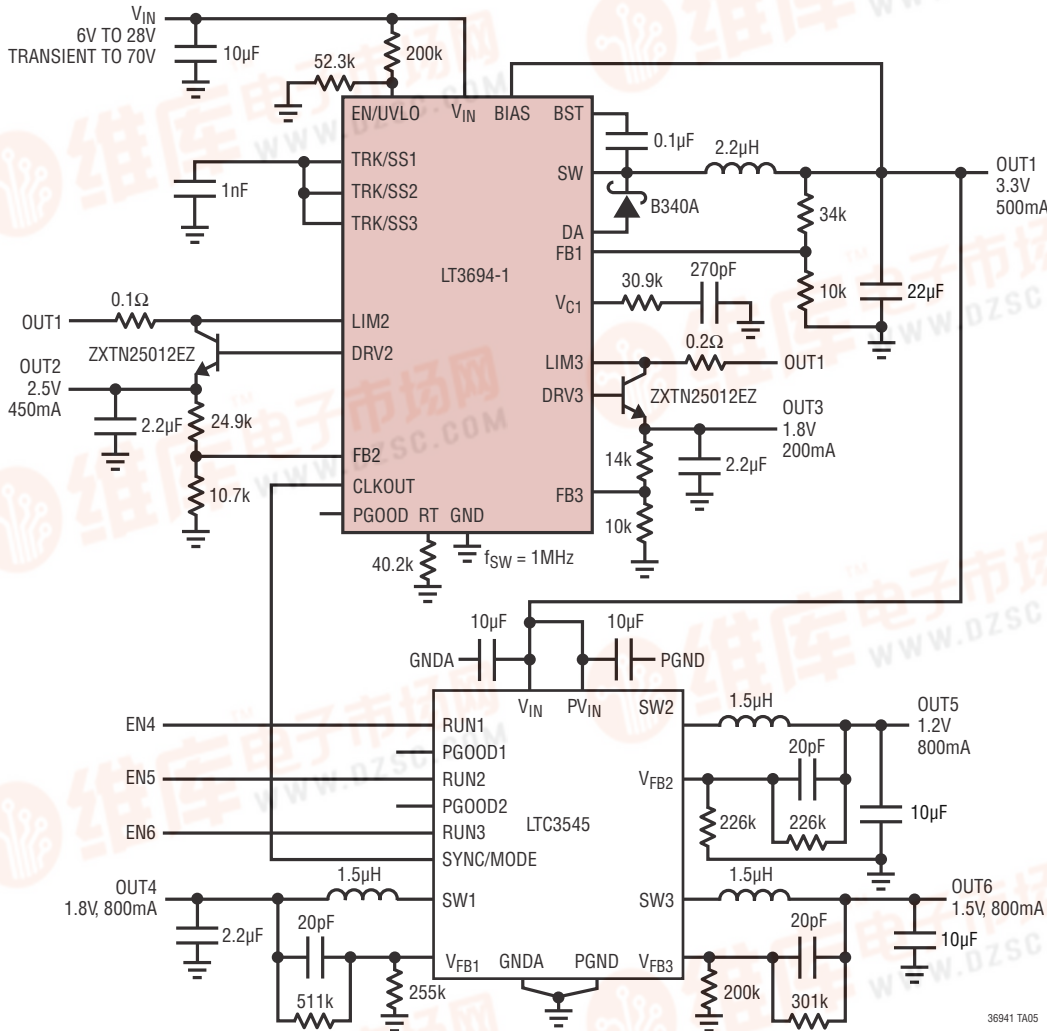
FE Package
20-Lead Plastic TSSOP (4.4mm)
 (Reference LTC DWG # 05-08-1663)
Exposed Pad Variation CB



- NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
 2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{INCHES}}$
 3. DRAWING NOT TO SCALE
 4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
- *DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

6V to 28V Input Range with Cascaded Step Down — 3.3V, 2.5V and 1.8V Outputs Plus Independently Enabled 1.8V, 1.5V and 1.2V Outputs



36941 TA05

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3480	36V with Transient Protection to 60V, 2A (I _{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode [®] Operation	V _{IN} : 3.6V to 38V, V _{OUT(MIN)} = 0.78V, I _Q = 70μA, I _{SD} < 1μA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3500	36V, 40V _{MAX} , 2A, 2.5MHz High Efficiency Step-Down DC/DC Converter and LDO Controller	V _{IN} : 3.6V to 36V, V _{OUT(MIN)} = 0.8V, I _Q = 2.5mA, I _{SD} < 10μA, 3mm × 3mm DFN-10 Package
LT3507	36V, 2.5MHz, Triple (2.4A + 1.5A + 1.5A (I _{OUT})) with LDO Controller High Efficiency Step-Down DC/DC Converter	V _{IN} : 4V to 36V, V _{OUT(MIN)} = 0.8V, I _Q = 7mA, I _{SD} < 1μA, 5mm × 7mm QFN-38 Package
LT3685	36V with Transient Protection to 60V, 2A (I _{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V _{IN} : 3.6V to 38V, V _{OUT(MIN)} = 0.78V, I _Q = 70μA, I _{SD} < 1μA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3970	40V, 350mA, 2MHz High Efficiency Micropower Step-Down DC/DC Converter	V _{IN} : 4V to 40V, Transient to 60V, V _{OUT(MIN)} = 1.21V, I _Q = 2μA, I _{SD} < 1μA, 3mm × 2mm DFN-10 and MSOP-10 Packages
LT3980	58V with Transient Protection to 80V, 2A (I _{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V _{IN} : 3.6V to 58V, Transient to 80V, V _{OUT(MIN)} = 0.8V, I _Q = 85μA, I _{SD} < 1μA, 3mm × 4mm DFN-16 and MSOP-16E Packages