



Obsolete Device

4K (512 x 8) CMOS EEPROM

PACKAGE TYPES

-
- The image displays two pinout diagrams for the 28C04A EPROM. The top diagram is for the DIP (Dual In-line Package) version, showing a 28-pin configuration with pins 1 through 14 on the left and pins 13 through 0 on the right. The bottom diagram is for the PLCC (Pin Grid Array) version, showing a 28-pin configuration with pins 1 through 14 on the left and pins 13 through 0 on the right. Both diagrams include a pin 1 indicator (a dot) and a central label '28C04A'.
- DIP Pinout:**
- | Pin | Signal |
|-----|------------------|
| 1 | V _{CC} |
| 2 | A ₆ |
| 3 | A ₅ |
| 4 | A ₄ |
| 5 | A ₃ |
| 6 | A ₂ |
| 7 | A ₁ |
| 8 | A ₀ |
| 9 | I/O ₀ |
| 10 | I/O ₁ |
| 11 | I/O ₂ |
| 12 | V _{SS} |
| 13 | I/O ₃ |
| 14 | I/O ₄ |
| 15 | I/O ₅ |
| 16 | I/O ₆ |
| 17 | I/O ₇ |
| 18 | CE |
| 19 | NC |
| 20 | OE |
| 21 | WE |
| 22 | NC |
| 23 | A ₈ |
| 24 | V _{CC} |
- PLCC Pinout:**
- | Pin | Signal |
|-----|------------------|
| 1 | V _{CC} |
| 2 | NC |
| 3 | NC |
| 4 | A ₇ |
| 5 | A ₆ |
| 6 | A ₅ |
| 7 | A ₄ |
| 8 | A ₃ |
| 9 | A ₂ |
| 10 | A ₁ |
| 11 | A ₀ |
| 12 | NC |
| 13 | I/O ₀ |
| 14 | I/O ₁ |
| 15 | I/O ₂ |
| 16 | I/O ₃ |
| 17 | I/O ₄ |
| 18 | I/O ₅ |
| 19 | I/O ₆ |
| 20 | I/O ₇ |
| 21 | CE |
| 22 | NC |
| 23 | OE |
| 24 | NC |
| 25 | WE |
| 26 | NC |
| 27 | NC |
| 28 | NC |
| 29 | A ₈ |
| 30 | V _{CC} |
- Pin 1 indicator on PLCC on top of package

BLOCK DIAGRAM

[illegible]

1.0 ELECTRICAL CHARACTERISTICS

1.1 MAXIMUM RATINGS*

V_{CC} and input voltages w.r.t. V_{SS} -0.6V to + 6.25V
Voltage on $\overline{OE}$ w.r.t. V_{SS}.....-0.6V to +13.5V
Output Voltage w.r.t. V_{SS}-0.6V to V_{CC}+0.6V
Storage temperature-65°C to +125°C
Ambient temp. with power applied-50°C to +95°C

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0 - A8	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
V _{CC}	+5V Power Supply
V _{SS}	Ground
NC	No Connect; No Internal Connection
NU	Not Used; No External Connection is Allowed

TABLE 1-2: READ/WRITE OPERATION DC CHARACTERISTICS

V _{CC} = +5V ±10% Commercial (C): T _{amb} = 0°C to +70°C Industrial (I): T _{amb} = -40°C to +85°C						
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1'	V _{IH}	2.0	V _{CC} +1	V	
	Logic '0'	V _{IL}	-0.1	0.8	V	
Input Leakage		I _{LI}	-10	10	μA	V _{IN} = -0.1V to V _{CC} +1
Input Capacitance		C _{IN}		10	pF	V _{IN} = 0V; T _{amb} = 25°C; f = 1 MHz
Output Voltages	Logic '1'	V _{OH}	2.4		V	I _{OH} = -400 μA I _{OL} = 2.1 mA
	Logic '0'	V _{OL}		0.45	V	
Output Leakage		I _{LO}	-10	10	μA	V _{OUT} = -0.1V to V _{CC} + 0.1V
Output Capacitance		C _{OUT}		12	pF	V _{IN} = 0V; T _{AMB} = 25°C; f = 1 MHz
Power Supply Current, Active	TTL input	I _{CC}		30	mA	f = 5 MHz (Note 1) V _{CC} = 5.5V
Power Supply Current, Standby	TTL input	I _{CC} (s) _{TTL}		2	mA	$\overline{CE}$ = V _{IH} (0°C to +70°C) $\overline{CE}$ = V _{IH} (-40°C to +85°C) $\overline{CE}$ = V _{CC} -0.3 to V _{CC} +1 $\overline{OE}$ = V _{CC} All inputs equal V _{CC} or V _{SS}
	TTL input	I _{CC} (s) _{TTL}		3	mA	
	CMOS input	I _{CC} (s) _{CMOS}		100	μA	

Note 1: AC power supply current above 5 MHz; 1 mA/MHz.

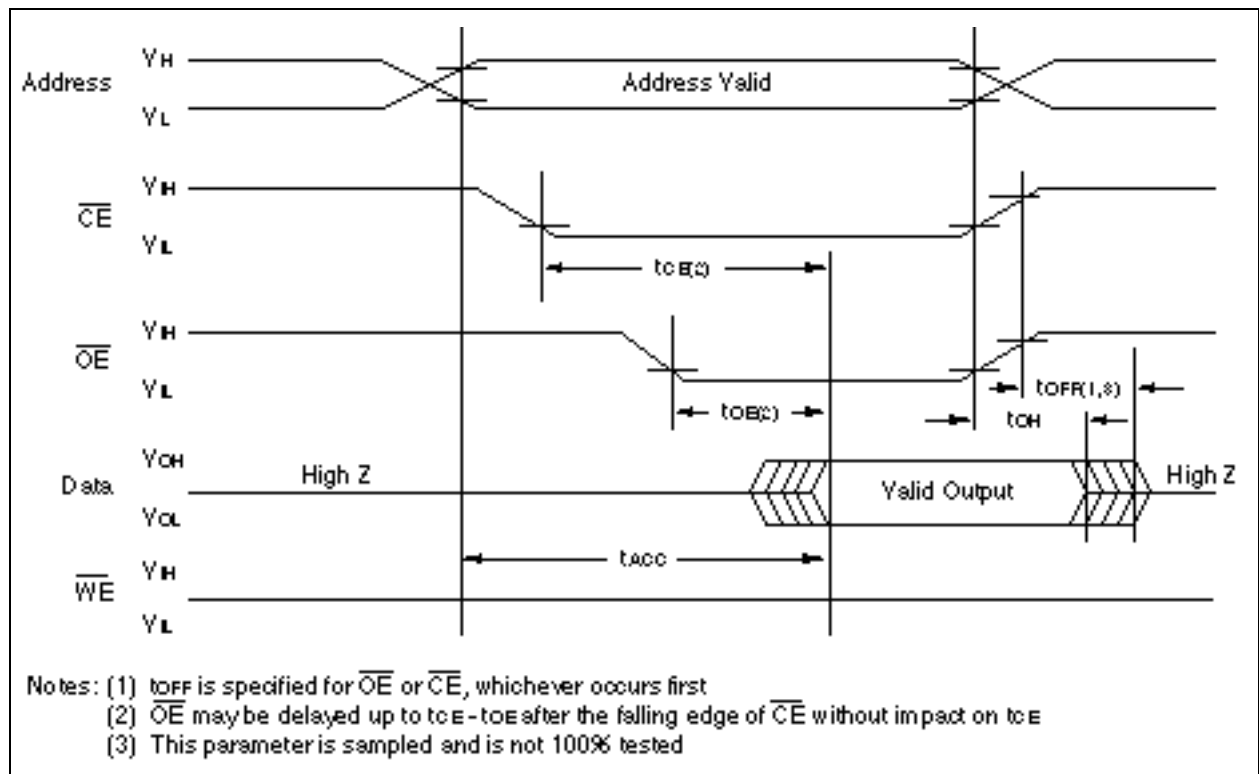
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TABLE 1-3: READ OPERATION AC CHARACTERISTICS

		AC Testing Waveform:		V _{IH} = 2.4V; V _{IL} = 0.45V; V _{OH} = 2.0V; V _{OL} = 0.8V					
		Output Load:		1 TTL Load + 100 pF					
		Input Rise and Fall Times:		20 ns					
		Ambient Temperature:		Commercial (C): Tamb = 0°C to +70°C					
				Industrial (I): Tamb = -40°C to +85°C					
Parameter	Sym	28C04A-15		28C04A-20		28C04A-25		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t _{ACC}		150		200		250	ns	$\overline{OE} = \overline{CE} = V_{IL}$
$\overline{CE}$ to Output Delay	t _{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t _{OE}		70		80		100	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ to $\overline{OE}$ High Output Float	t _{OFF}	0	50	0	55	0	70	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurs first	t _{OH}	0		0		0		ns	
Endurance	—	1M	—	1M	—	1M	—	cycles	25°C, V _{CC} = 5.0V, Block Mode (Note)

Note: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS

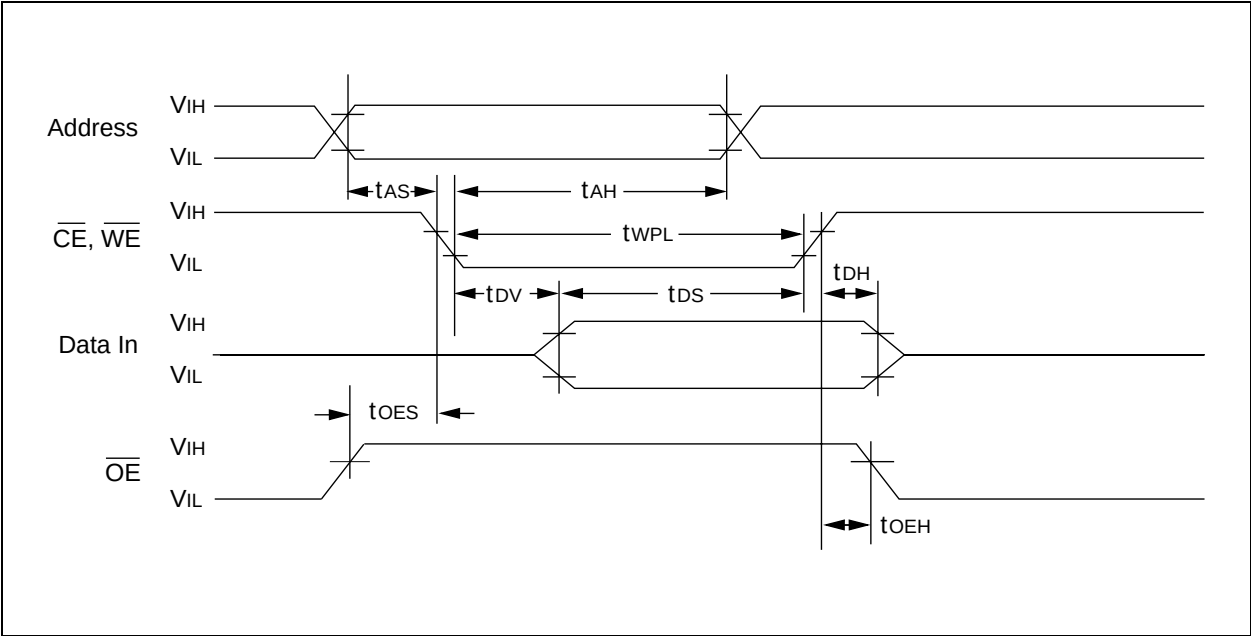


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TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

		AC Testing Waveform: Output Load: Input Rise/Fall Times: Ambient Temperature:		V _{IH} = 2.4V; V _{IL} = 0.45V; V _{OH} = 2.0V; V _{OL} = 0.8V 1 TTL Load + 100 pF 20 nsec Commercial (C): Tamb= 0°C to 70°C Industrial (I): Tamb= -40°C to 85°C	
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t _{AS}	10		ns	
Address Hold Time	t _{AH}	50		ns	
Data Set-Up Time	t _{DS}	50		ns	
Data Hold Time	t _{DH}	10		ns	
Write Pulse Width	t _{WPL}	100		ns	Note 1
Write Pulse High Time	t _{WPH}	50		ns	
$\overline{\text{OE}}$ Hold Time	t _{OE H}	10		ns	
$\overline{\text{OE}}$ Set-Up Time	t _{OE S}	10		ns	
Data Valid Time	t _{DV}		1000	ns	Note 2
Write Cycle Time (28C04A)	t _{WC}		1	ms	0.5 ms typical
Write Cycle Time (28C04AF)	t _{WC}		200	μs	100 μs typical

- Note 1: A write cycle can be initiated by $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs first.
- 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS



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FIGURE 1-3: DATA POLLING WAVEFORMS

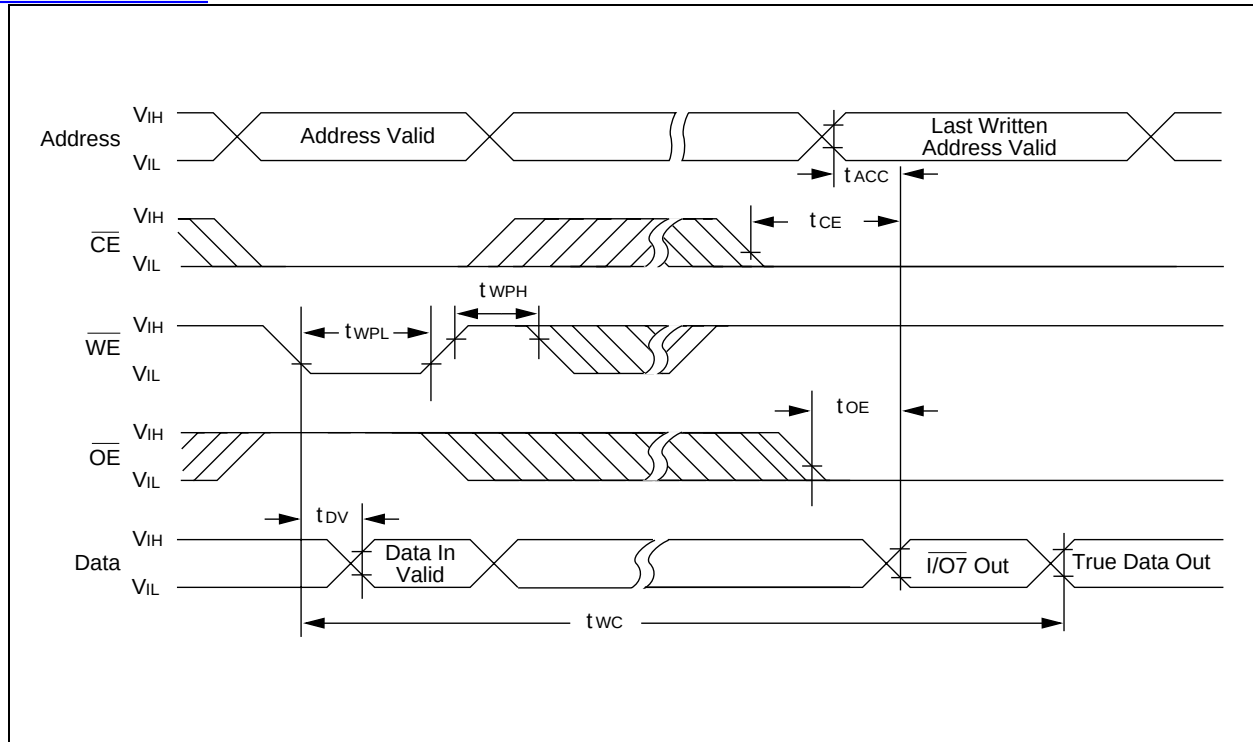
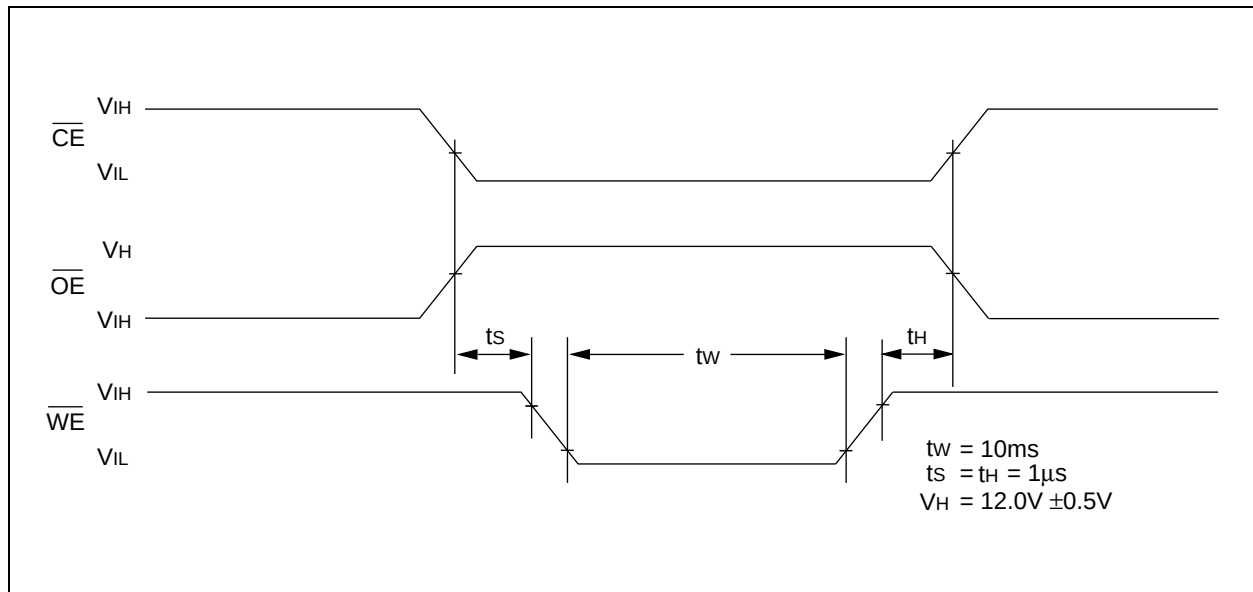


FIGURE 1-4: CHIP CLEAR WAVEFORMS



2.0 DEVICE OPERATION

The Microchip Technology Inc. 28C04A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{\text{CE}}$	$\overline{\text{IE}}$	$\overline{\text{WE}}$	I/O
Read	L	L	H	DOUT
Standby	H	X	X	High Z
Write Inhibit	H	X	X	High Z
Write Inhibit	X	L	X	High Z
Write Inhibit	X	X	H	High Z
Byte Write	L	H	L	DIN
Byte Clear	Automatic Before Each "Write"			

X = Any TTL level.

2.1 Read Mode

The 28C04A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{\text{ACC}} - t_{\text{OE}}$.

2.2 Standby Mode

The 28C04A is placed in the standby mode by applying a high signal to the $\overline{\text{CE}}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal Vcc detect (3.3 volts typical) will inhibit the initiation of non-volatile programming operation when Vcc is less than the Vcc detect circuit trip.

Second, there is a $\overline{\text{WE}}$ filtering circuit that prevents $\overline{\text{WE}}$ pulses of less than 10 ns duration from initiating a write cycle.

Third, holding $\overline{\text{WE}}$ or $\overline{\text{CE}}$ high or $\overline{\text{OE}}$ low, inhibits a write cycle during power-on and power-off (Vcc).

2.4 Write Mode

The 28C04A has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{\text{WE}}$ pin. On the falling edge of $\overline{\text{WE}}$, the address information is latched. On rising edge, the data and the control pins ($\overline{\text{CE}}$ and $\overline{\text{OE}}$) are latched.

2.5 Data Polling

The 28C04A features Data polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 are indeterminate). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{\text{OE}}$ to 12 volts and bringing the $\overline{\text{WE}}$ and $\overline{\text{CE}}$ low. This procedure clears all data.

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



28C04A

[NOTES: 本海28C04A供应商](#)

Note the following details of the code protection feature on Microchip devices:

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