Dual P-Channel 30V (D-S) MOSFET

Features

-30V/-4.5A,RDS(ON)=60mΩ@VGS=-10V
-30V/-4.2A,RDS(ON)=90mΩ@VGS=-4.5V
Super high density cell design for extremely low RDS(ON)
Exceptional on-resistance and maximum DC current capability

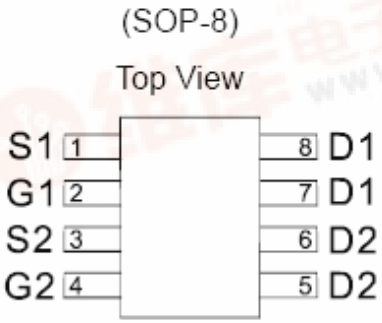
Applications

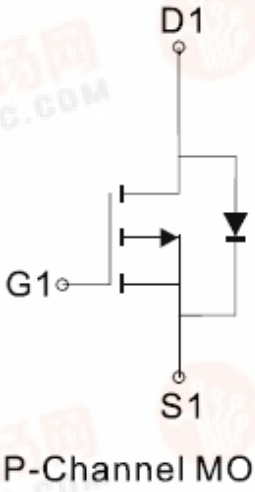
Power Management in Note book
Portable Equipment
Battery Powered System
DC/DC Converter
Load Switch
DSC
LCD Display inverter

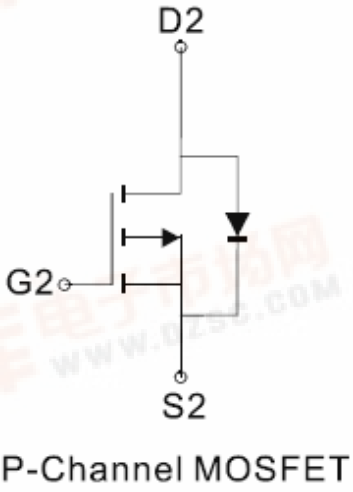
General Description

The Z4953 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Pin Configurations







- **Absolute Maximum Ratings** @T_A=25℃ unless otherwise noted

Parameter		Symbol	Limits	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (tj=150)	Ta=25	I_D	-4.5	A
	Ta=70		-4.2	
Pulsed Drain Current[1)]		I_{DM}	-30	A
Continuous Drain Current (Diode Conduction)		I_s	-1.7	A
Maximum Power Dissipation	T_A=25	P_D	2.0	W
	T_A=70		1.3	
Operating Junction Temperature		T_J	-55 to 150	℃
Storage Temperature Range		T_{stg}	-55 to 150	℃
Thermal Resistance- Junction-to-Ambient *		R_{JA}	47	W
			Steady State 75	
Thermal Resistance- Junction-to-Case		R_{Jc}	45	W

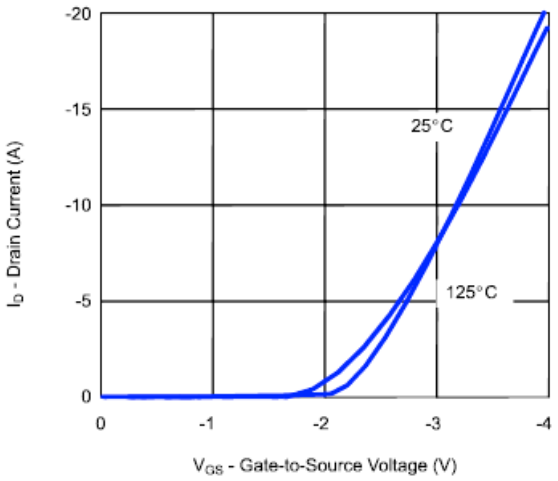
Notes: *The device mounted on 1in2 FR4 board with 2 oz copper

- **Electrical Characteristics** @TA=25℃ unless otherwise Specified

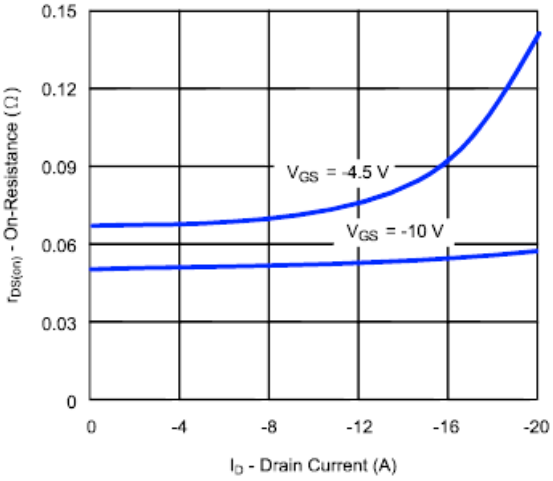
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} =VGS, I_D=-250 A	-1	-1.4	-3	V
I_{GSS}	Gate Leakage Current	V_{DS} = 0V, V_{GS} =±20V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -30V, V_{GS} = 0V	-	-	-1	A
		V_{DS} = -30V, V_{GS} = 0V,Tj=55	-	-	-25	
$I_{D(ON)}$	On-State Drain Current	V_{DS} = -5V, V_{GS} = -10V	-20	-	-	A
$R_{D(ON)}$	Drain-Source On-Resistance	V_{GS} =-10V, I_D= -4.5 A	-	50	60	MA
		V_{GS} =-4.5V, I_D= -4.2 A	-	69	90	
V_{SD}	Diode Forward Voltage	I_S=-1.7A, V_{GS}=0V	-	-0.8	-1.2	V
Dynamic						
R_g	Gate resistance	VDS=0V, VGS=0V, f=1MHz	-	3.5	-	Ω
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=-0V,f=1MHz	-	450	490	pF
Coss	Output Capacitance		-	70	-	
Crss	Reverse Transfer Capacitance		-	20	-	
Qg	Total Gate Charge	VDS=-15V, VGS=-10V, ID=-4.5A	-	14	17	nC
Qgs	Gate-Source Charge		-	4	-	
Qgd	Gate-Drain Charge		-	3	-	
$t_{D(on)}$	Turn-On Delay Time	V_{DD}= -15V, R_L = 15Ω I_D = -1A, V_{GEN}=-10V R_G = 6Ω	-	27	33	ns
t_r	Turn-On Rise Time		-	11	15	
$t_{D(off)}$	Turn-Off Delay Time		-	40	52	
t_f	Turn-Off Fall Time		-	4	6	

- **Typical Performance Characteristics (Tj=25)**

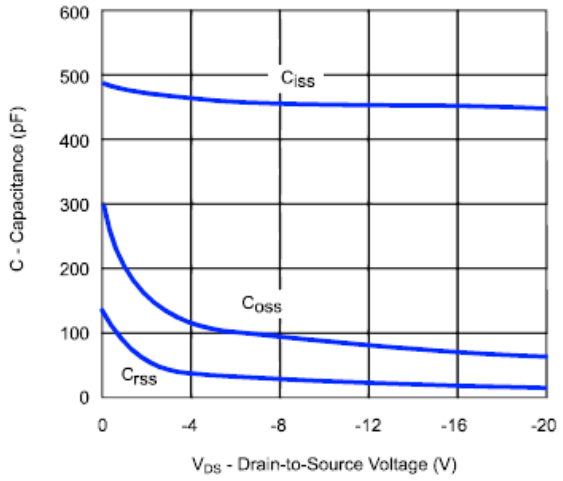
Transfer Characteristics



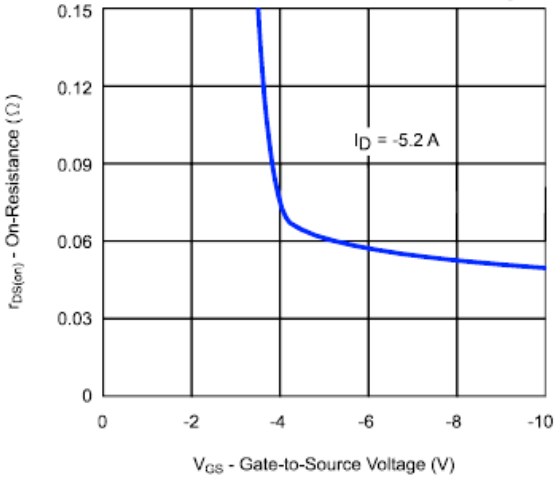
On-Resistance vs. Drain Current



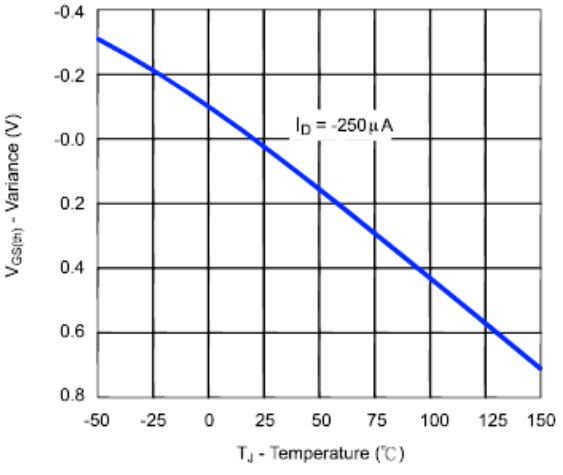
Capacitance



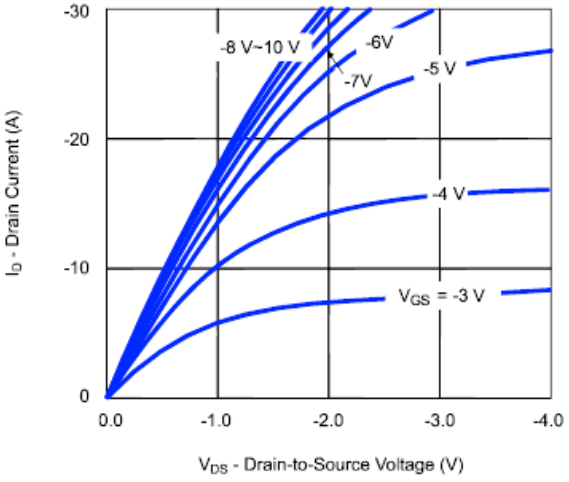
On-Resistance vs. Gate-to-Source Voltage



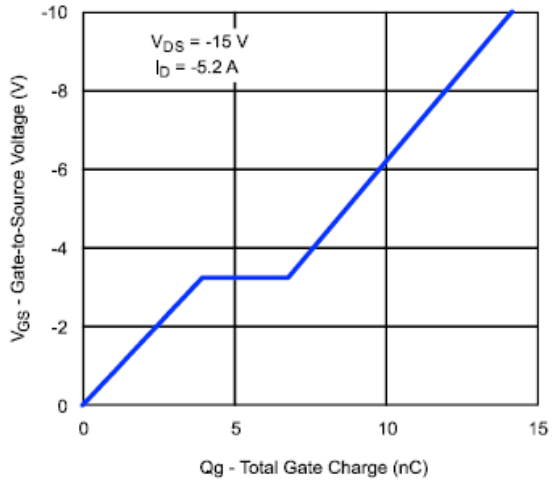
Threshold Voltage



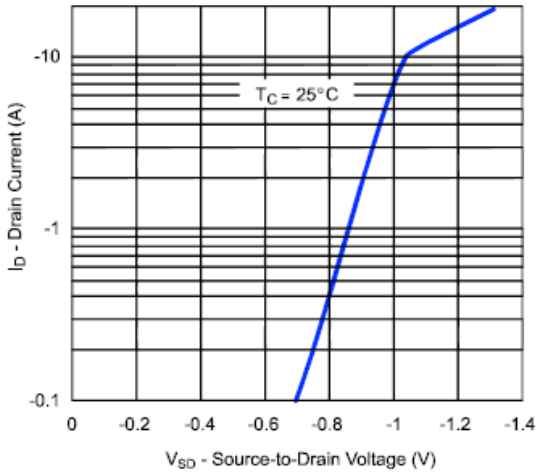
On-Region Characteristics



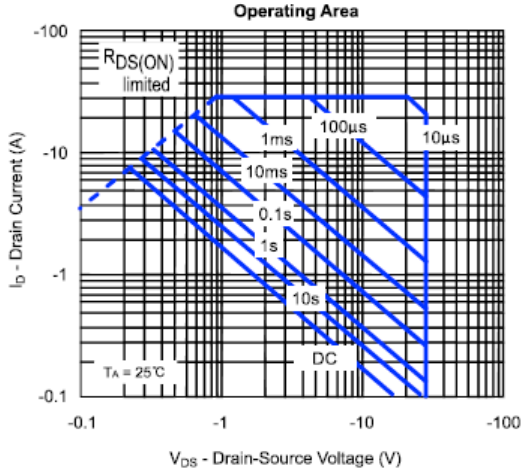
Gate Charge



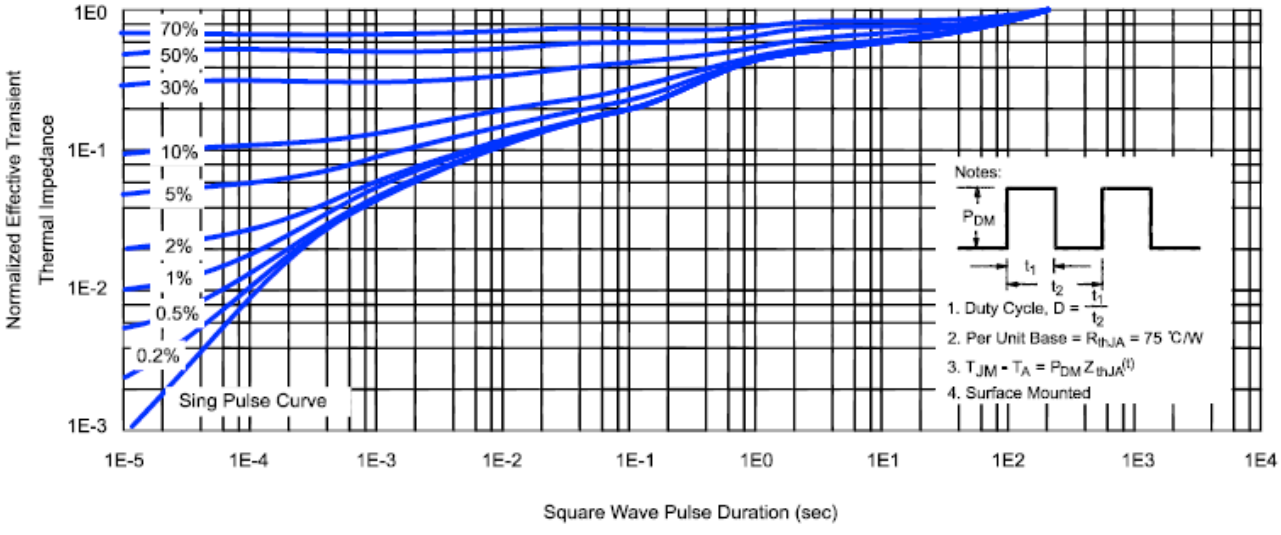
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area

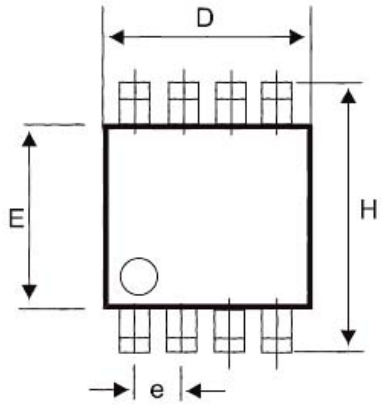


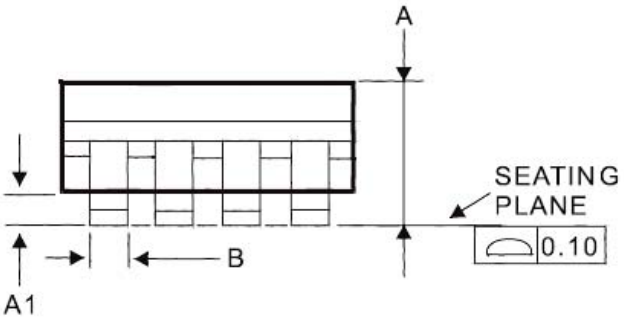
Normalized Thermal Transient Impedance, Junction-to-Ambient

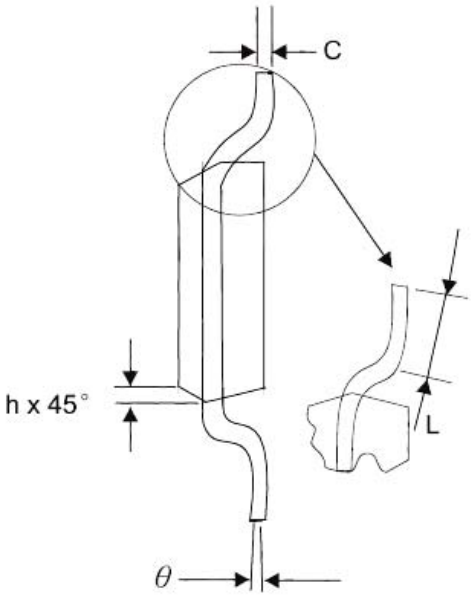


- **Package Information**

SOP-8 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.50
A1	0.10	0.20
B	0.013	0.42
C	0.026	1.50
D	0.189	4.95
E	3.82	3.98
e	0.050 BSC	
H	0.232	6.15
h	0.55	0.75
L	0.020	0.030

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