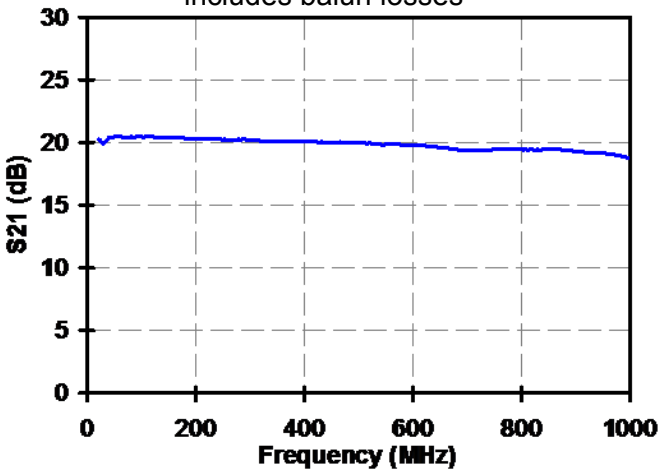
TGA2806-SM

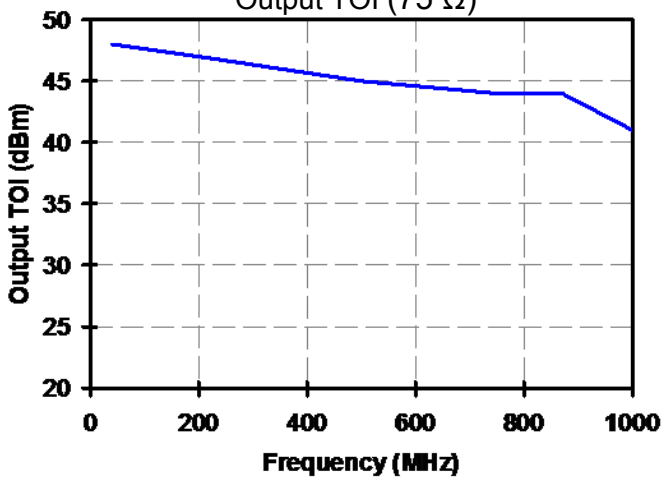
CATV Linear Amplifier

Measured Performance

Small Signal Gain (75 Ω)
includes balun losses



Output TOI (75 Ω)



Key Features

- Frequency Range: 40MHz - 1GHz
- Gain: 20 dB
- 1.7 dB 75 Ω Noise Figure
- Ultra-Low Distortion (45dBm IP3 typ.)
- Low DC Power Consumption
- Single Supply Bias (+8V)
- 28L Package Dimension: 5.0 x 5.0 x 0.85 mm

Primary Applications

- CMTS Equipment
- CATV Line Amplifiers

Product Description

The TriQuint TGA2806-SM is an ultra-linear, packaged Gain Block which operates from 40MHz to 1000MHz.

The TGA2806-SM typically provides flat gain along with ultra-low distortion. It also provides high output power with low DC power consumption.

This amplifier is ideally suited for use in CATV distribution systems or other applications requiring extremely low noise and distortion.

Demonstration Boards are available.

Lead-free and RoHS compliant.

Datasheet subject to change without notice.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	11 V	
Vd1, Vd2	Drain Voltage	10 V	2/
Vg1	Gate Voltage Range	-1 to 3 V	
Vg2	Gate Voltage Range	0 to 5 V	
Id1	Drain Current	275 mA	2/
Id2	Drain Current	275 mA	2/
Pin	Input Continuous Wave Power per RF input	25 dBm	2/
Tchannel	Channel Temperature	200 °C	1/

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value	Value 2/
Vd1, Vd2	Bias Supply Voltage	8 V	8 V
Id1 + Id2	Bias Supply Current	380 mA	350 mA
Vg1	Gate 1 Voltage (Pin 26)	1.1 V	0.9 V
Vg2	Gate 2 Voltage (Pin 10)	3.2 V	2.67 V
R1 / R2	External Bias Resistors	6.8k / 10k	open / open

1/ The amplifier is self-biased.

2/ These gate voltages are developed internally using on-chip resistive divider networks.

Table III
RF Characterization Table 1/

T_A=25°C, Vd1, Vd2=8V

Symbol	Parameter	Min	Typ	Max	Units	Note
BW	Bandwidth	40		1000	MHz	
S_{21}	Power Gain	17	20	26	dB	
GF	Gain Flatness		± 0.3		dB	
NF	Noise Figure		1.7		dB	
TZ	Transimpedance		800		Ω	
I_n	Equivalent Input Current Noise		5		pA/rtHz	2/
IP_3	Two-Tone, Third-Order Intercept (450 MHz)		46		dBm	3/
IP_3	Two-Tone, Third-Order Intercept (750 MHz)	39	42		dBm	3/
	Harmonics (2^{nd}, 3^{rd}, 4^{th}) (40 to 500MHz)		-64	-58	dBc	4/
IRL	Input Return Loss		16		dB	
ORL	Output Return Loss		20		dB	
Id1 + Id2	Drain Current		380	500	mA	5/
P_sat	Saturated Output Power (320 MHz)	26	28		dBm	

1/ Using application circuit on pg. 7 including resistors R1 and R2
2/ Measured with open-circuited input
3/ Measured at 16dBm output power per tone
4/ Measured at 15dBm fundamental frequency output power
5/ Increasing drain current will improve linearity of device

Table IV
Power Dissipation and Thermal Properties

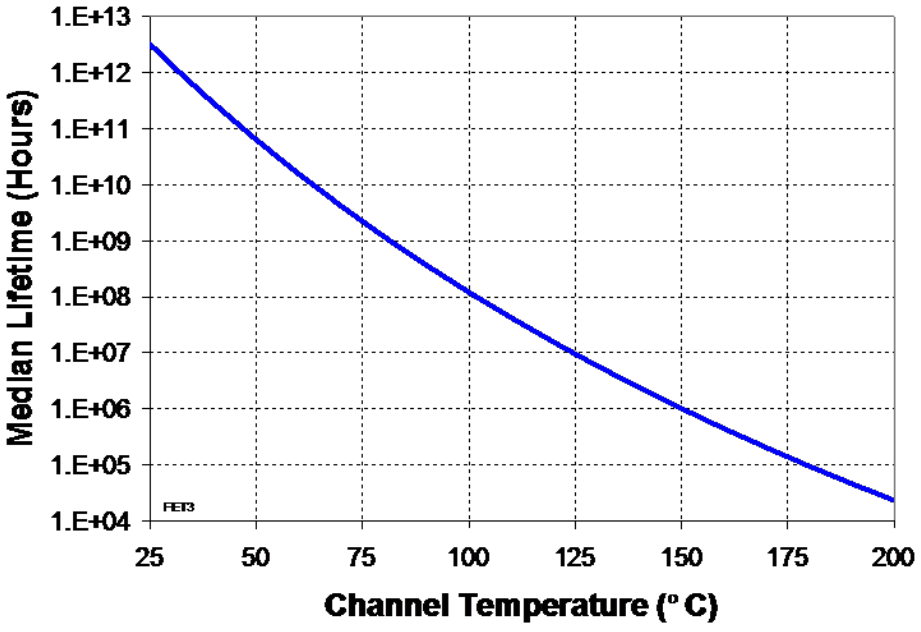
Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 85 °C	Pd = 5.5 W Tchannel = 168 °C Tm = 2.4E+5 Hrs	1/ 2/
Thermal Resistance, θjc	Vd1, Vd2 = 8 V Id1+Id2 = 380 mA Pd = 3.04 W	θjc = 15.1 (°C/W) Tchannel = 131 °C Tm = 5.4E+6 Hrs	
Mounting Temperature	30 Seconds	320 °C	
Storage Temperature		-65 to 150 °C	

1/ For a median life of 1E+6 hours, Power Dissipation is limited to

Pd(max) = (150 °C – Tbase °C)/θjc.

2/ Channel operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.

Median Lifetime (Tm) vs. Channel Temperature



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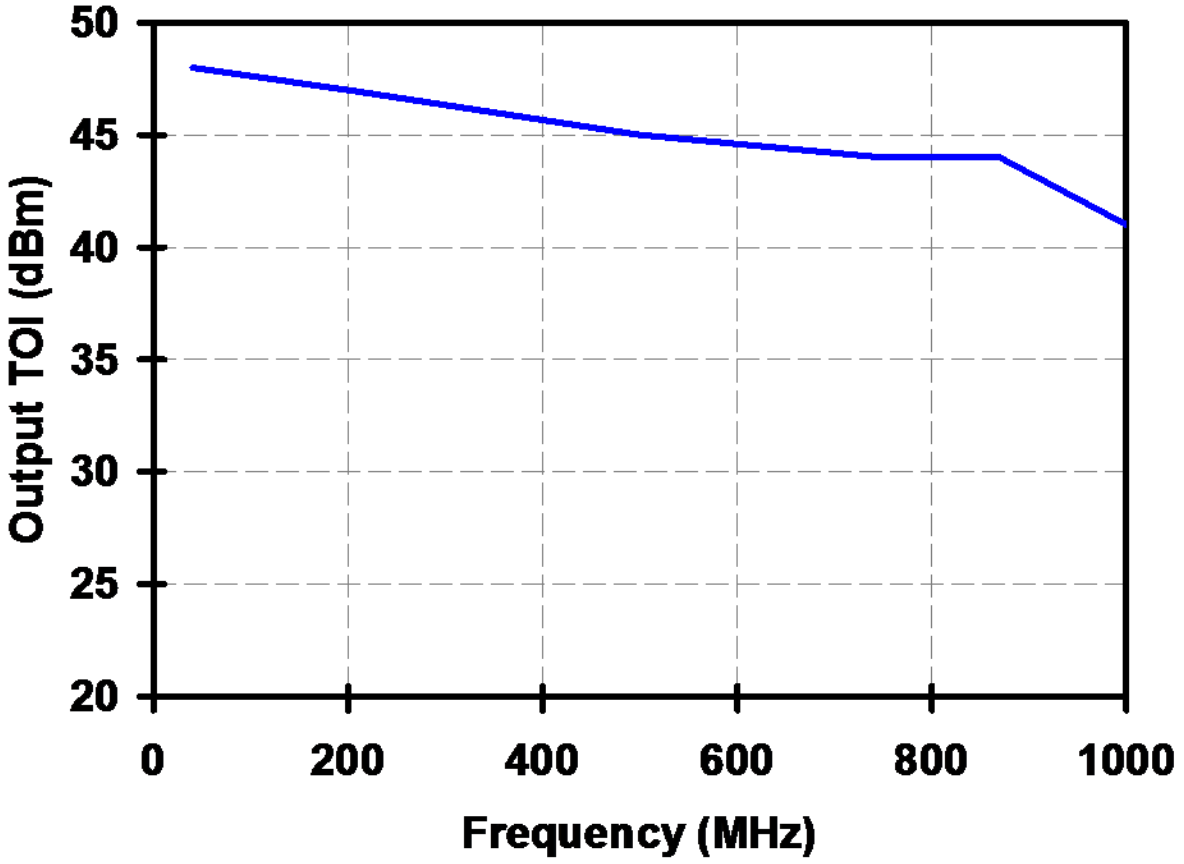
Typical Measured S-Parameters (75 Ω)
Using Application Circuit

Vd1, Vd2 = 8 V, Id1+Id2 = 380mA typ
(includes effects of external baluns)



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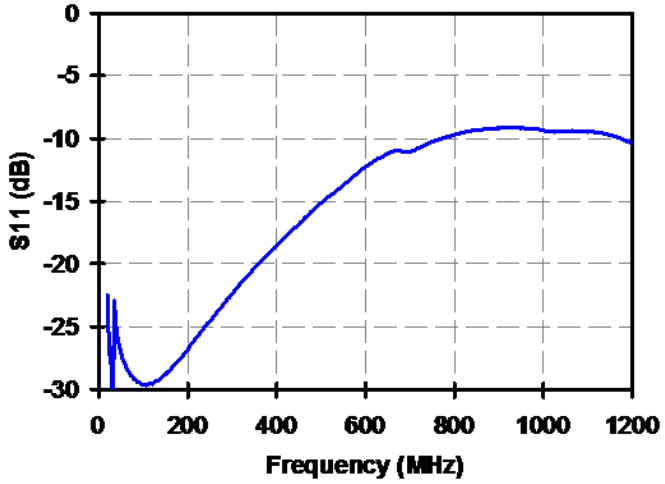

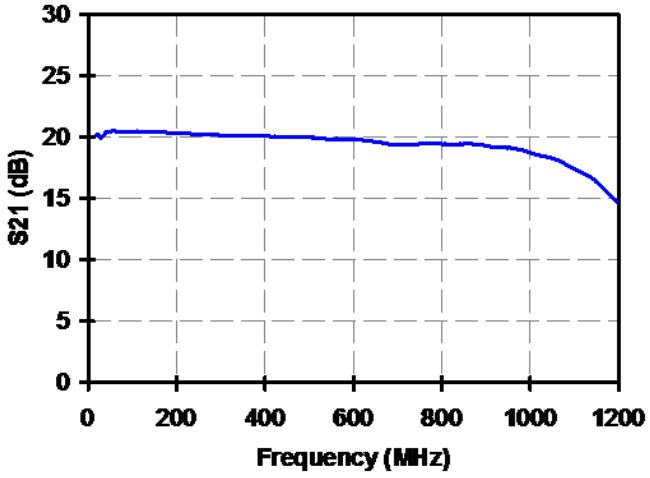

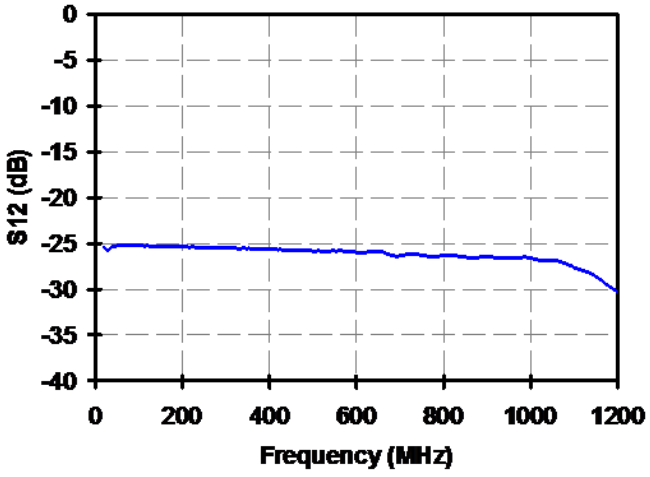

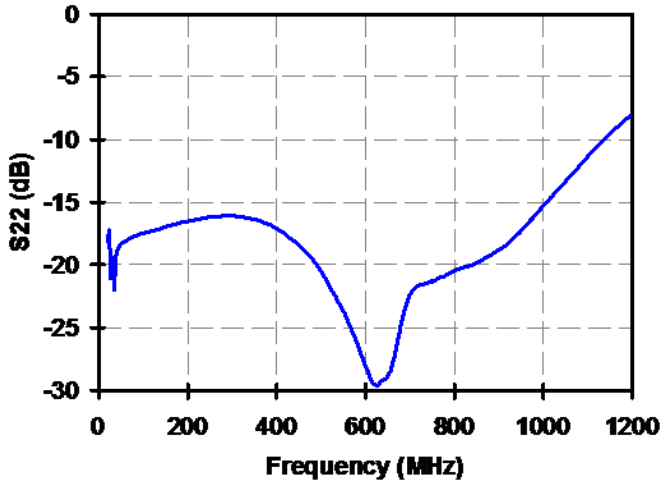

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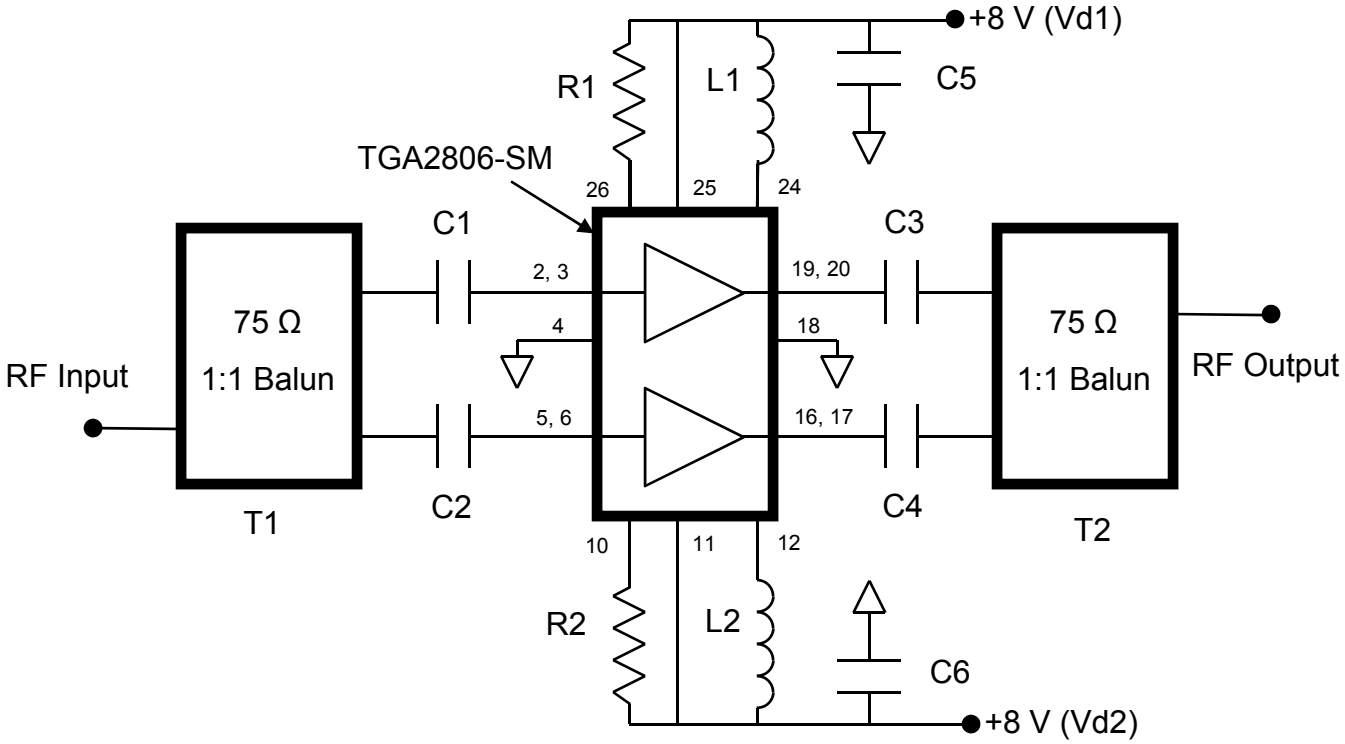
Application Circuit

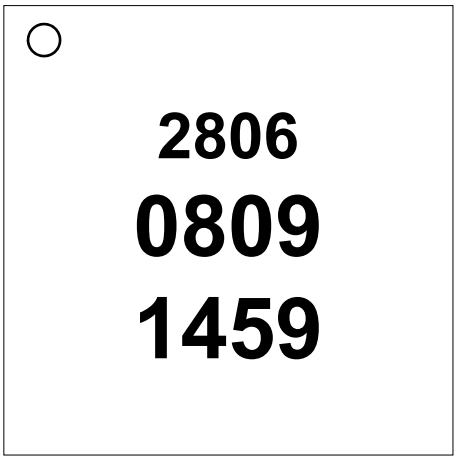


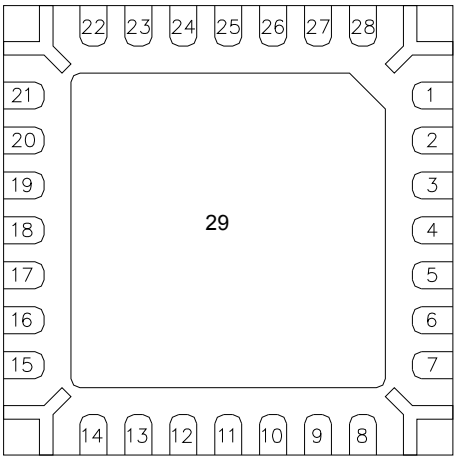
Ref Des	Description
C1, C2	0.01µF
C3, C4	470pF
C5, C6	270pF
L1, L2	820nH
T1, T2	Balun 1/
R1	6.8k 2/
R2	10k 2/

1/ Balun performance impacts amplifier return losses and gain. Best performance can be achieved by winding 34 or 36 gauge bifilar wire around a small binocular core made from low-loss magnetic material. Suitable wire may be obtained from MWS Wire Industries. Core vendors include Ferronics, Fairrite, TDK, and Micrometals.

Alternatively, off-the-shelf baluns can be purchased from a number of vendors including Mini-Circuits (ADTL1-18-75), M/A-COM (ETC1-1-13), and Pulse Engineering (CX2071).

2/ Optional external resistors R1 and R2 increase the Vg1 and Vg2 voltages, respectively as described in Table II. The increased current improves the output TOI by about 1dB.





Pin	Description	Pin	Description
2	RF Input 1	16	RF Output 2
3	RF Input 1	17	RF Output 2
4	GND	18, 29	GND
5	RF Input 2	19	RF Output 1
6	RF Input 2	20	RF Output 1
1, 7, 8,14	NC	15, 21, 22, 23	NC
9	GND	24	Vd1 (choked)
10	Vg2 (Optional)	25	Vd1
11	Vd2	26	Vg1 (Optional)
12	Vd2 (choked)	27	GND
13	Isense	28	NC

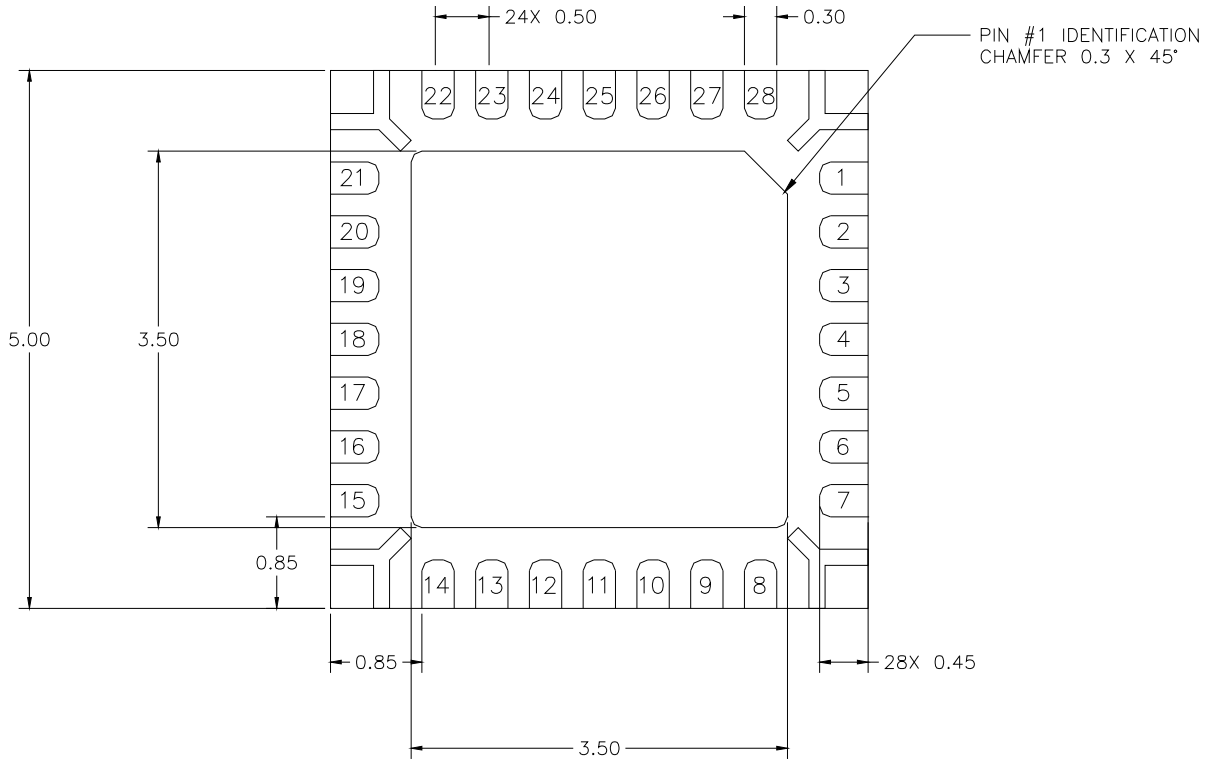
Notes: Pin 13 (Isense) is used to monitor the drain current across a 4 ohm resistor, if desired

The voltage at pin 13 is Vsense = (Id1+Id2) * 4 Volts

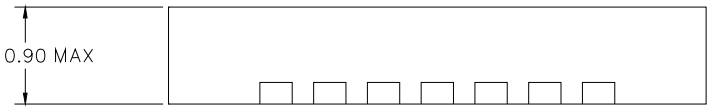
Pins 9 and 27 are internally connected to GND but may be left open

Pins 4 and 18 should be connected to large GND pad (pin 29)

NC pins (1,7,8,14,15,21,22,23,28) are not connected internally; they may be grounded externally, if desired



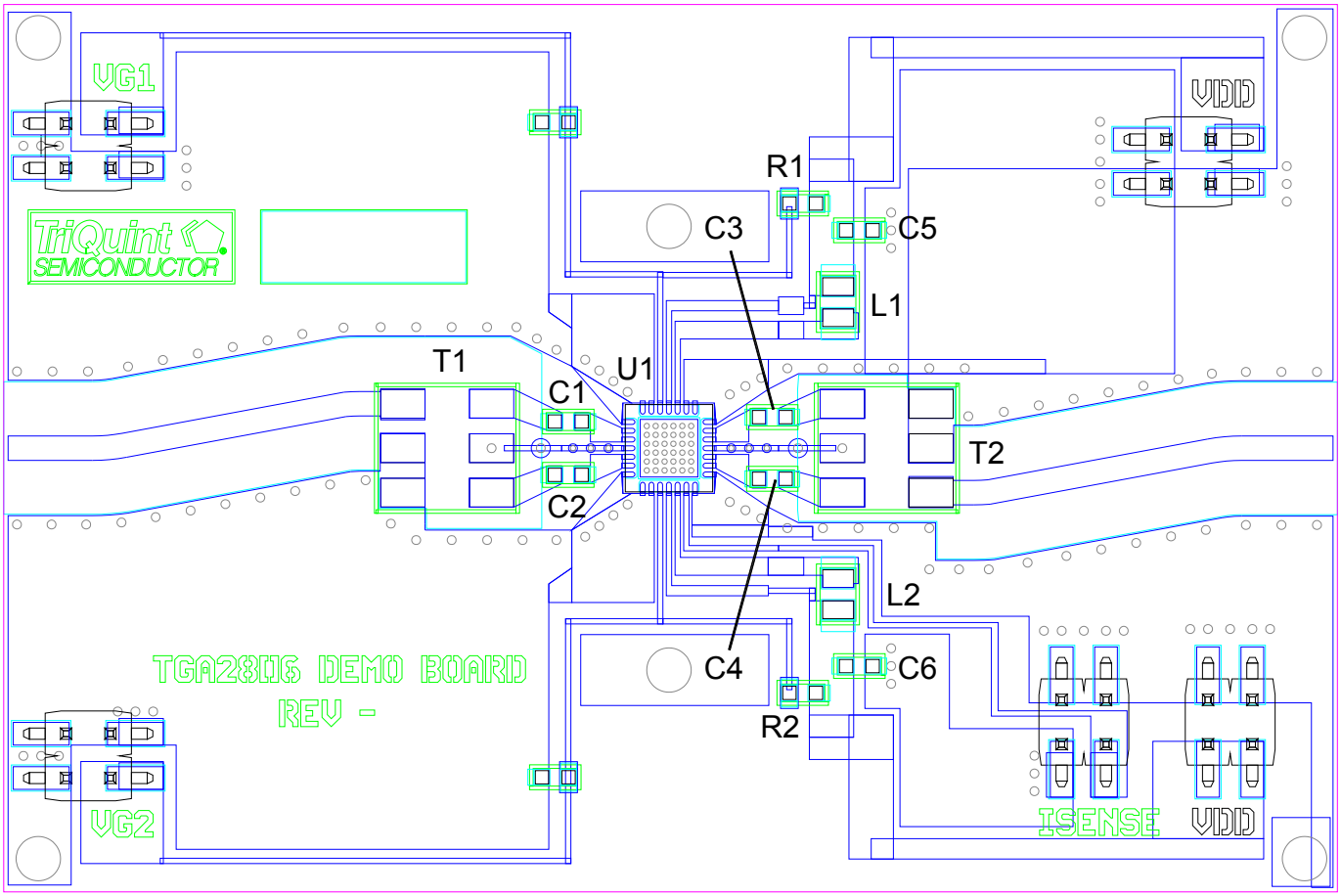
BOTTOM VIEW



SIDE VIEW

Dimensions are in mm

Recommended Assembly Diagram



Board material: 1.57mm thick FR4

Thirty-six (36) open plated vias in center of land pattern

Vias are 12 mil diameter with 20 mil center-to-center spacing

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Assembly Notes

Recommended Surface Mount Package Assembly

- Proper ESD precautions must be followed while handling packages.
- Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.
- TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.
- Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.
- Clean the assembly with alcohol.

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

Ordering Information

Part	Package Style
TGA2806-SM, TAPE AND REEL	5mm x 5mm QFN Surface Mount, TAPE AND REEL

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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