CH7315B HDMI Transmitter

FEATURES

- Supports High-Definition Multimedia Interface (HDMI) version 1.1 and 1.2
- High-speed SDVO* (1G~2Gbps) AC-coupled serial differential inputs
- Supports Intel® High Definition Audio (HD Audio) version 1.0
- Supports S/PDIF sampling rate up to 192 kHz
- Supports switched DVI/HDMI encoding two outputs port A and B one at the time
- Provides High-Bandwidth Digital Content Protection (HDCP) version 1.1 over HDMI
- Support HDMI repeater, a maximum depth of two with maximum number of two leaves (non-repeating receivers)
- Supports HDMI video formats (480i/576i/240p/480p/288p/576p/720p/1080i/1080p) specified in EIA/CEA-861C, DVI and VGA outputs.
- Supports VESA video formats for both the CVT standard and the CEA-861-C standard
- Supports DVI video formats (Up to 1600x1200 graphics resolution, refer to Table 4 for more information)
- Support video pixel rate range from 25M to165M pixels per second
- Support fixed 24MHz clock input for audio data synchronization
- HDMI video low jitter PLL
- HDMI hot plug detection
- Automatically enters power saving mode if TV monitor is turned off or disconnected from the input video source
- Chrontel's advanced "Audio Listening Mode" can automatically intercept digital audio stream from a HD controller to a third party HD audio device
- Configuration through Intel® OpCodes*
- Windows XP and Vista support (including MCE and 64-bit variations)
- Offered in a 64-pin LQFP package

* Intel® Proprietary.

GENERAL DESCRIPTION

The CH7315B HDMI transmitter is mixed-signal video interface chip that transmits uncompressed, copy-protected video and audio data over a secure link from PCs to external television, HDTVs, DVD recorders and A/V receivers using HDMI standard.

The CH7315B also complies with Intel SDVO (Serial Digital Video Output} PC interface specification. The CH7315B HDMI transmitter receives video data through the SDVO bus, and it receive audio data from via an Intel HD (High Definition) Audio bus. CH7315B combines video and audio data, converting it into a single HDMI compliant bit stream for transmission to external CE (consumer electronics) devices. . The CH7315B device contains HDCP cryptographic functions and HDCP keys.

The CH7315B accepts SDVO serial input speeds of 1Gbps to 2Gbps and transmits video output at 25Mpps (pixels per second) to 165Mpps – pixel rates that support all HDTV display modes from 480I to 1080i/1080p.
The CH7315B device accepts RGB signals of 256-level (0-255) or 220-level (16-235) over three pairs of serial differential data ports, then performs the color space conversion and outputs 256-level (0-255) or 220-level (16-235) RGB, 4:2:2 YCbCr or 4:4:4 YcbCr data.

The CH7315B device also supports up to 8-channel audio output at 192 KHz. audio data. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

Auto Power Saving mode is a new feature in the CH7315B that saves PC laptops power by automatically putting the chip into a low power consumption state if a no-need-for-transmission situation is detected.

Audio, video and auxiliary data are transmitted across the three HDMI data channels. The video pixel clock is transmitted on the HDMI clock channel. In order to transmit audio and auxiliary data across the HDMI channels, HDMI uses a packet structure and a special error reduction coding.

The CH7315B features dual output ports with dedicated DDC pins so that two external CE devices can be connected simultaneously and can be selected one at a time via software control. This eliminates the need to manually switch connectors as consumers swap the active receiving device from one connector to another. This feature allows easy implementation of a second HDMI output via the docking station of a notebook PC.

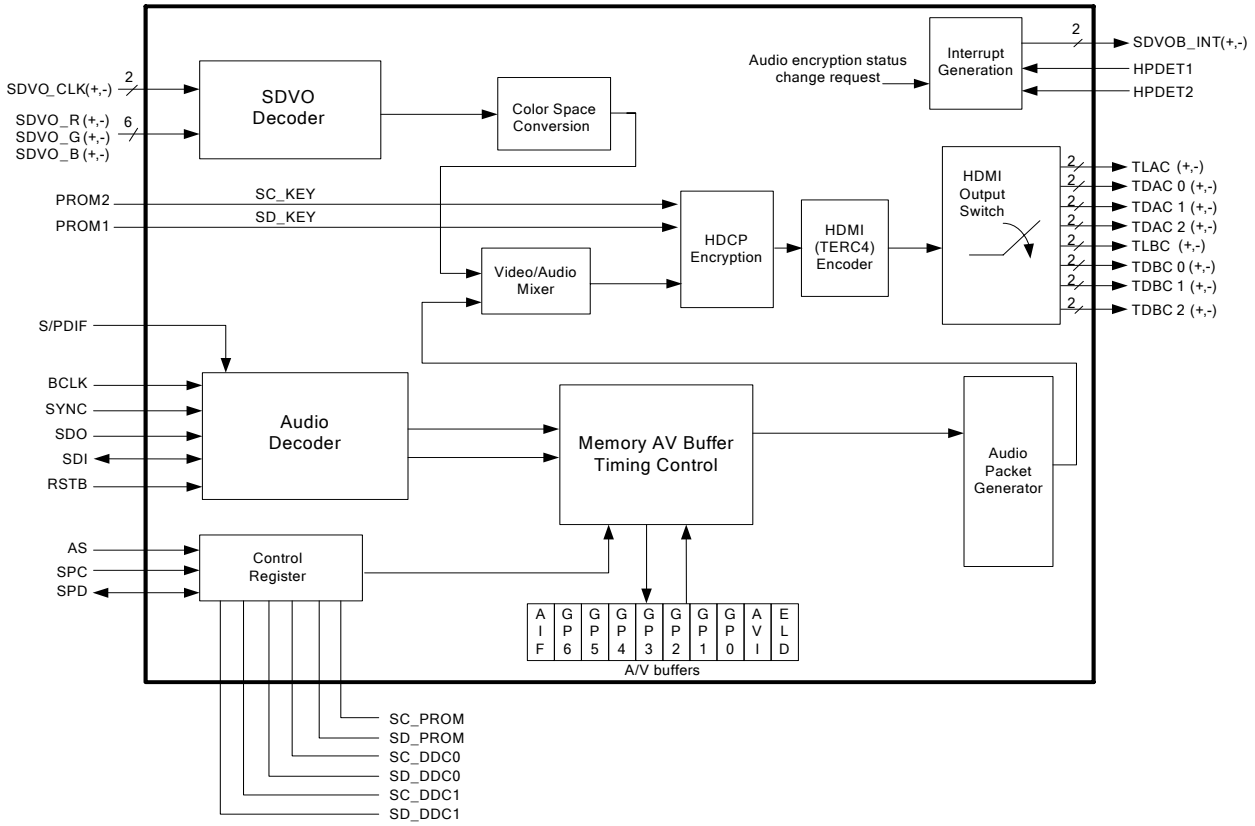

Figure 1: Functional Block Diagram

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1.0 PIN-OUT

1.1 Package Diagram

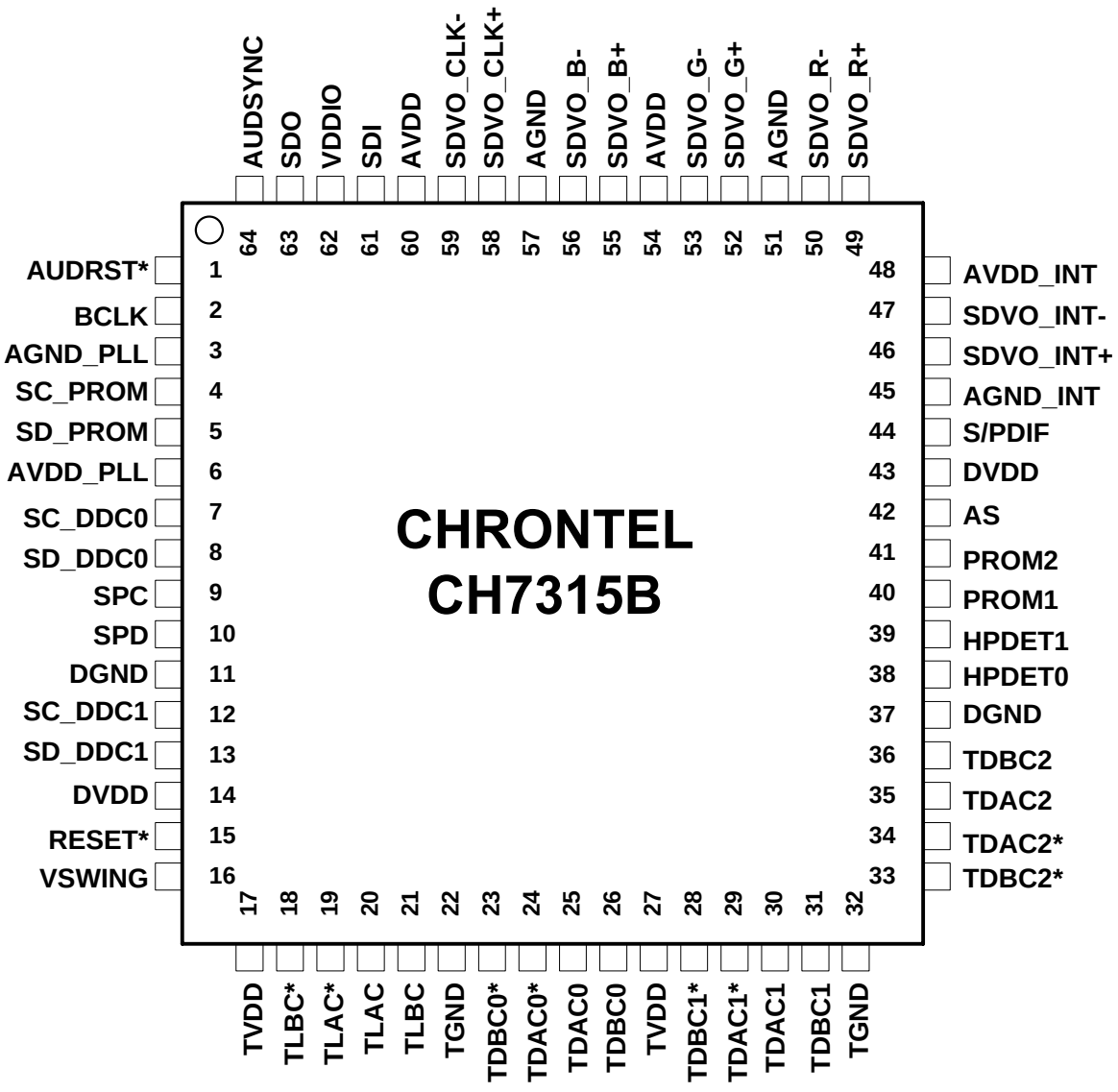

Figure 2: 64-Pin LQFP Pin Out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1	In	AUDRST*	**Audio Reset** This signal sources from HD audio link. When it is low, the device is in default power on reset state.
2	In	BCLK	**Audio Bit Clock** 24.00MHz clock sources from HD audio link.
4	In/Out	SC_PROM	**Routed Clock Output to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
5	In/Out	SD_PROM	**Routed Data to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
7	In/Out	SC_DDC0	**Routed Serial Port Clock to Port A DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open or tied high with a 10kΩ resistor if unused.
8	In/Out	SD_DDC0	**Routed Serial Port Data to Port A DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open or tied high with a 10kΩ resistor if unused.
9	In/Out	SPC	**Serial Port Clock Input / Output** This pin functions as the clock input of the serial port and operates with inputs from 0 to 2.5V. This pin requires an external 2.2kΩ pull up resistor to 2.5V.
10	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 2.5V. Outputs are driven from 0 to 2.5V. This pin requires an external 2.2kΩ pull up resistor to 2.5V.
12	In/Out	SC_DDC1	**Routed Serial Port Clock to Port B DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor of 5.6kΩ to the desired high state voltage. Leave open or tied high with a 10kΩ resistor if unused.
13	In/Out	SD_DDC1	**Routed Serial Port Data to Port B DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor of 5.6kΩ to the desired high state voltage. Leave open or tied high with a 10kΩ resistor if unused.
15	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
16	In	VSWING	**HDMI Swing Control** This pin sets the swing level of the HDMI outputs. A 1.2K-ohm resistor should be connected between this pin and TGND using short and wide traces.
19, 20	Out	TLAC*, TLAC	**HDMI Port A Clock Outputs** These pins provide the differential clock output for the HDMI port A corresponding to data on the TDAC [2:0] outputs.
24, 25	Out	TDAC0*, TDAC0	**HDMI Port A Data Channel 0 Outputs** These pins provide the HDMI port A differential outputs for data channel 0 (blue).
29, 30	Out	TDAC1*, TDAC1	**HDMI Port A Data Channel 1 Outputs** These pins provide the HDMI port A differential outputs for data channel 1 (green).
34, 35	Out	TDAC2*, TDAC2	**HDMI Port A Data Channel 2 Outputs** These pins provide the HDMI port A differential outputs for data channel 2 (red).
18, 21	Out	TLBC*, TLBC	**HDMI Port B Clock Outputs**

Pin #	Type	Symbol	Description
			These pins provide the differential clock output for the HDMI port B corresponding to data on the TDBC [2:0] outputs.
23, 26	Out	TDBC0*, TDBC0	**HDMI Port B Data Channel 0 Outputs** These pins provide the HDMI port B differential outputs for data channel 0 (blue).
28, 31	Out	TDBC1*, TDBC1	**HDMI Port B Data Channel 1 Outputs** These pins provide the HDMI port B differential outputs for data channel 1 (green).
33, 36	Out	TDBC2*, TDBC2	**HDMI Port B Data Channel 2 Outputs** These pins provide the HDMI port B differential outputs for data channel 2 (red).
38	In	HPDET0	**Hot Plug Detect (internal pull-down)** This input pin determines whether the HDMI output driver is connected to a HDMI monitor. When port A is connected, the monitor is required to supply a voltage greater than 2.4 volts.
39	In	HPDET1	**Hot Plug Detect (internal pull-down)** This input pin determines whether the HDMI output driver is connected to a HDMI monitor. When port B is connected, the monitor is required to supply a voltage greater than 2.4 volts.
40	In/Out	PROM1	**Routed Data to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2 card. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open if unused.
41	In/Out	PROM2	**Routed Clock to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a pull-up resistor of 1.8kΩ to the desired high state voltage. Leave open if unused.
42	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (0,1,1,1,0,0,AS*, 0). When AS is tied low (10kΩ), the address is 72h. When AS is tied high (10kΩ), the address is 70h.
44	In	S/PDIF	**S/PDIF Audio Input** This pin accepts digital serial input that complies with IEC60958 for audio bitstreams.
46, 47	Out	SDVO_INT+/-	**Interrupt Output Pair associated with SDVO Data Channel** This pair is used as a hot plug attach/detach notification to VGA controller. Toggling between 100MHz and 200MHz on this pair is considered an assertion (‘1’ value); not toggling at all is considered a de-assertion (‘0’ value).
49, 50, 52,53, 55,56	In	SDVO_R+/-, SDVO_G+/-, SDVO_B+/-	**SDVO Data Channel Inputs** These pins accept 3 AC-coupled (100nF) differential pair of inputs from a digital video port of a graphics controller. These 3 pairs of inputs are R, G, B. The differential peak-peak input voltage has a max value of 1.2V, with a min. value of 175mV.
58,59	In	SDVO_CLK+/-	**Differential Clock Input associated with SDVO Data channel** The range of this clock pair is 100~200MHz. For specified pixel rates in specified modes this clock pair will run at an integer multiple of the pixel rate. The differential peak-peak input voltage has a max value of 1.2V, with a min. value of 175mV.
61	Out	SDI	**Serial Data In for audio side** The device drives SDI and the controller samples SDI with respect to the rising edge of BCLK.
63	In	SDO	**Serial Data Out for audio side** The controller drives data onto SDO and the device samples data present on SDO with respect to every edge of BCLK.
64	In	AUDSYNC	**SYNC signal for audio side** This signal marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). **SYNC** is always sourced from the controller.
14,43	Power	DVDD	**Digital Supply Voltage** (2.5V)
11,37	Power	DGND	**Digital Ground**

Pin #	Type	Symbol	Description
17, 27	Power	TVDD	**HDMI Transmitter Supply Voltage** (3.3V)
22,32	Power	TGND	**HDMI Transmitter Ground**
45	Power	AGND_INT	**Interrupt block Ground**
48	Power	AVDD_INT	**Interrupt block Supply Voltage** (2.5V)
54, 60	Power	AVDD	**Analog Supply Voltage** (2.5V)
51, 57	Power	AGND	**Analog Ground**
3	Power	AGND_PLL	**HDMI PLL Ground**
6	Power	AVDD_PLL	**HDMI PLL Supply Voltage** (3.3V)
62	Power	VDDIO	**HDMI audio interface supply voltage (1.5V/3.3V)**

2.0 FUNCTIONAL DESCRIPTION

2.1 Video Input Interface

2.1.1 Overview

The CH7315B HDMI transmitter receives video data through the SDVO bus. One pair of differential clock signal and three differential pairs of data signals (R/G/B) form one channel data. The input data are 10-bit serialized data. Input data run at 1Gbits/s~2Gbits/s, being a 10x multiple of the clock rate (SDVO_CLK+/-). The CH7315B de-serializes the input into 10-bit parallel data with synchronization and alignment. Then the 10-bit characters are mapped into 8-bit color data or control data (Hsync, Vsync, DE).

2.1.2 Interface Voltage Levels

All differential SDVO pairs are AC coupled differential signals. Therefore, there is not a specified DC signal level for the signals to operate at. The differential peak-peak input voltage has a min of 175mV, and a max of 1.2V. The differential peak-peak output voltage has a min of 0.8V, with a max of 1.2V.

2.1.3 Input Clock and Data Timing

A data character is transmitted least significant bit first. The beginning of a character is noted by the falling edge of the SDVO_CLK+ edge. The skew among input lanes is required to be no larger than 2ns.

The clock rate runs at 100MHz~200MHz. The pixel rate can be 25MP/s~165MP/s. The pixel rate and the clock rate do not always equal. The clock rate can be a multiple of the pixel rate (1x, 2x, or 4x depending on the pixel rate) so that the clock rate will be stay in the 100MHz~200MHz range. In the condition that the clock rate is running at a multiple of the pixel rate, there isn't enough pixel data to fill the data channels. Dummy fill characters ('0001111010') are used to stuff the data stream. The CH7315B supports the following clock rate multipliers and fill patterns shown in Table 2

Table 2: CH7315B supported Pixel Rates, Clock Rates, Data Transfer Rates and Fill Patterns

Pixel Rate	Clock Rate – Multiplier	Stuffing Format	Data Transfer Rate - Multiplier
25~50 MP/s	100~200 MHz – 4xPixel Rate	Data, Fill, Fill, Fill	1.00~2.00Gbits/s – 10xClock Rate
50~100 MP/s	100~200 MHz – 2xPixel Rate	Data, Fill	1.00~2.00Gbits/s – 10xClock Rate
100~200 MP/s	100~200 MHz – 1xPixel Rate	Data	1.00~2.00Gbits/s – 10xClock Rate

2.1.4 Synchronization

Synchronization and channel-to-channel de-skewing is facilitated by the transmission of special characters during the blank period. The CH7315B synchronizes during the initialization period and subsequently uses the blank periods to re-synch to the data stream.

2.2 Audio

The CH7315B can support both HD Audio and S/PDIF audio inputs. It also has the ability to decode a third party HD Audio Codec's digital audio stream from the HD Audio Link

2.2.1 HD Audio General Description

The CH7315B HDMI transmitter receives audio data from via an Intel High Definition Audio with UAA (Universal Audio Architecture) and features a digital output converter and a HDMI pin widget, which is designed for high performance multimedia platform. The CH7315B transmitter supports up to 8 channels, 192kHz and 24 bits per sample, and pack all these audio data into data island package, then send them out through HDMI link.

2.2.2 HD Audio Features

- Supports 32/44.1/48/88.2/96/176.4/192kHz sample rate input
- Supports 16/20/24 bits per sample input
- Supports up to 8 channels
- Supports HDCP for audio and video
- Supports multiple power states control
- Supports up to 7 general-purposed buffer
- Supports AC3 and LPCM

2.2.3 S/PDIF

CH7315B supports 32 kHz, 44.1 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192kHz sampling rates.

2.2.4 Audio Listening Mode

CH7315B can playback an audio stream from a HD audio controller without changing the audio driver.

In addition to supporting the HD Audio and S/PDIF, CH7315B has a capability of automatically detecting, intercepting and transmitting through HDMI a digital audio stream that is sent from a HD Audio Controller to a third party HD Audio decoder device. In other words, the intercepting is done automatically without changing the audio driver in order to have such a simultaneous playback on two devices.

For more implementation, please contact Chrontel Application Support.

2.3 Power Saving

CH7315B offers two power saving features that allow for a significant reduction in the power consumed for the PC system. If a normal system Power-off/Suspend procedure has taken place or GMCH has failed to communicate to TV monitor through DDC lines, the Intel Software Graphic Driver will send an Opcode* Command to CH7315B to enter Power-Down mode. The other smart feature that has been incorporated to the CH7315B is the Auto Power-Saving Mode*. This feature detects the TV monitor connection voltage level and automatically forces CH7315B into a low power state when a significant voltage drop has occurred. For example, if a TV monitor is switched off or is disconnected from the input video source, a voltage drop on DVI/HDMI transmission lines will trigger the CH7315B Auto Power Saving circuitry, and it will automatically shut off most of the device circuitry including the HDMI Output Driver. The CH7315B will resume its normal operation once the TV monitor is plugged back in or switched on.

2.4 HDCP Compatibility

High Bandwidth Digital Content Protect (HDCP) provides a means of protecting the video transmission between a HDMI video transmitter and a HDMI video receiver. Under HDMI, both audio and video data are encrypted or both are decrypted. The CH7315B supports HDCP in its audio and video output data stream. CH7315B process incoming audio encryption status change request along with video transmission. The content protection system includes a process of (a) authentication in which the video transmitter verifies that a given video receiver is licensed to receive protected content; (b) encryption in which the transmitted video data is encrypted based on secret codes exchanged during the authentication process; and (c) renewability in which the video transmitter can identify compromised receivers and prevent the transmission of protected content.

Each HDCP authorized device (transmitter or receiver) has an array of 40, 56-bit secret device keys and a Key Selection Vector (KSV) obtainable from Digital Content Protection LLC (http://www.digital-cp.com/). With the addition of the encrypted HDCP device keys, the CH7315B can be configured to be a HDCP compliant transmitter. A possible connection diagram is shown in the following figure.

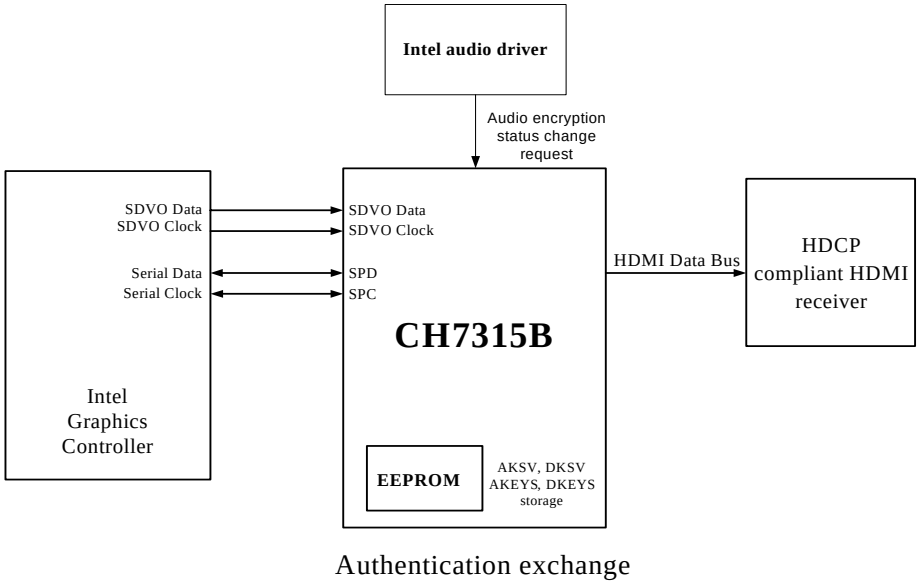

Figure 3: Possible Connection Diagram for HDCP

Details of the CH7315B HDCP operation are available in a separate document. Contact Chrontel for details. See also the "High Bandwidth Digital Content Protection System" specification available at http://www.digital-cp.com/.

2.5 HDMI Transmitter

The CH7315B HDMI link includes three Data channels and a single Clock channel. The Clock channel constantly runs at the pixel rate of the transmitted video. During every cycle of the Clock channel, each of the three data channels transmits a 10-bit character. This 10-bit word is encoded using one of several different coding techniques.

The input stream to CH7315B's encoding logic contains video pixel, packet and control data. The packet data consists of audio and auxiliary data and associated error correction codes.

These data items are processed in a variety of ways and are presented to the HDMI encoder as either 2 bits of control data, 4 bits of packet data or 8 bits of video data per HDMI channel. CH7315B encodes one of these data types or encodes a Guard Band character on any given clock cycle.

CH7315B allows any video format timing to be transmitted and displayed. To maximize interoperability between products, common DTV formats have been defined. Table 4 lists all video formats CH7315B supports (Refer to VESA CVT Standard and EIA/CEA861C for detailed timing information).

Table 3: HDMI video formats CH7315B supports

Video Code	Display Video Format		Pixel Frequency (MHz)
1	640x480p@59.94/60		25.175/25.200
2&3	720x480p@59.94/60		27.000/27.027
4	1280x720p@59.94/60		74.176/74.250
5	1920x1080i@59.94/60		74.176/74.250
6&7	720 (1440) x480i @59.94/60		27.000/27.027
8&9	720 (1440) x 240p@59.94/60	Mode1	27.000/27.027
		Mode2	
10&11	(2880) x 480i @ 59.94/60		54.000/54.054
12&13	(2880) x 240p @	Mode1	54.000/54.054

Video Code	Display Video Format		Pixel Frequency (MHz)
	59.94/60	Mode2	
14&15	1440x480p@59.94/60		54.000/54.054
16	1920x1080p@59.94/60		148.352/148.500
17&18	720x576p@50		27.000
19	1280x720p@50		74.250
20	1920x1080i@50		74.250
21&22	720 (1440) x 576i @50		27.000
23&24	720 (1440) x288p @50	Mode1	27.000
		Mode2	
		Mode3	
25&26	(2880) x 576i @50		54.000
27&28	(2880) x 288p @50	Mode1	54.000
		Mode2	
		Mode3	
29&30	1440x576p@50		54.000
31	1920x1080p@50		148.500
32	1920x1080p@23.97/24		74.176/74.250
33	1920x1080p@25		74.250
34	1920x1080p@29.97/30		74.176/74.250
35,36	2880x480p @ 59.94/60Hz		108.000/108.108
37,38	2880x576p @ 50Hz		108.000
39	1920x1080i (1250 total) @ 50Hz		72.00
40	1920x1080i @ 100Hz		148.500
41	1280x720p @ 100Hz		148.500
42,43	720x576p @ 100Hz		54.000
44,45	720 (1440) x576i @ 100Hz		54.000
46	1920x1080i @ 119.88/120Hz		148.352/148.500
47	1280x720p @ 119.88/120Hz		148.352/148.500
48,49	720x480p @ 119.88/120Hz		54.000/54.054
50,51	720 (1440) x480i @ 119.88/120Hz		54.000/54.054
52,53	720X576p @ 200Hz		108.000
54,55	720 (1440) x 576i @ 200Hz		108.000
56,57	720x480p @ 239.76/240Hz		108.000/108.108
58,59	720 (1440) x480i @ 239.76/240Hz		108.000/108.108

Table 4: DVI Output Formats CH7315B supports

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	Input pixel Frequency (MHz)	DVI Frequency (Mbits/Sec)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<85	<110	<1100
1280x768	15:9	1:1	<85	<119	<1190
1280x1024	4:3	1:1	<85	<158	<1580
1366x768	16:9	1:1	<85	<140	<1400
1360x1024	4:3	1:1	<75	<145	<1450
1400x1050	4:3	1:1	<75	<156	<1560
1600x1200	4:3	1:1	<60	<165	<1650

Table 5: Popular Panel Sizes

UXGA	1600x1200
SXGA+	1400x1050
	1360x1024
SXGA	1280x1024
	1280x960
XGA	1024x768
	1024x600
SVGA	800x600

2.6 Command Interface

Communication is through two-wire path, control clock (SPC) and data (SPD). The CH7315B accepts incoming control clock and data from graphics controller, and is capable of redirecting that stream to PROM, DDC, or CH7315B internal registers. The control bus is able to run up to 1MHz when communicating with internal registers, up to 400KHz for the PROM and up to 100KHz for the DDC.

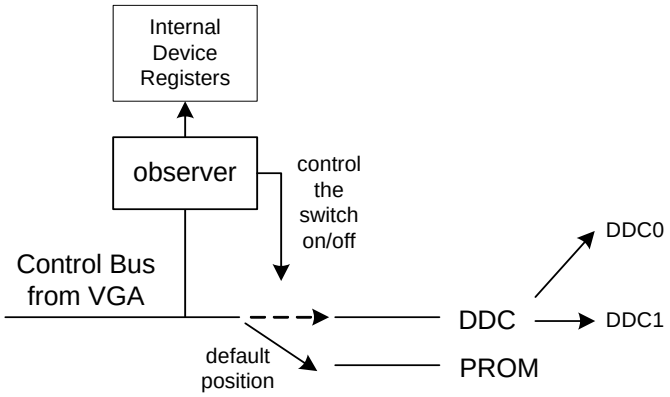

Figure 4: Control Bus Switch

Upon reset, the default state of the directional switch is to redirect the control bus to PROM. At this stage, the CH7315B observes the control bus traffic. If the observing logic sees a control bus transaction destined for the internal registers (device address 70h or 71h based on AS pin external setting), it disables the PROM output pairs, and switches to internal registers. In the condition that traffic is to the internal registers, an OpCode command is used to set the redirection circuitry to the appropriate destination (PROM or DDC). Redirecting the traffic to internal registers while at the stage of traffic to DDC occurs on observing a STOP after a START on the control bus.

3.0 REGISTER CONTROL

The CH7315B is controlled via a serial control port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written into even in all power down modes. The device will retain all register values during power down modes.

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Table 6: T_{SC}, T_{AMB}, T_{STOR}, T_J, T_{VPS} Ratings

Symbol	Description	Min	Typ	Max	Units
	All 2.5V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		3.0 5.0	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-20		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second)			260	°C
	Vapor phase soldering (11 second)			245	
	Vapor phase soldering (60 second)			225	

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can cause permanent damage.

4.2 Recommended Operating Conditions

Table 7: Recommended Operating Conditions

Symbol	Description	Test Condition	Min	Typ	Max
AVDD	Analog Power Supply Voltage	2.375	2.5	2.625	V
AVDD_INT	Analog interrupt Power Supply Voltage	2.375	2.5	2.625	V
AVDD_PLL	Analog PLL Power Supply Voltage	3.100	3.3	3.500	V
DVDD	Digital Power Supply Voltage	2.375	2.5	2.625	V
TVDD	DVI Power Supply	3.100	3.3	3.500	V
VDDIO	Audio interface Power Supply voltage	1.425		3.500	V
VDD33	Generic for all 3.3V supplies	3.100	3.3	3.500	V
VDD25	Generic for all 2.5V supplies	2.375	2.5	2.625	V
	Ambient operating temperature	-20		70	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = -20°C – 70°C, VDD25 =2.5V ± 5%, VDD33=3.3V± 5%)

Table 8: Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
I_{VDD25}	Total VDD25 supply current (2.5V supplies) Pixel Rate=162MHz		210		mA
I_{VDD33}	Total VDD33 supply current (3.3V supply) Pixel Rate=162MHz		75		mA
I_{PD}	Total Power Down Current (all supplies)		100		uA

4.4 DC Specifications

Table 9: DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$V_{RX-DIFFp-p}$	SDVO Receiver Differential Input Peak to Peak Voltage	$V_{RX-DIFFp-p} = 2 * \lvert V_{RX-D+} - V_{RX-D-} \rvert$	0.175		1.200	V
$Z_{RX-DIFF-DC}$	SDVO Receiver DC Differential Input Impedance		80	100	120	Ω
$Z_{RX-COM-DC}$	SDVO Receiver DC Common Mode Input Impedance		40	50	60	Ω
$Z_{RX-COM-INITIAL-DC}$	SDVO Receiver Initial DC Common Mode Input Impedance	Impedance allowed when receiver terminations are first turned on	5	50	60	Ω
$V_{INT-DIFFp-p}$	SDVO INT Differential Output Peak to Peak Voltage		0.8		1.2	V
V_{SPOL} [1]	Serial Port Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH} [2]	Serial Port Input High Voltage		2.0		VDD25 + 0.5	V
V_{SPIL} [2]	Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{HYS} [2]	Serial Port Input Hysteresis		0.25			V
V_{DDCIH}	DDC Serial Port Input High Voltage		4.0		VDD5 + 0.5	
V_{DDCIL}	DDC Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{PROMIH}	PROM Serial Port Input High Voltage		4.0		VDD5 + 0.5	
V_{PROMIL}	PROM Serial Port Input Low Voltage		GND-0.5		0.4	V

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SD_DDCOL}[3]	SPD (serial port data) Output Low Voltage from SD_DDC (or SD_PROM)	Input is V_{INL} at SD_DDC or SD_PROM. 2.2kΩ pullup to 2.5V.			$0.9*V_{INL}$ + 0.25	V
V_{DDCOL}[4]	SC_DDC and SD_DDC Output Low Voltage	Input is V_{INL} at SPC and SPD. 1.8kΩ pullup to 5.0V.			$0.933*V_{INL}$ + 0.35	V
V_{PROMOL}[5]	SC_PROM and SD_PROM Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6kΩ pullup to 2.5V.			$0.933*V_{INL}$ + 0.35	V
$V_{MISC1IH}$[6]	RESET* Input High Voltage		2.7		VDD33 + 0.5	V
$V_{MISC1IL}$[6]	RESET* Input Low Voltage		GND-0.5		0.5	V
$V_{MISC2IH}$[7]	AS Input High Voltage		2.0		VDD25 + 0.5	V
$V_{MISC2IL}$[7]	AS Input Low Voltage	DVDD=2.5V	GND-0.5		0.5	V
$V_{MISC3IH}$	HPDET0, HPDET1, Input High Voltage		1.4		3.72	V
$V_{MISC3IL}$	HPDET0, HPDET1, Input Low Voltage		GND-0.5		0.5	V
$I_{MISC1PU}$	RESET* Pull Up Current	V_{IN} = 0V	10		40	uA
$I_{MISC2PD}$	HPDET0, HPDET1 Pull Down Current	V_{IN} = 2.5V V_{IN} = 2.5V	5 10		20 40	uA uA
$I_{MISC2PU}$	AS Pull Up Current	V_{IN} = 0V	10		40	uA
V_{AUDIL}[8]	Audio Interface input low voltage		GND-0.5		0.35*VDDIO	V
V_{AUDIH}[8]	Audio Interface input high voltage		0.65*VDDIO		VDDIO + 0.5	V
V_{AUDOL}[8]	Audio interface output low voltage	I_{OUT} = 1500 uA	GND-0.5		0.1*VDDIO	V
V_{AUDOH}[8]	Audio interface output high voltage	I_{OUT} = -500 uA	0.9*VDDIO		VDDIO + 0.5	V
V_H	HDMI Single Ended Output High Voltage	TVDD = 3.3V ± 5% R_{TERM} = 50Ω ± 1% R_{SWING} = 1200Ω ± 1%	TVDD – 0.01		TVDD + 0.01	V
V_L	HDMI Single Ended Output Low Voltage		TVDD – 0.6		TVDD – 0.4	V
V_{SWING}	HDMI Single Ended Output Swing Voltage		400		600	mVp-p
V_{OFF}	HDMI Single Ended Standby(off) Output Voltage		TVDD – 0.01		TVDD + 0.01	V
I_{OFF}	HDMI Single Ended Standby(off) Output Current				10	uA

Notes:

1. Refers to SPD. V_{SPOL} is the output low voltage from SPD when transmitting from internal registers not from DDC, EPROM or system.
2. Refers to SPC and SPD.
3. V_{SD_DDCOL} is the output low voltage at the SPD pin when the voltage at SD_DDC or SD_PROM is V_{INL}. Maximum output voltage has been calculated with a worst case pullup of 2.2kΩ to 2.5V on SPD. There are two DDC SPP interface, SC_DDC0/1 and SD_DDC0/1.
4. V_{DDCOL} is the output low voltage at the SC_DDC and SD_DDC pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 1.8k pullup to 5V on SC_DDC and SD_DDC.
5. V_{PROMOL} is the output low voltage at the SC_PROM and SD_PROM pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6kΩ pullup to 2.5V on SC_PROM and SD_PROM.
6. V_{MISC1} refers to RESET* input which is 3.3V compliant.
7. V_{MISC2} refers to AS. AS is 2.5V compliant.
8. V_{AUD} refers to SDI, SDO, AUDSYNC, AUDRST* and BCLK which are 1.5V and 3.3V compliant. Only SDI can be output. VDDIO is the audio interface supply voltage, it can be 1.5V or 3.3V.

4.5 AC Specifications

Table 10: AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
UI_{DATA}	SDVO Receiver Unit Interval for Data Channels		Typ. – 300ppm	1/[Data Transfer Rate]	Typ. + 300ppm	ps
f_{SDVO_CLK}	SDVO CLK Input Frequency		100		200	MHz
f_{PIXEL}	HDMI Transmitter Pixel Rate		25		165	MHz
f_{SYMBOL}	SDVO Receiver Symbol Frequency		1		2	GHz
t_{RX-EYE}	SDVO Receiver Minimum Eye Width		0.4			UI
$t_{RX-EYE-JITTER}$	SDVO Receiver Max. time between jitter median and max. deviation from median				0.3	UI
$V_{RX-CM-Acp}$	SDVO Receiver AC Peak Common Mode Input Voltage				150	mV
$RL_{RX-DIFF}$	Differential Return Loss	50MHz – 1.25GHz	15			dB
RL_{RX-CM}	Common Mode Return Loss	50MHz – 1.25GHz	6			dB
t_{SKEW}	SDVO Receiver Total Lane to Lane Skew of Inputs	Across all lanes			2	ns
T_{HDMIR}	HMDI Output Rise Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
T_{HDMIF}	HDMI Output Fall Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{SKDIFF}	HDMI Output intra-pair skew	f_{XCLK} = 165MHz			90	ps
t_{SKCC}	HDMI Output inter-pair skew	f_{XCLK} = 165MHz			1.2	ns
$T_{HDMIJIT}$	HDMI Output Clock Jitter	f_{XCLK} = 165MHz			150	ps
T_{rf1}	Rise/fall time of Audio output signal SDI with VDDIO=3.3V		1		3	V/ns
T_{rf2}	Rise/fall time of Audio output signal SDI with VDDIO=1.5V		0.5		1.5	V/ns
Freq	Frequency of AC rating waveform as applied to AUDIO input (SDI and SDO) input buffers				24	MHz
I_{oh1}	Current drive ability of AUDIO Output signal SDI (pull up)	Vout=0.9VCC with VDDIO=3.3V	-500			uA
I_{ol1}	Current drive ability of AUDIO Output signal SDI (pull down)	Vout=0.1VCC with VDDIO=3.3V	1500			uA
I_{oh2}	Current drive ability of AUDIO Output signal SDI (pull up)	Vout=0.9VCC with VDDIO=1.5V	-500			uA

Symbol	Description	Test Condition	Min	Typ	Max	Unit
I_{ol2}	Current drive ability of AUDIO Output signal SDI (pulldown)	Vout=0.1VCC with VDDIO=1.5V	1500			uA
T_tco	Time after rising edge of BCLK that output SDI become valid at the Codec		3		11	ns
T_su	Setup for ADUIO Input SDO at both rising and falling edge of BCLK		5			ns
T_h	Hold for SDO at both rising and falling edge of BCLK		5			ns

5.0 PACKAGE DIMENSIONS

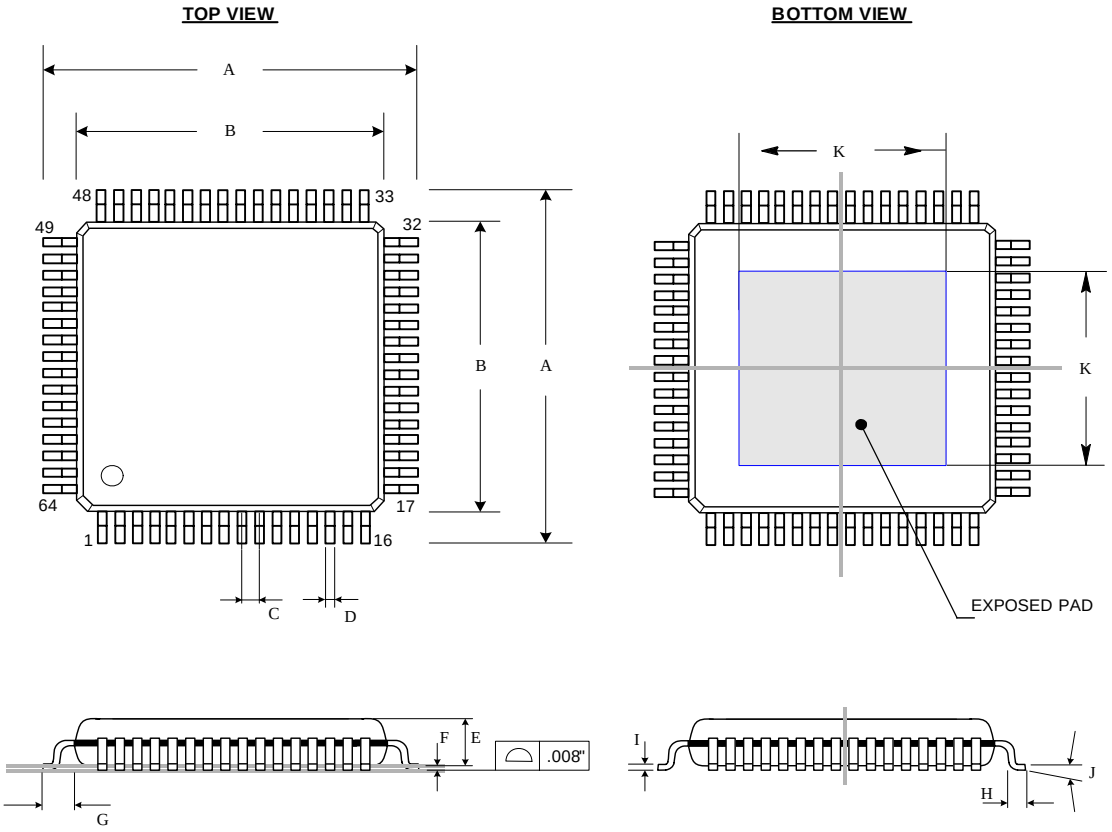

Figure 5: 64 Pin LQFP (Exposed Pad) Package

Table of Dimensions

No. of Leads		SYMBOL										
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°	5.85
	MAX				0.27	1.45	0.15		0.75	0.20	7°	7

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

6.0 REVISION HISTORY

Table 11: Revisions

Rev. #	Date	Section	Description
1.0	3/14/07	All	Initial release
1.1	3/16/07	1.0	General Description update.
1.2	8/2/07	4.4	Change HPDET0, HPDET1 input high voltage spec.
1.3	9/7/07	1.2 & 4.4	Update Pin 9, Pin 10, Pin 12 and Pin 13 in Table 1 and Table 9.
1.4	1/7/08	1.1 & 1.2	Update Pin 44, Figure 1 and Figure 2.
1.5	12/19/2008	4.2, 4.3.	Update operating temperature.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
CH7315B-TEF	Lead Free LQFP with exposed pad	64	2.5V & 3.3V
CH7315B-TEF-TR	Lead Free LQFP with exposed pad in Tape & Reel	64	2.5V & 3.3V

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