CH7317B SDVO◊ / RGB DAC

Features

- Supporting analog RGB outputs for a display monitor
- Supporting maximum pixel rate of 165MP/s or graphics resolutions up to 1920x1200*
- High-speed SDVO◊ (1G~2Gbps) AC-coupled serial differential RGB inputs
- Supporting monitor connection detection
- Programmable power management
- Fully programmable through serial port
- Configuration through Intel® SDVO Opcode ◊
- Offered in 64-pin LQFP package and 64-pin QFN package

* Reduced Blanking
◊ Intel® Proprietary.

General Description

The CH7317B is a Display Controller device interfaces seamlessly to HDTV or PC monitors that is equipped with a VGA RGB interface display connector. Its input port, complied with Intel SDVO Specification 1.2, can accept a digital graphics, high-speed, AC-coupled, serial-differential RGB input signal, and convert it to analog RGB signal for driving the display.

The CH7317B supports maximum pixel rate of 165MP/s and is capable of displaying up to 1920x1200 resolution with reduced blanking. The built-in serial port controller will allow the graphics chipset to obtain the monitor's EDID information or communicate with CH7317B internal registers through SDVO Opcodes. In addition, the transmitter is designed with a monitor connection detection algorithm that allows the graphics chipset to read back the connection status through CH7317B internal registers.

The CH7317B provides the Boundary-scan test to help system developers to check the interconnection between chip I/O and the printed circuit board for faults. When the device is powered down by the graphics chipset, its current consumption is less than 100uA. The CH7317B is available in 64-pin LQFP and 64-pin QFN packages.

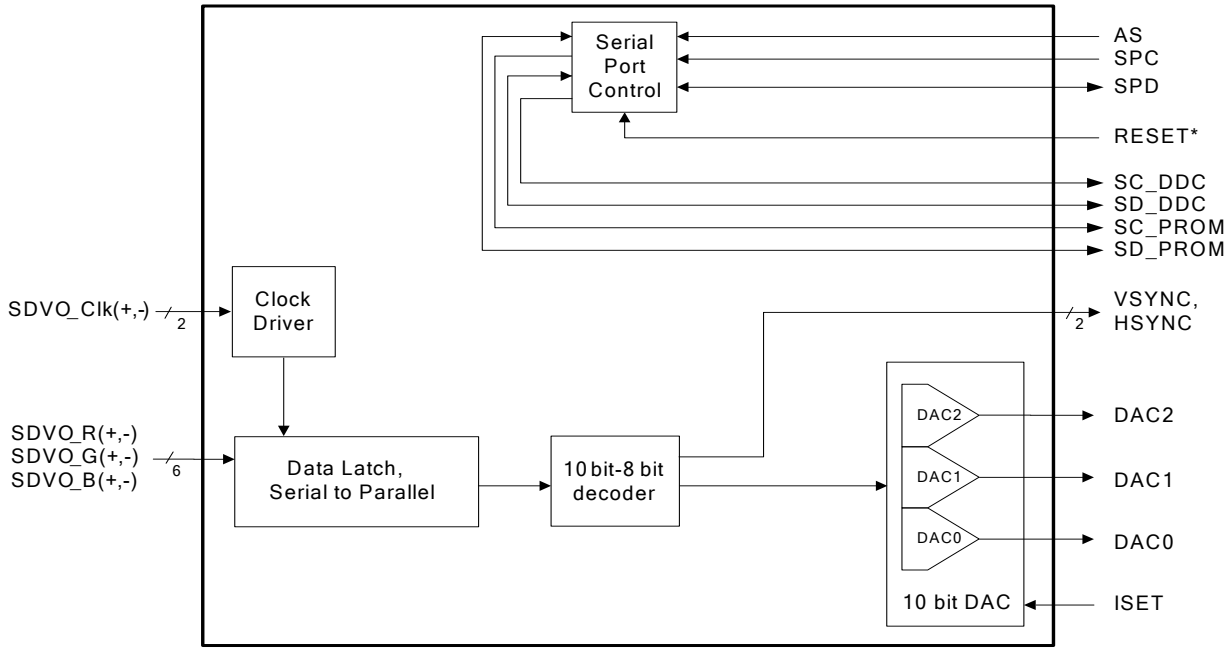

Figure 1: Functional Block Diagram

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1.1 Package Diagram

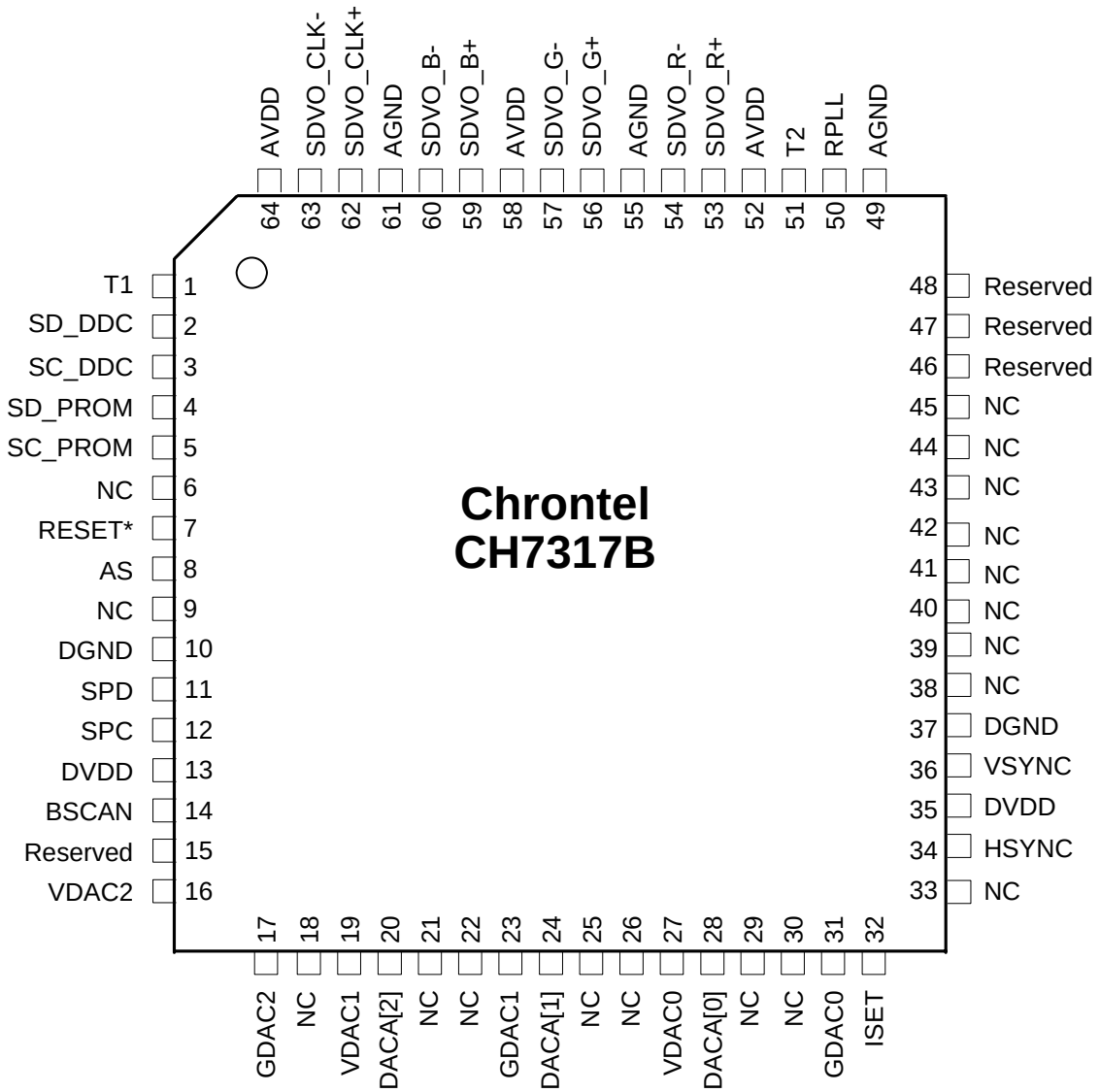


Figure 2: 64-Pin LQFP Package

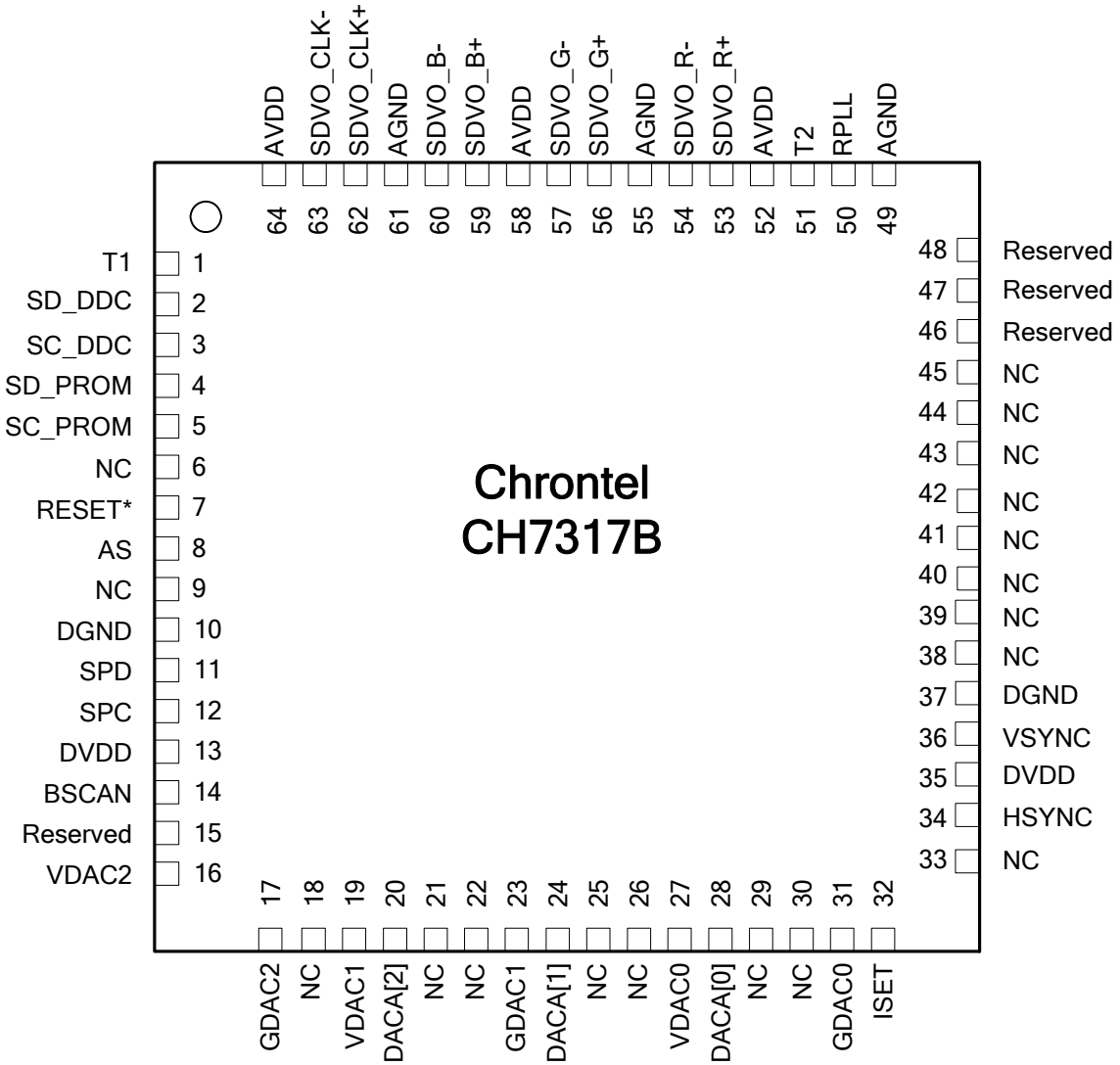


Figure 3: 64-Pin QFN Package

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1,51	Out	T1,T2	**Test** These pins are reserved for factory test and default to high impedance.
2	In/Out	SD_DDC	**Routed Serial Port Data Output to DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a 10KΩ pull-up resistor to the desired high state voltage. Leave open if unused.
3	Out	SC_DDC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a 10KΩ pull-up resistor to the desired high state voltage. Leave open if unused.
4	In/Out	SD_PROM	**Routed Data Output to PROM** This pin functions as the bi-directional data pin of the serial port for PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
5	Out	SC_PROM	**Routed Clock Output to PROM** This pin functions as the clock bus of the serial port to PROM on ADD2 card. This pin will require a pull-up resistor to the desired high state voltage. Leave open if unused.
7	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register. This pin is 3.3V compliant.
8	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (0,1,1,1,0,0,AS*,0). When AS is low the address is 72h, when high the address is 70h.
11	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 2.5V. Outputs are driven from 0 to 2.5V. This pin requires an external 4KΩ - 9KΩ pull up resistor to 2.5V.
12	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and operates with inputs from 0 to 2.5V. This pin requires an external 4KΩ - 9KΩ pull up resistor to 2.5V.
14	In	BSCAN	**BSCAN (Internal pull-down)** This pin should be left open or pulled low with a 10KΩ resistor in the application. This pin enables the boundary scan for in-circuit testing. See section 2.3.1 for details. Voltage level is 0 to DVDD. This pin should be pulled low during normal operation.
15	In	Reserved	**Reserved (Internal pull-down)** This pin should be left open or pulled low with a 10KΩ resistor in the application.
20,24,28	Out	DACA[2:0]	**DAC Output A** Video Digital-to-Analog outputs. RGB Bypass outputs. Each output is capable of driving a 75-ohm doubly terminated load.

Table 1: Pin Description (contd.)

Pin #	Type	Symbol	Description
32	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2Kohm resistor should be connected between this pin and DAC ground (pin 31) using short and wide traces.
34	Out	HSYNC	**Horizontal Sync Output** A buffered version of VGA horizontal sync can be acquired from this pin.
36	Out	VSYNC	**VSYNC** A buffered version of VGA vertical sync can be acquired from this pin.
46	Out	Reserved	This pin should be left open.
47	Out	Reserved	This pin should be left open.
48	Out	Reserved	This pin should be left open.
50	In	RPLL	**PLL Resistor Input** External resistor 10Kohm should be connected between this pin and pin 49.
53,54,56,57 59,60	In	SDVO_R+/-, SDVO_G+/-, SDVO_B+/-	**SDVO Data Channel Inputs** These pins accept 3 AC-coupled differential pair of inputs from a digital video port of a graphics controller. These 3 pair of inputs can be R, G, B or Y, Cr, Cb.
62,63	In	SDVO_CLK+/-	**Differential Clock Input associated with SDVOB Data channel (SDVOB_R+/-, SDVOB_G+/-, SDVOB_B+/-)** The range of this clock pair is 100~200MHz. For specified pixel rates in specified modes this clock pair will run at an integer multiple of the pixel rate. Refer to to section 2.1.3 for details.
13,35	Power	DVDD	**Digital Supply Voltage** (2.5V)
10,37	Power	DGND	**Digital Ground**
16	Power	VDAC2	**DAC Supply Voltage** (3.3V)
17	Power	GDAC2	**DAC Ground**
19	Power	VDAC1	**DAC Supply Voltage** (3.3V)
23	Power	GDAC1	**DAC Ground**
27	Power	VDAC0	**DAC Supply Voltage** (3.3V)
31	Power	GDAC0	**DAC Ground**
52,58,64	Power	AVDD	**Analog Supply Voltage** (2.5V)
49,55,61	Power	AGND	**Analog Ground**

2.0 Functional Description

2.1 Input Interface

2.1.1 Overview

One pair of differential clock signal and three differential pairs of data signals (R/G/B) form one channel data. The input data are 10-bit serialized data. Input data run at 1Gbits/s~2Gbits/s, being a 10x multiple of the clock rate (SDVOB_CLK+/-). The CH7317B de-serializes the input into 10-bit parallel data with synchronization and alignment. Then the 10-bit characters are mapped into 8-bit color data or control data (Hsync, Vsync, DE).

2.1.2 Interface Voltage Levels

All differential SDVO pairs are AC coupled differential signals. Therefore, there is not a specified DC signal level for the signals to operate at. The differential p-p input voltage has a min of 175mV, and a max of 1.2V. The differential p-p output voltage has a min of 0.8V, with a max of 1.2V.

2.1.3 Input Clock and Data Timing

A data character is transmitted least significant bit first. The beginning of a character is noted by the falling edge of the SDVOB_CLK+ edge. The skew among input lanes is required to be no larger than 2ns.

The clock rate runs at 100MHz~200MHz. The pixel rate can be 25MP/s~165MP/s. The pixel rate and the clock rate do not always equal. The clock rate can be a multiple of the pixel rate (1x, 2x, 4x depending on the pixel rate) so that the clock rate will be stay in the 100MHz~200MHz range. In the condition that the clock rate is running at a multiple of the pixel rate, there isn't enough pixel data to fill the data channels. Dummy fill characters ('0001111010') are used to stuff the data stream. The CH7317B supports the following clock rate multipliers and fill patterns shown in Table 2.

Table 2: CH7317B supported Pixel Rates, Clock Rates, Data Transfer Rates and Fill Patterns

Pixel Rate	Clock Rate – Multiplier	Stuffing Format	Data Transfer Rate - Multiplier
25~50 MP/s	100~200 MHz – 4xPixel Rate	Data, Fill, Fill, Fill	1.00~2.00Gbits/s – 10xClock Rate
50~100 MP/s	100~200 MHz – 2xPixel Rate	Data, Fill	1.00~2.00Gbits/s – 10xClock Rate
100~200 MP/s	100~200 MHz – 1xPixel Rate	Data	1.00~2.00Gbits/s – 10xClock Rate

2.1.4 Synchronization

Synchronization and channel-to-channel de-skewing is facilitated by the transmission of special characters during the blank period. The CH7317B synchronizes during the initialization period and subsequently uses the blank periods to re-synch to the data stream.

2.2 VGA Output Operation

The CH7317B can operate in VGA RGB Bypass mode. In VGA RGB Bypass mode, data from the graphics device, after proper decoding, are bypassed directly to the video DACs to implement a second RGB DAC function. Sync signals, after proper decoding, are buffered internally, and can be output to drive the VGA Monitor. The CH7317B can support a pixel rate of 200MHz. This operating mode uses 8-bits of three of the DAC's 10-bit range, and provides a nominal signal swing of 0.661V (or 0.7V depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied in VGA RGB Bypass modes.

Table 3 lists some of the VGA resolutions.

Table 3: Various VGA resolutions.

Name	Resolution
	320x200
	320x240
	400x300
	640x350, 640x400, 640x480
	512x384
	704x480, 704x576
	720x350, 720x400, 720x480, 720x540, 720x576
	768x480, 768x576
SVGA/WSVGA	800x600
	832x624
	848x480
	920x766
	960x600
	1024x600
XGA/WXGA	1024x768
	1124x768
	1152x720
	1280x768, 1280x720, 1280x960
SXGA/WSXGA	1280x1024
	1360x768, 1360x1024
SXGA+/WSXGA+	1400x1050
	1400x1200
	1536x960
UXGA/WUXGA	1600x1200
	1680x1050
	1704x960
	1920x1080
	1920x1200 [1]

Note:
1. With reduced blanking.

Table 4 below lists the DAC output configurations of the CH7317B.

Table 4: Video DAC Configurations for CH7317B

Output Type	DACA[0]	DACA[1]	DACA[2]
VGA RGB	B	G	R

2.3 Command Interface

Communication is through two-wire path, control clock (SPC) and data (SPD). The CH7317B accepts incoming control clock and data from graphics controller, and is capable of redirecting that stream to an ADD2 card PROM, DDC, or CH7317B internal registers. The control bus is able to run up to 1MHz when communicating with internal registers, up to 400kHz for the PROM and up to 100kHz for the DDC.

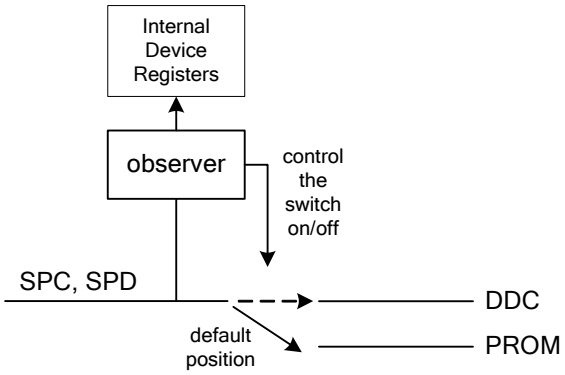


Figure 4: Control Bus Switch

Upon reset, the default state of the directional switch is to redirect the control bus to the ADD2 PROM. At this stage, the CH7317B observes the control bus traffic. If the observing logic sees a control bus transaction destined for the internal registers (device address 70h or 72h), it disables the PROM output pairs, and switches to internal registers. In the condition that traffic is to the internal registers, an Opcode command is used to set the redirection circuitry to the appropriate destination (ADD2 PROM or DDC). Redirecting the traffic to internal registers while at the stage of traffic to DDC occurs on observing a STOP after a START on the control bus.

2.3.1 Boundary scan Test

CH7317B provides a called "NAND TREE Testing" to verify IO cell function at the PC board level. This test will check the interconnection between chip I/O and the printed circuit board for faults (soldering, bend leads, open printed circuit board traces, etc.). NAND tree test is a simple serial logic which turns all IO cell signals to input mode, connects all inputs with NAND gates as shown in the figure below and switches each signal to high or low according to the sequence in Table 11. The test results then pass out at pin 51 (**T2**).

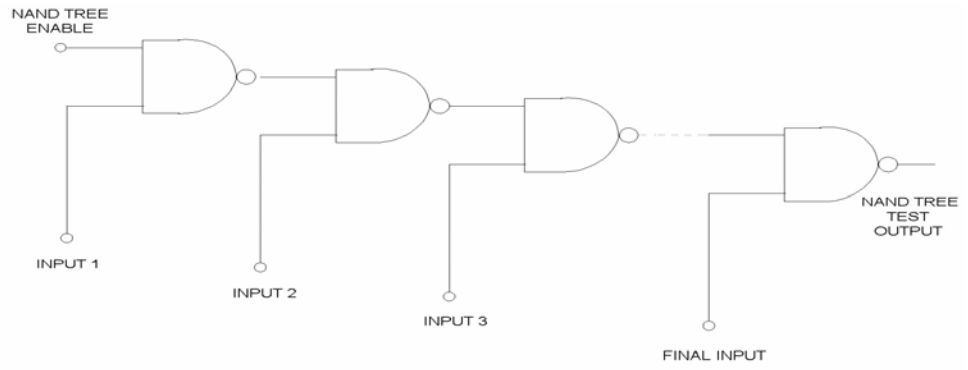


Figure 5: NAND Tree Connection

Set BSCAN =1; (internal weak pull low)
Set all signals listed in to 1.
Set all signals listed in to 0, toggle one by one with certain time period, suggested 100 ns. Pin 51 (**T2**) will change its value each time an input value changed.

Table 5: Signal Order in the NAND Tree Testing

Order	Pin Name	LQFP Pin
1	SD_DDC	2
2	SC_DDC	3
3	SD_PROM	4
4	SC_ PROM	5
5	RESETB	7
6	AS	8
7	SPD	11
8	SPC	12
9	DACA[2]	20
10	DACA[1]	24
11	DACA[0]	28
12	ISET	32
13	HSYNC	34
14	VSYNC	36
15	Reserved	46
16	Reserved	47
17	Reserved	48
18	T2	51

Table 6: Signals not Tested in NAND Test besides power pins

Pin Name	LQFP Pin
SDVO_R+	53
SDVO_R-	54
SDVO_G+	56
SDVO_G-	57
SDVO_B+	59
SDVO_B-	60
SDVO_CLK+	62
SDVO_CLK-	63
RESET*	7
BSCAN	14
Reserved	15
T1	1

3.0 Register Control

The CH7317B is controlled via a serial control port. The serial bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device will retain all register values during power down modes.

Registers 00h to 11h are reserved for Opcode use. All registers except bytes 00h to 11h are reserved for internal factory use. For details regarding Intel® SDVO Opcodes, please contact Intel®.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All 2.5V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		3.0 5.0	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-20		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second) Vapor phase soldering (11 second) Vapor phase soldering (1 minute)			260 245 225	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The temperature requirements of vapor phase soldering apply to all standard and lead free parts.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latch-up.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Analog Power Supply Voltage	2.375	2.5	2.625	V
DVDD	Digital Power Supply Voltage	2.375	2.5	2.625	V
VDAC	DAC Power Supply	3.100	3.3	3.500	V
VDD33	Generic for all 3.3V supplies	3.100	3.3	3.500	V
VDD25	Generic for all 2.5V supplies	2.375	2.5	2.625	V
Rset	Resistor on ISET pin (32)	1188	1200	1212	Ω
R_{RPLL}	Resistor on RPLL pin (50)	9900	10000	10100	Ω
	Ambient operating temperature	-20		70	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = -20°C – 70°C, VDD25 =2.5V ± 5%, VDD33 = 3. 3V ± 5%,)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		17.63		mA
	Video level error			10	%
$I_{VDD25,VGA}$	Total VDD25 supply current (2.5V supplies) with VGA By-Pass output and 1024x768@60Hz input		100	110	mA
$I_{VDD33,VGA}$	Total VDD33 supply current (3.3V supplies) with VGA By-Pass output and 1024x768@60Hz input		75	80	mA
I_{PD}	Total Power Down Current		0.1		mA

4.4 DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Units
$V_{RX-DIFFp-p}$	SDVO Receiver Differential Input Peak to Peak Voltage	$V_{RX-DIFFp-p} = 2 * \lvert V_{RX-D+} - V_{RX-D-} \rvert$	0.175		1.200	V
$Z_{RX-DIFF-DC}$	SDVO Receiver DC Differential Input Impedance		80	100	120	Ω
$Z_{RX-COM-DC}$	SDVO Receiver DC Common Mode Input Impedance		40	50	60	Ω
$Z_{RX-COM-INITIAL-DC}$	SDVO Receiver Initial DC Common Mode Input Impedance	Impedance allowed when receiver terminations are first turned on	5	50	60	Ω
$Z_{RX-COM-High-IMP-DC}$	SDVO Receiver Powered Down DC Common Mode Input Impedance	Impedance allowed when receiver terminations are not powered	20k		200k	Ω
V_{PP_TVCLK}	TVCLK Differential Pk – Pk Output Voltage		0.8		1.2	V
V_{SDOL} [1]	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH} [2]	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD33 + 0.5	V
V_{SPIL} [2]	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Inputs		0.25			V
V_{DDCIH}	DDC Serial Port Input High Voltage		4.0		+5V +0.5	V
V_{DDCIL}	DDC Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{PROMIH}	PROM Serial Port Input High Voltage		4.0		+5V +0.5	V
V_{PROMIL}	PROM Serial Port Input Low Voltage		GND-0.5		0.4	V

Symbol	Description	Test Condition	Min	Typ	Max	Units
V_{SD_DDCOL}[3]	SPD (serial port data) Output Low Voltage from SD_DDC (or SD_EPROM)	Input is V_{INL} at SD_DDC or SD_EPROM. 4.0kΩ pullup to 2.5V.			0.9*V_{INL} + 0.25	V
V_{DDCOL}[4]	SC_DDC and SD_DDC Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6kΩ pullup to 5.0V.			0.933*V_{INL} + 0.35	V
$V_{EPROMOL}$[5]	SC_EPROM and SD_EPROM Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6kΩ pullup to 5.0V.			0.933*V_{INL} + 0.35	V
$V_{MISC1IH}$[6]	RESET* Input High Voltage		2.7		VDD33 + 0.5	V
$V_{MISC1IL}$[6]	RESET* Input Low Voltage		GND-0.5		0.5	V
$V_{MISC2IH}$[7]	AS, BSCAN Input High Voltage		2.0		VDD25 + 0.5	V
$V_{MISC2IL}$[7]	AS, BSCAN Input Low Voltage	DVDD=2.5V	GND-0.5		0.5	V
I_{PU}	AS, RESET* Pull Up Current	V_{IN} = 0V	10		30	uA
I_{PD}	BSCAN Pull Down Current	V_{IN} = 2.5V	10		30	uA
V_{SYNCOH}[8]	HSYNC, VSYNC Output High Voltage	I_{OH} = -0.4mA	2.0			V
V_{SYNCOL}[8]	HSYNC, VSYNC Output Low Voltage	I_{OL} = 3.2mA			0.4	V

Notes:

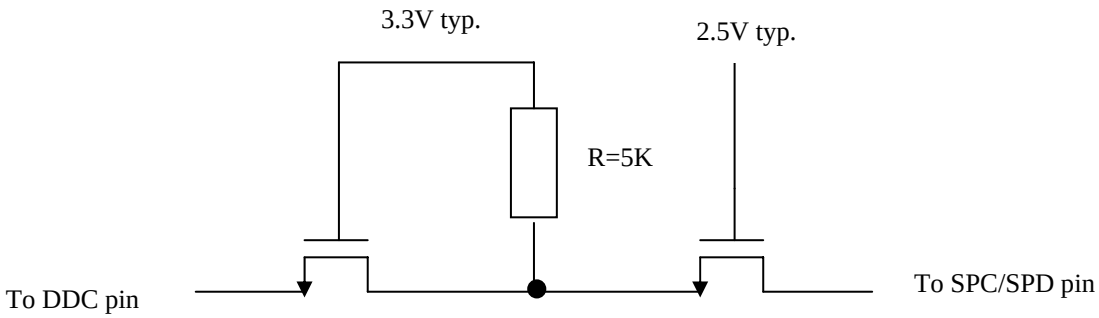
1. V_{SDOL} is the SPD output low voltage when transmitting from internal registers, not from DDC or EEPROM.
2. V_{SPIH} and V_{SPIL} are the serial port (SPC and SPD) input low voltage when transmitting to internal registers. Separate requirements may exist for transmission to the DDC and EEPROM.
3. V_{SD_DDCOL} is the output low voltage at the SPD pin when the voltage at SD_DDC or SD_EPROM is V_{INL}. Maximum output voltage has been calculated with a worst case pullup of 4.0kΩ to 2.5V on SPD.
4. V_{DDCOL} is the output low voltage at the SC_DDC and SD_DDC pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6k pullup to 5V on SC_DDC and SD_DDC.
5. $V_{EPROMOL}$ is the output low voltage at the SC_EPROM and SD_EPROM pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6kΩ pullup to 5V on SC_EPROM and SD_EPROM.
6. V_{MISC1} - refers to RESET* input which is 3.3V compliant.
7. V_{MISC2} - refers to AS, BSCAN, which are 2.5V compliant
8. V_{SYNC} - refers to HSYNC and VSYNC outputs.

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Units
UI_{DATA}	SDVO Receiver Unit Interval for Data Channels		Typ. – 300ppm	1/[Data Transfer Rate]	Typ. + 300ppm	ps
f_{SDVOB_CLK}	SDVO CLK Input Frequency		100		200	MHz
f_{PIXEL}	SDVO Receiver Pixel frequency		25		165	MHz
f_{SYMBOL}	SDVO Receiver Symbol frequency		1		2	GHz
t_{RX-EYE}	SDVO Receiver Minimum Eye Width		0.4			UI
$t_{RX-EYE-JITTER}$	SDVO Receiver Max. time between jitter median and max. deviation from median				0.3	UI
$V_{RX-CM-ACp}$	SDVO Receiver AC Peak Common Mode Input Voltage				150	mV
$RL_{RX-DIFF}$	Differential Return Loss	50MHz – 1.25GHz	15			dB
RL_{RX-CM}	Common Mode Return Loss	50MHz – 1.25GHz	6			dB
T_{SPR}	SPC, SPD Rise Time (20% - 80%)	Standard mode 100k Fast mode 400k 1M running speed			1000 300 150	ns ns ns
T_{SPF}	SPC, SPD Fall Time (20% - 80%)	Standard mode 100k Fast mode 400k 1M running speed			300 300 150	ns ns ns
T_{PROMR}	SC_PROM, SD_PROM Rise Time (20% - 80%)	Fast mode 400K			300	ns
T_{PROMF}	SC_PROM, SD_PROM Rise Time (20% - 80%)	Fast mode 400K			300	ns
T_{DDCR}	SC_DDC, SD_DDC Rise Time (20% - 80%)	Standard mode 100k			1000	ns
T_{DDCF}	SC_DDC, SD_DDC Fall Time (20% - 80%)	Standard mode 100k			300	ns
$T_{DDCR-DELAY}$[1]	SC_DDC, SD_DDC Rise Time Delay (50%)	Standard mode 100k		0		ns
$T_{DDCF-DELAY}$[1]	SC_DDC, SD_DDC Fall Time Delay (50%)	Standard mode 100k		3		ns
t_{SKEW}	SDVO Receiver Total Lane to Lane Skew of Inputs	Across all lanes			2	ns
t_R	HSYNC and VSYNC (when configured as outputs) Output Rise Time (20% - 80%)	15pF load DVDD = 2.5V			1.50	ns

t_F	H and V (when configured as outputs) Output Fall Time (20% - 80%)	15pF load DVDD = 2.5V			1.50	ns

Notes:
1. Refers to the figure below, the delay refers to the time pass through the internal switches.



5.0 Package Dimensions

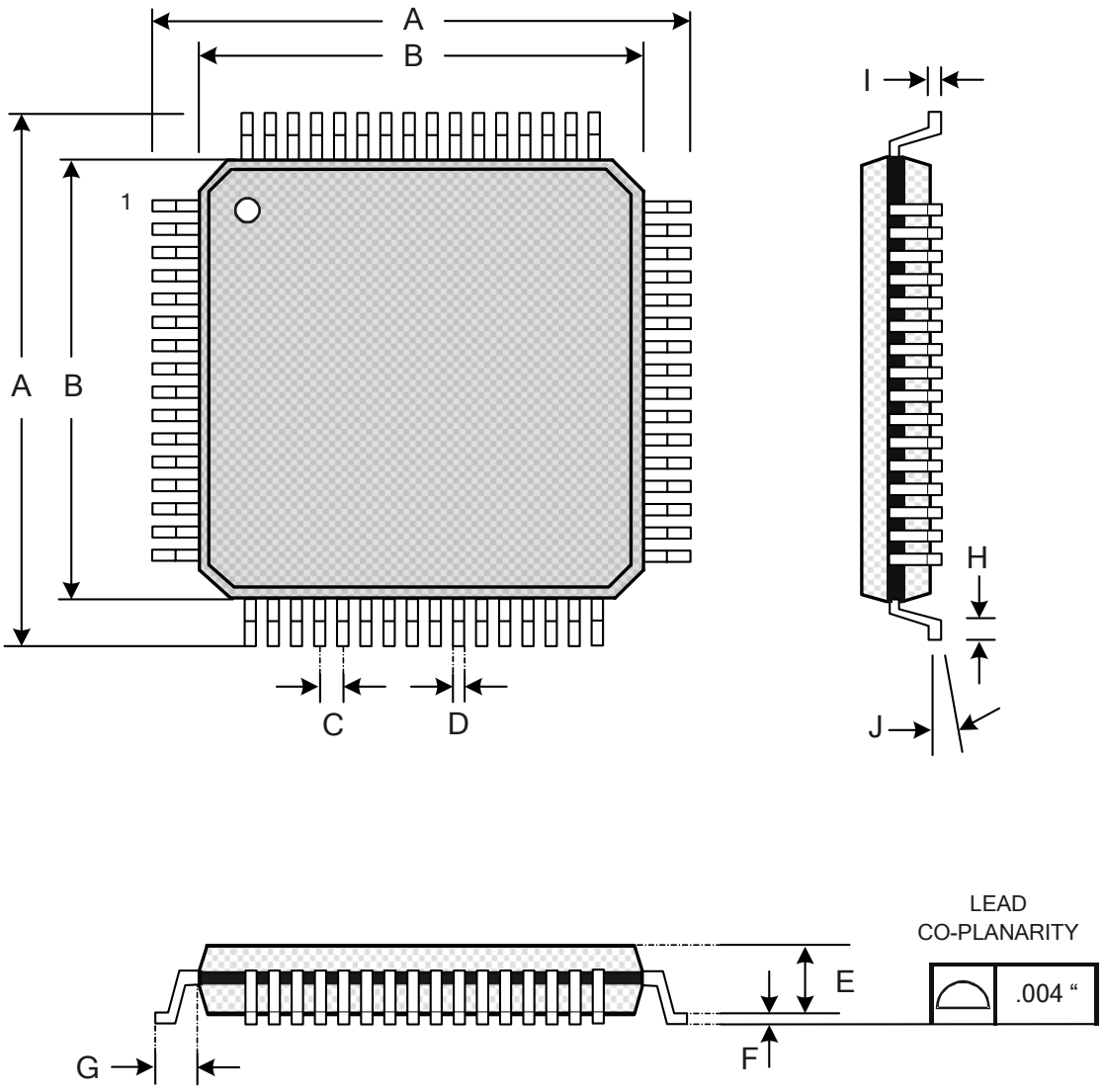


Figure 6: 64 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

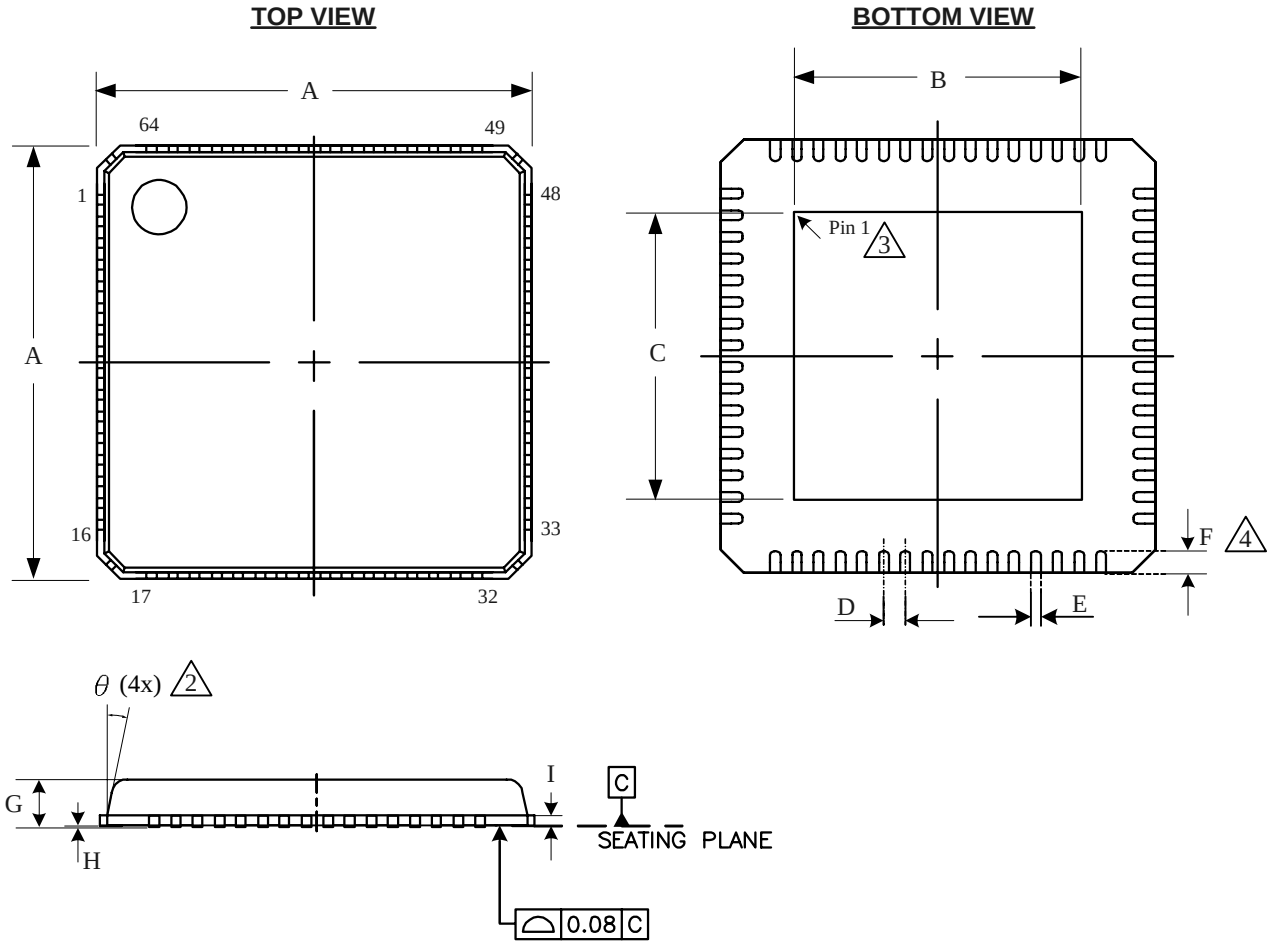


Figure 7: 64 Pin QFN Package (8 X 8 mm)

Table of Dimensions

No. of Leads		SYMBOL								
64 (8 X 8 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	7.9	4.85	4.85	0.4	0.15	0.30	0.7	0	0.2
	MAX	8.1	6.3	6.3		0.25	0.50	1	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

2 Side of body may be square or curved.

3 Exposed pad may have chamfer in area of Pin 1.

4 Pins may protrude from edge of body by 0.05 mm.

6.0 Revision History

Table 7: Revisions

Rev. #	Date	Section	Description
1.0	04/06/09	All	Official release.
1.1	05/06/09	2.2, 2.3 4.2	Update Table 3, Table 4 and Figure 4. Update Ambient operating temperature.
1.2	05/14/09	4.4, 4.5	Add some parameters and notes.
1.3	06/12/09	1.0 1.2 5.0	Update Figure 2 and Figure 3, Pin definition of Pin34. Update Table 1, Pin definition of Pin34. Update Figure 7, QFN package drawing.
1.4	04/04/10	1.2	Update Table 1, the Type of Pin 3 and Pin 5.

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
CH7317B-TF	Lead Free LQFP	64	2.5V & 3.3V
CH7317B-TF-TR	Lead Free LQFP in Tape & Reel	64	2.5V & 3.3V
CH7317B-BF	Lead Free QFN	64	2.5V & 3.3V
CH7317B-BF-TR	Lead Free QFN in Tape & Reel	64	2.5V & 3.3V

Chrontel

2210 O'Toole Avenue, Suite 100,
San Jose, CA 95131-1326
Tel: (408) 383-9328
Fax: (408) 383-9338
www.chrontel.com
E-mail: sales@chrontel.com