Product List

SM8951A/8952AL25, 25MHz 4/8KB internal flash MCU
SM8951A/8952AC25, 25MHz 4/8KB internal flash MCU
SM8951A/8952AC40, 40MHz 4/8KB internal flash MCU

Description

The SM8951A/8952A series product is an 8-bit single chip micro controller with 4/8 KB flash embedded. It provides hard-ware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 4/8 KB flash memory either for program or for data or mixed.
To program the flash block, a commercial programmer is capable to do it.

Ordering Information

yymmv
SM8951A/8952AihhkL

yy: year, ww: month
v: version identifier{ , A, B,…}
i: process identifier {L=3.0V~3.6V,C=4.5V~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}
L:PB Free identifier
{No text is Non-PB Free，”P”is PB Free}

Postfix	Package	Pin / Pad Configuration
P	40L PDIP	Page 2
J	44L PLCC	Page 3
Q	44L QFP	Page 4

Features

- Working Voltage: 3.0V ~ 3.6V For L Version.
  4.5V ~ 5.5V For C Version.
- General 8052 family compatible
- 12 clocks per machine cycle
- 4/8K internal flash memory
- 256 bytes data RAM
- 2/3 16 bit timers/counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Nested interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
  Idle mode and Power down mode
- Code protection function
- One watch dog timer(WDT)
- Low EMI (inhibit ALE)

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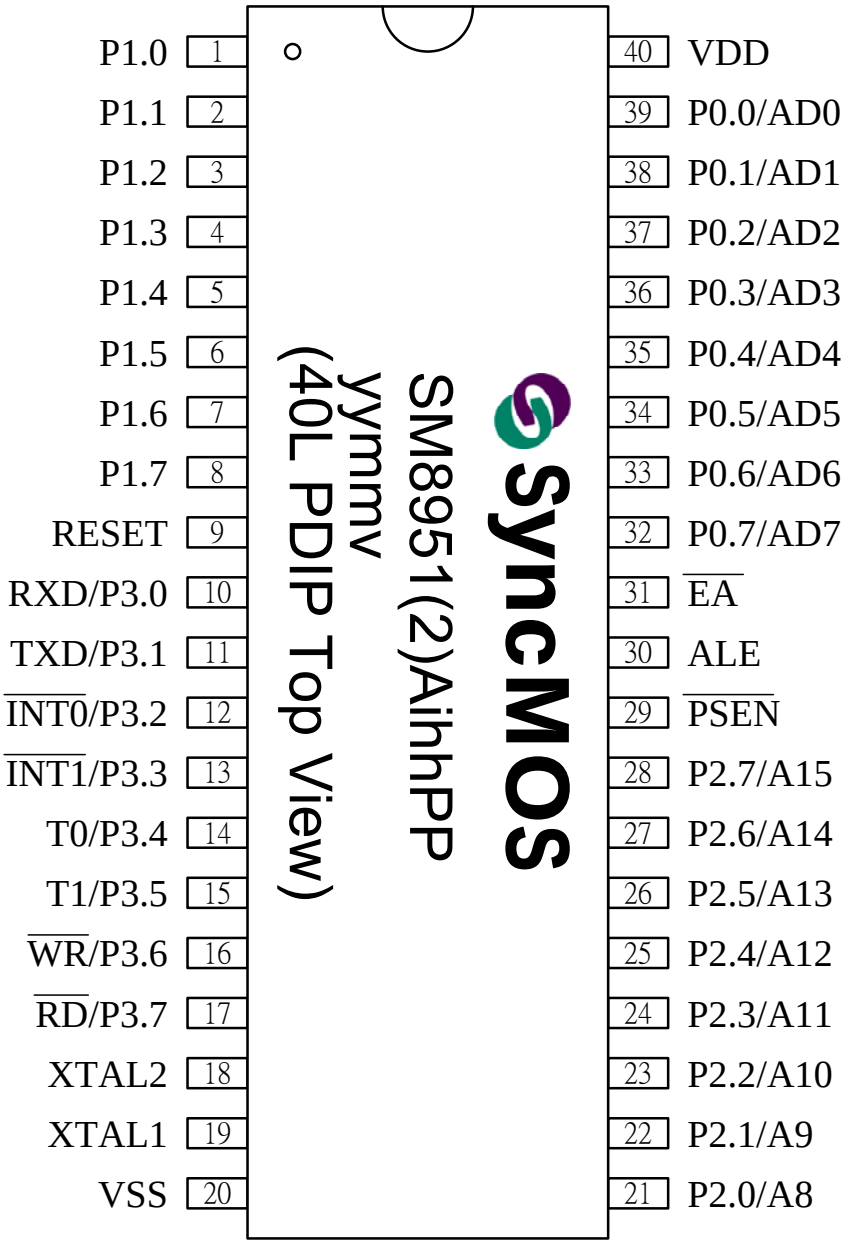
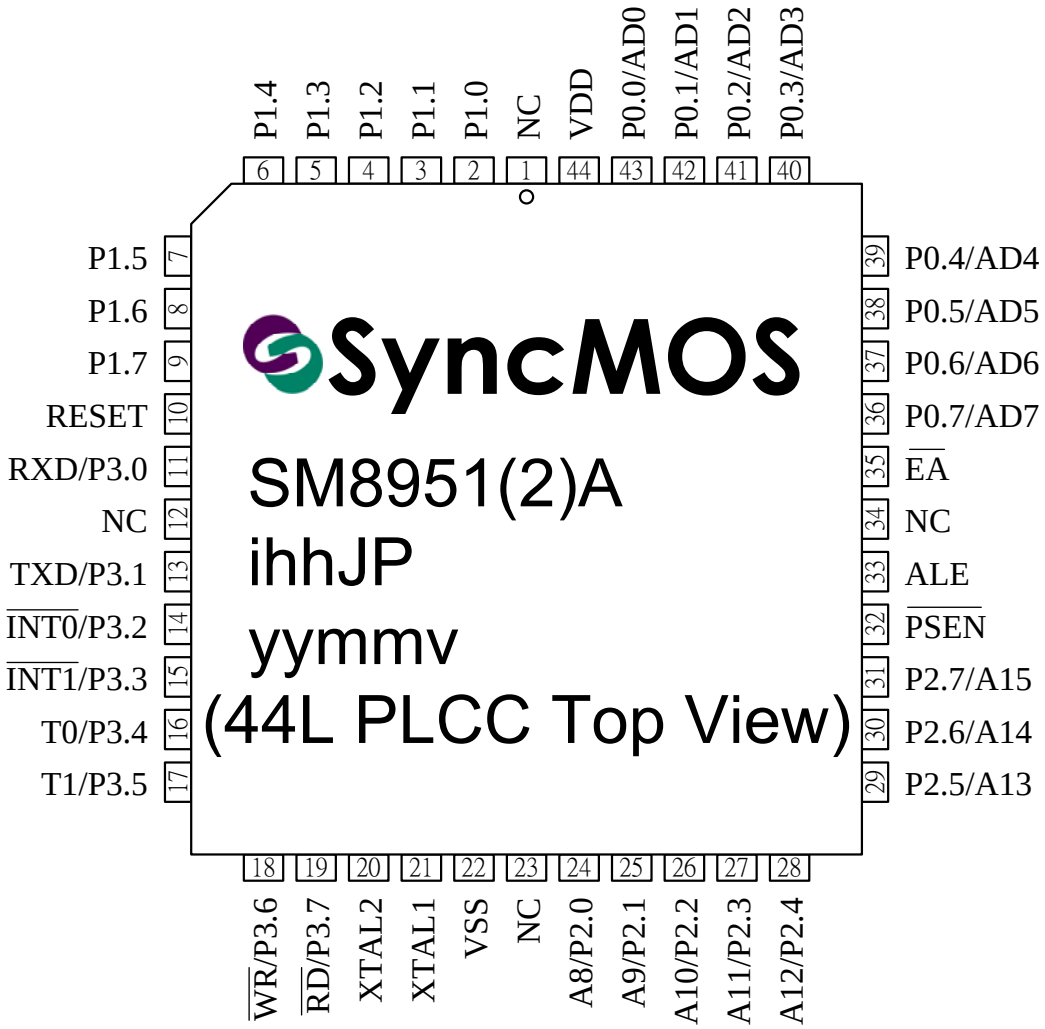
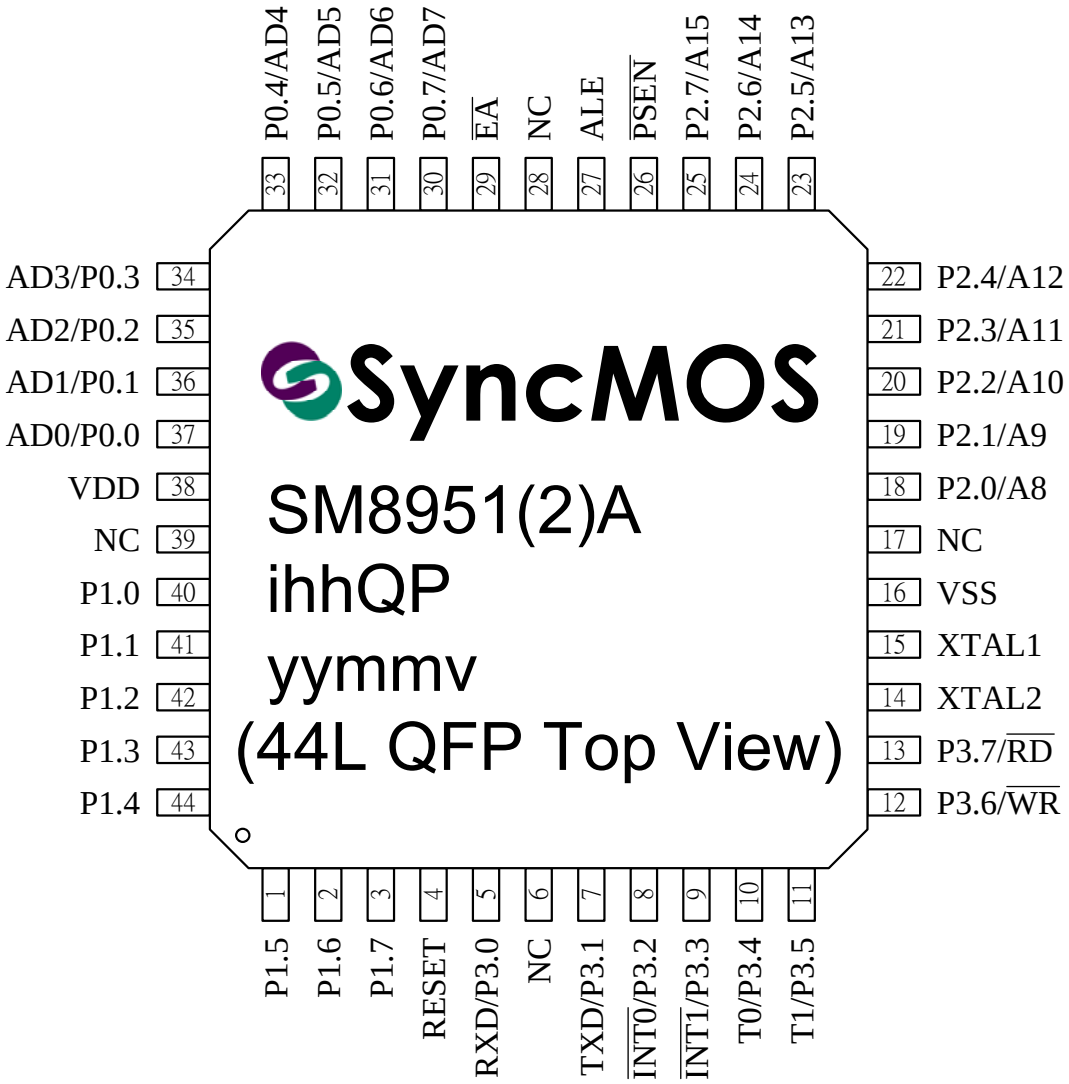
Hsinchu, Taiwan 30078

TEL: 886-3-567-1820
886-3-567-1880
FAX: 886-3-567-1891
886-3-567-1894

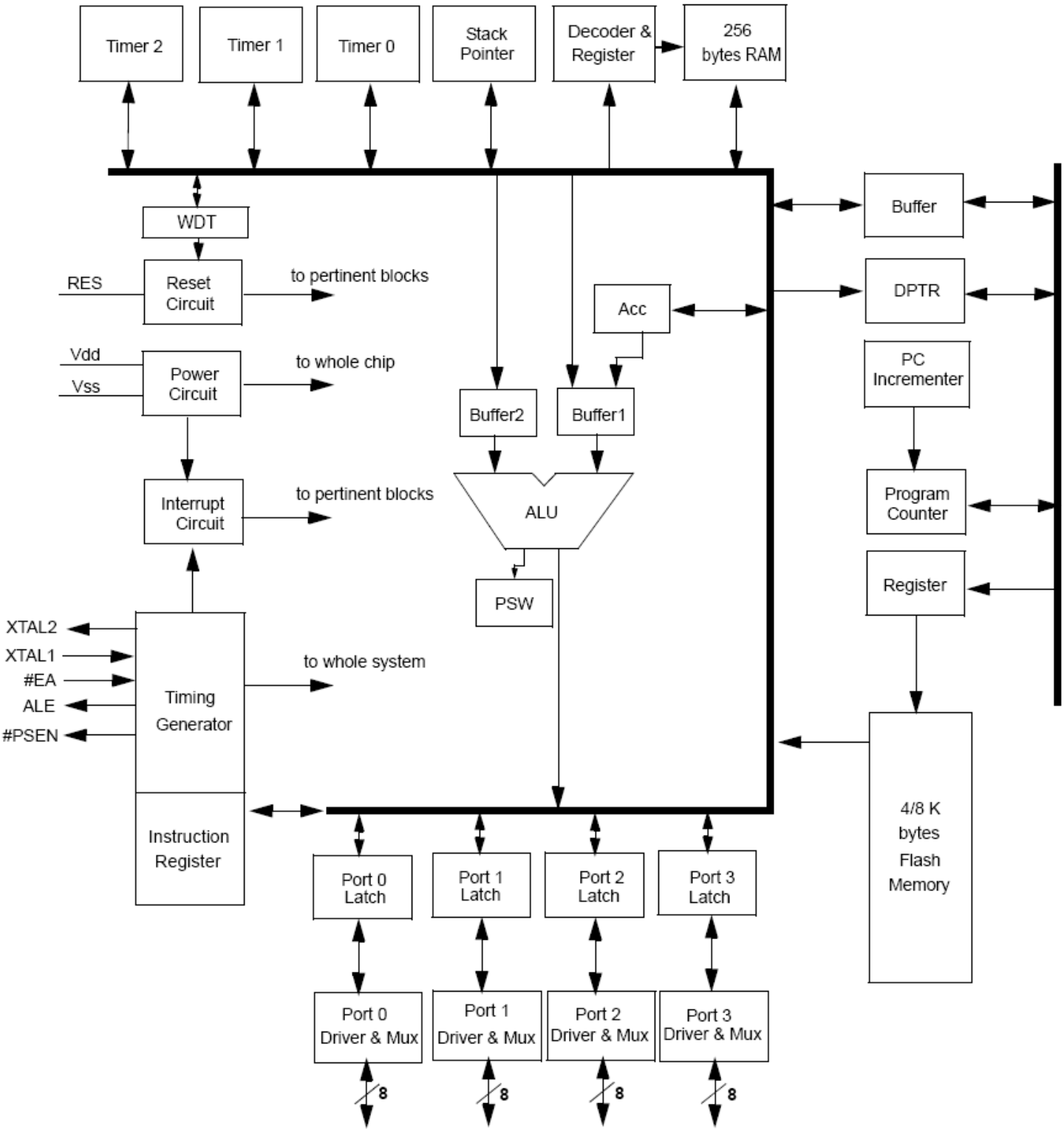
Pin Configuration




P1.4 6
P1.3 5
P1.2 4
P1.1 3
P1.0 2
NC 1
VDD 44
P0.0/AD0 43
P0.1/AD1 42
P0.2/AD2 41
P0.3/AD3 40
P1.5 7
P1.6 8
P1.7 9
RESET 10
RXD/P3.0 11
NC 12
TXD/P3.1 13
INT0/P3.2 14
INT1/P3.3 15
T0/P3.4 16
T1/P3.5 17
P0.4/AD4 39
P0.5/AD5 38
P0.6/AD6 37
P0.7/AD7 36
EA 35
NC 34
ALE 33
PSEN 32
P2.7/A15 31
P2.6/A14 30
P2.5/A13 29
SyncMOS
SM8951(2)A
ihhJP
yymmv
(44L PLCC Top View)
18 WR/P3.6
19 RD/P3.7
20 XTAL2
21 XTAL1
22 VSS
23 NC
24 A8/P2.0
25 A9/P2.1
26 A10/P2.2
27 A11/P2.3
28 A12/P2.4


P0.4/AD4 33
P0.5/AD5 32
P0.6/AD6 31
P0.7/AD7 30
EA 29
NC 28
ALE 27
PSEN 26
P2.7/A15 25
P2.6/A14 24
P2.5/A13 23
AD3/P0.3 34
AD2/P0.2 35
AD1/P0.1 36
AD0/P0.0 37
VDD 38
NC 39
P1.0 40
P1.1 41
P1.2 42
P1.3 43
P1.4 44
SyncMOS
SM8951(2)A
ihhQP
yymmv
(44L QFP Top View)
22 P2.4/A12
21 P2.3/A11
20 P2.2/A10
19 P2.1/A9
18 P2.0/A8
17 NC
16 VSS
15 XTAL1
14 XTAL2
13 P3.7/RD
12 P3.6/WR
1 P1.5
2 P1.6
3 P1.7
4 RESET
5 RXD/P3.0
6 NC
7 TXD/P3.1
8 INT0/P3.2
9 INT1/P3.3
10 T0/P3.4
11 T1/P3.5

Block Diagram



Pin Description

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0		i/o	bit 0 of port 1
2	41	3	P1.1		i/o	bit 1 of port 1
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5		i/o	bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receiver data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/-	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/-	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR	L/-	i/o	bit 6 of port 3 & external memory write
17	13	19	P3.7/#RD	L/-	i/o	bit 7 of port 3 & external memory Read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of external memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of external memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of external memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of external memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of external memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of external memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of external memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of external memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of external memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of external memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of external memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of external memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of external memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of external memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of external memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of external memory
40	38	44	VDD			Drive Voltage, +5 Vcc

SFR Memory Map

$F8									$FF
$F0	B								$F7
$E8									$EF
$E0	ACC								$E7
$D8									$DF
$D0	PSW								$D7
$C8	T2CON		RC2L	RC2H	TL2	TH2			$CF
$C0									$C7
$B8	IP							**SCONF**	$BF
$B0	P3								$B7
$A8	IE								$AF
$A0	P2								$A7
$98	SCON	SBUF						**WDTC**	$9F
$90	P1								$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH				PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM8951A/8952A

Extension Function Description

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The SM8951/8952 WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) OF Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM8958A been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

Watch Dog Timer Registers - WDT Control Register (WDTC, $9F)

	WDTE	R	Clear	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

MSB LSB

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
If CLEAR bit set to 1 , Watch Dog Timer will be reset . User don't reset value to 0 .

PS2~PS0:clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF, $BFH)

bit-7 bit-0

	WDR	Unused	Unused	Unused	Unused	Unused	Unused	ALEI
Read / Write:	R/W	-	-	-	-	-	-	R/W
Reset value:	0	*	*	*	*	*	*	0

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1
ALEI : ALE output inhibit bit, to reduce EMI
The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

Reduce EMI Function

The SM8951A/8952A allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external pro gram memory or no external data RAM in the system.

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	For C Version
VCC3	Supply voltage	3	3.3	3.6	V	For L Version
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V, 3.3V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 3.0V to 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,#EA	-0.5	0.8	V	
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=8mA (5V) / IOL=6mA (3.3V)
VOL2	Output Low Voltage	port 1,2,3		0.45	V	IOL=6.5mA (5V) / IOL=5mA (3.3V)
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA (only for VCC =5V)
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,ALE,#PSEN	2.4		V	IOH=-60uA (only for VCC =5 V)
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 ℃
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1:Under steady state (non-transient) conditions, IOL must be externally
Limited as follows : Maximum IOL per port pin : 10mA
Maximum IOL per 8-bit port : port 0 :26mA
port 1,2,3 :15mA
Maximum total IOL for all output pins : 71mA
If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

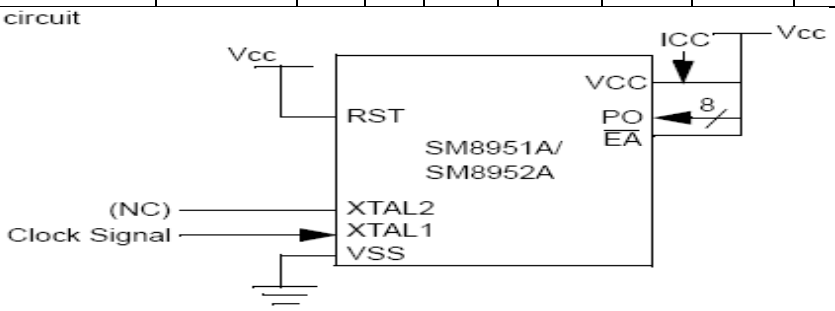
Note2 : Minimum VCC for Power-down is 2V.

AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

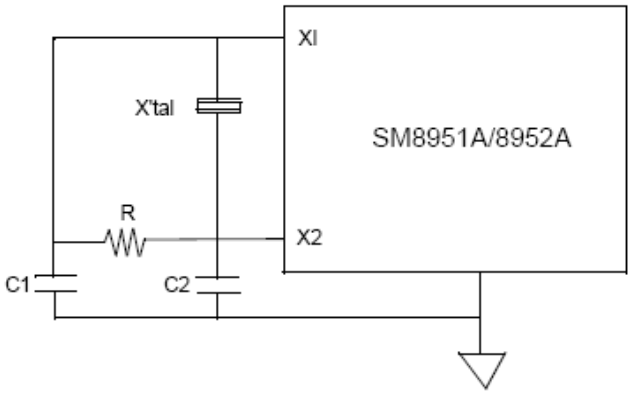
Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT-10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T+25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT-20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT-10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT+20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT-10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT-20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT+10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T+10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

ICC Active mode test circuit



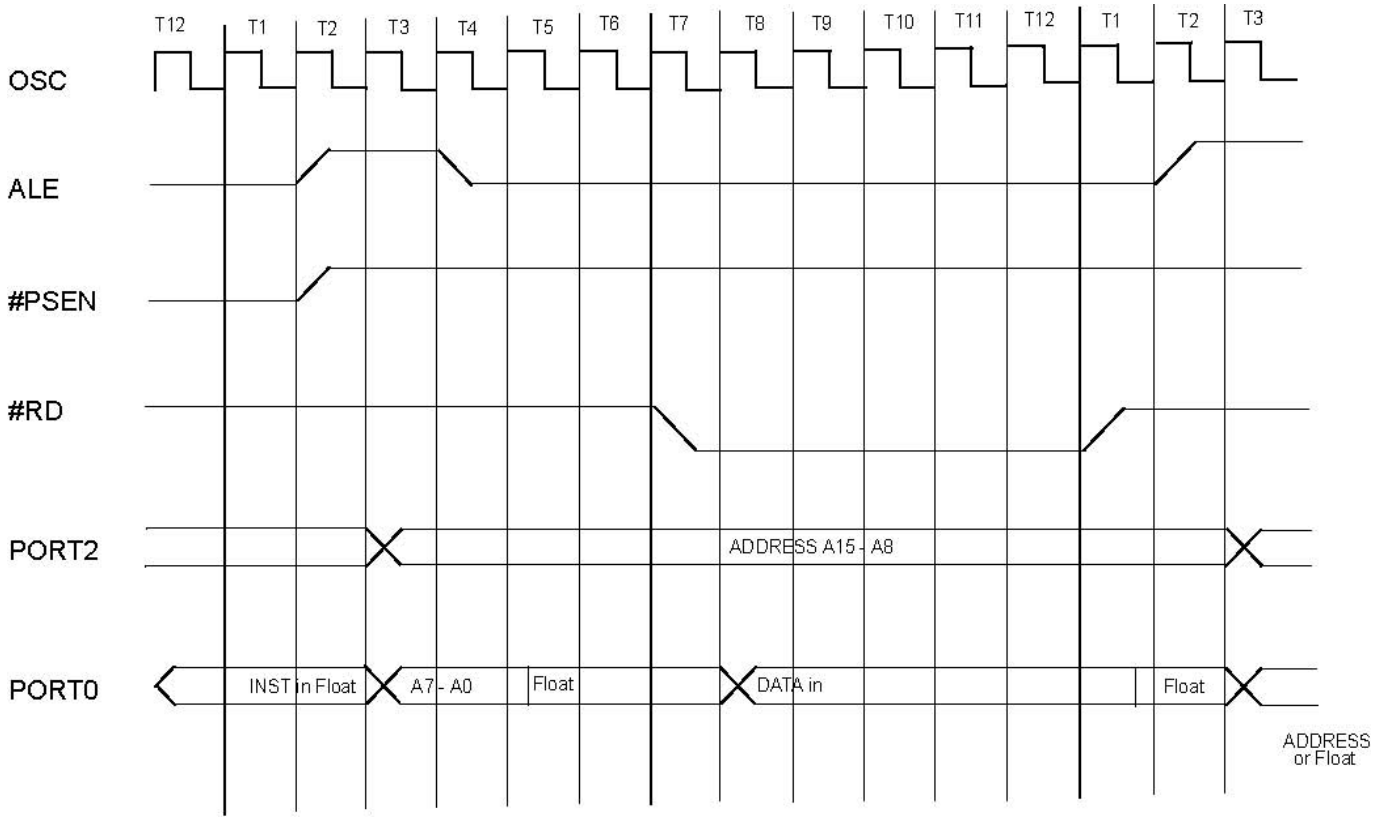
Application Reference

Valid for SM8958A				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	Open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

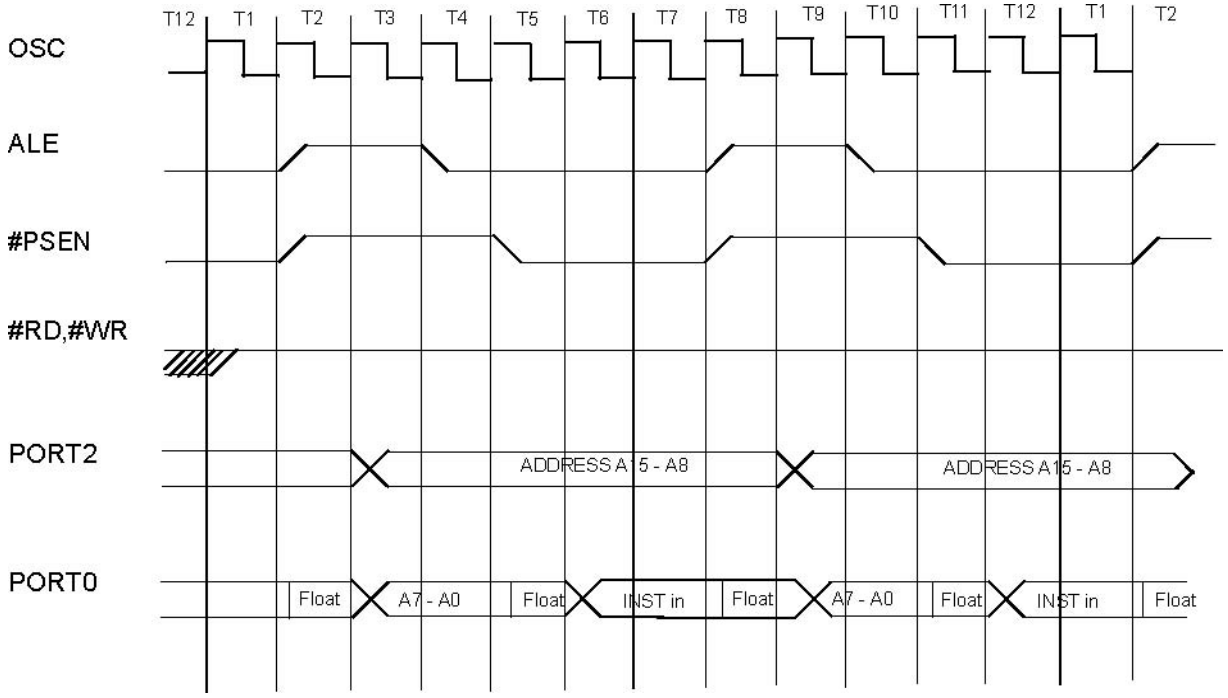


NOTE: Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics.
User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

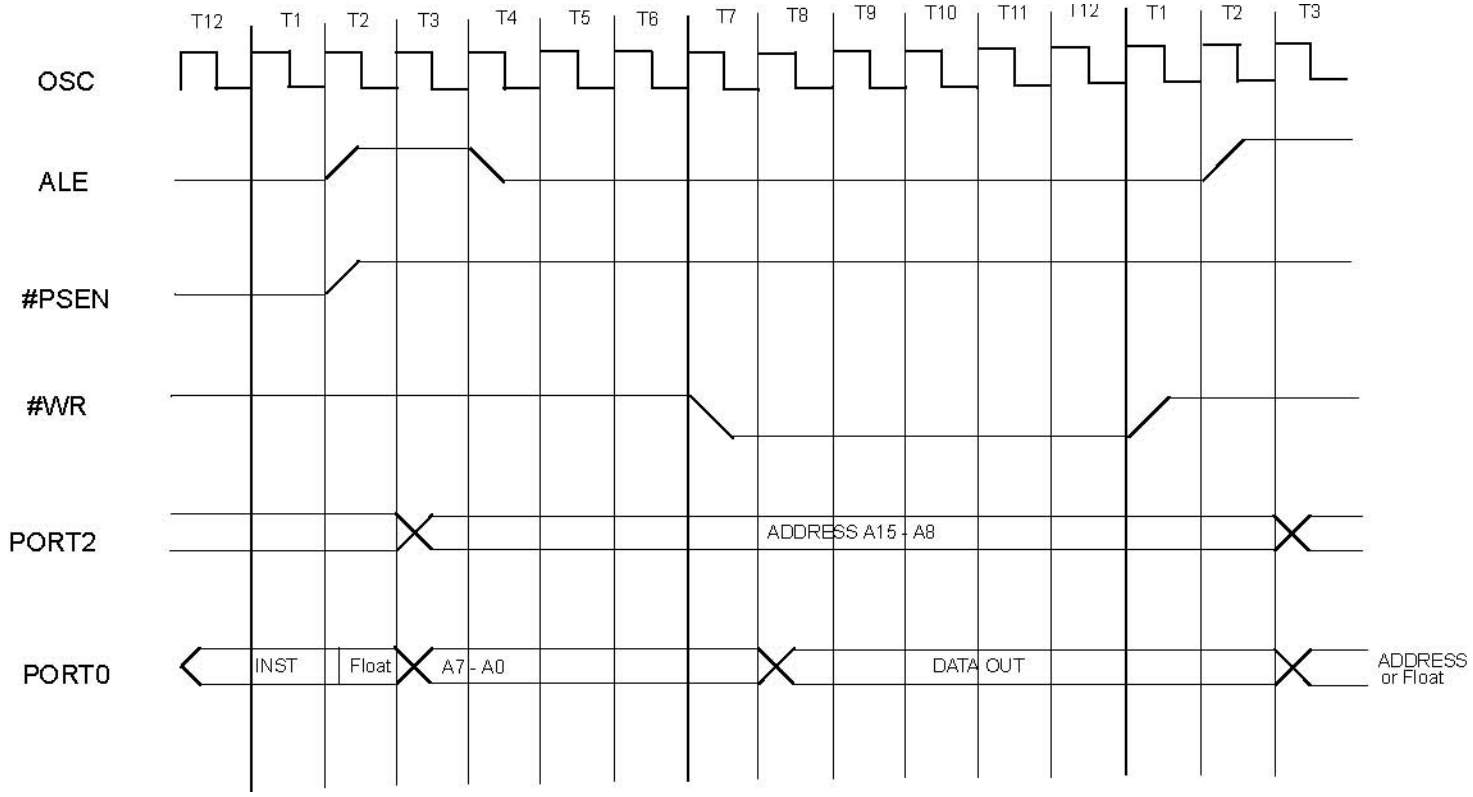
Data Memory Read Cycle Timing



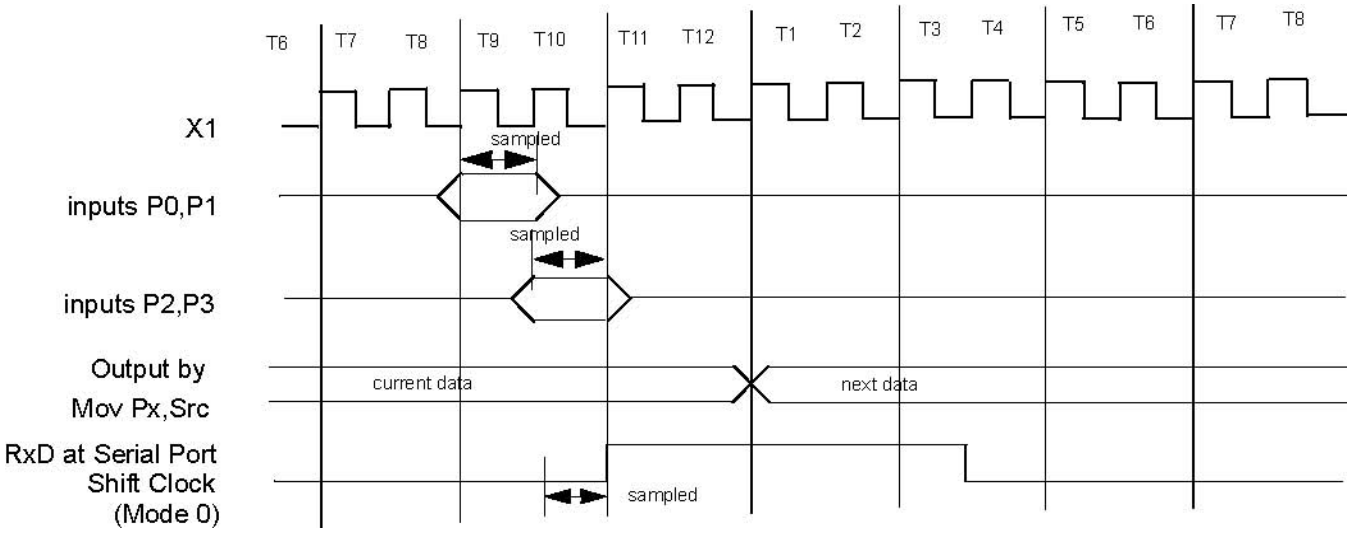
Program Memory Read Cycle Timing



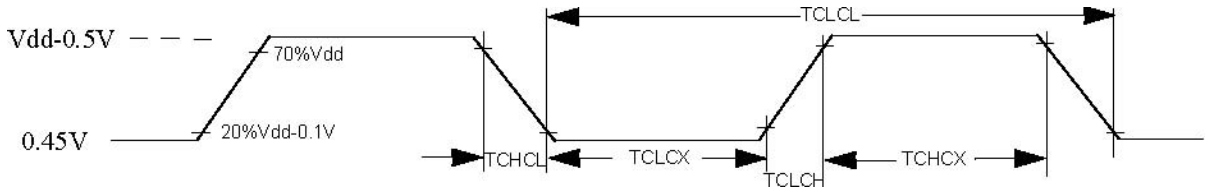
Data Memory Write Cycle Timing



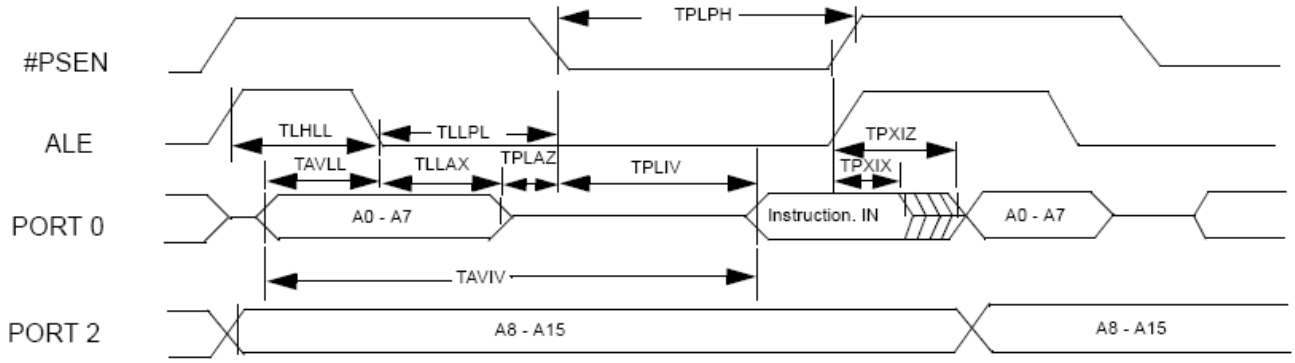
I/O Ports Timing



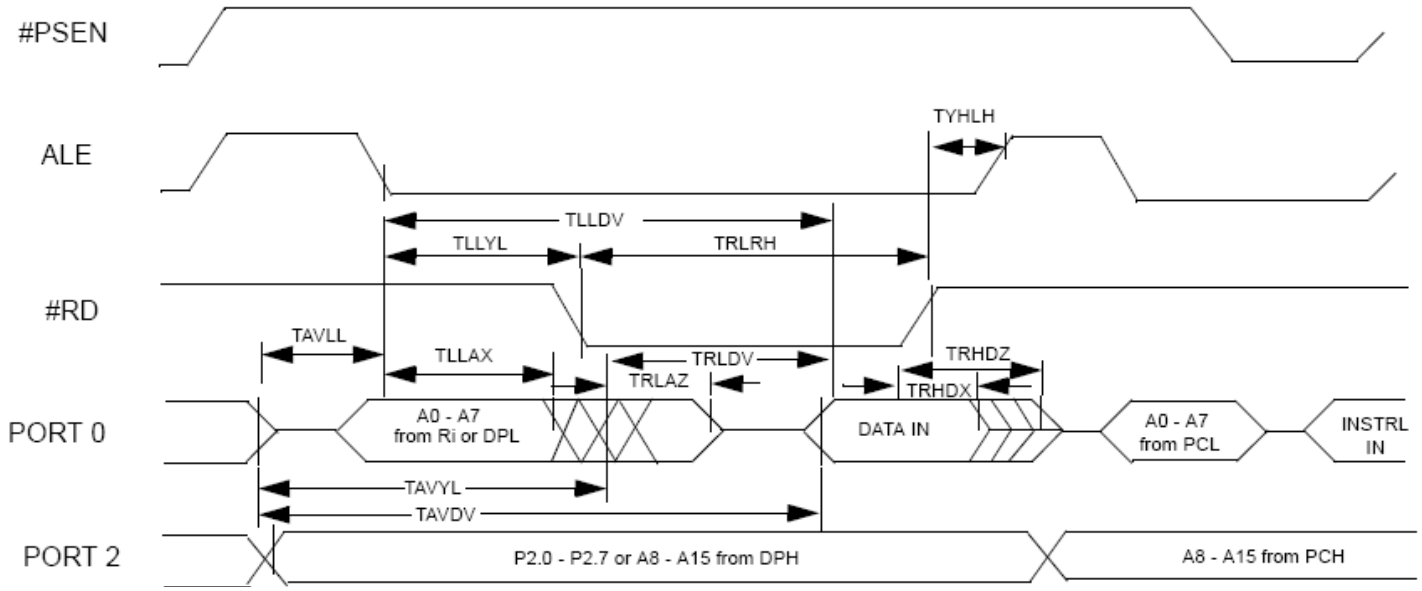
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



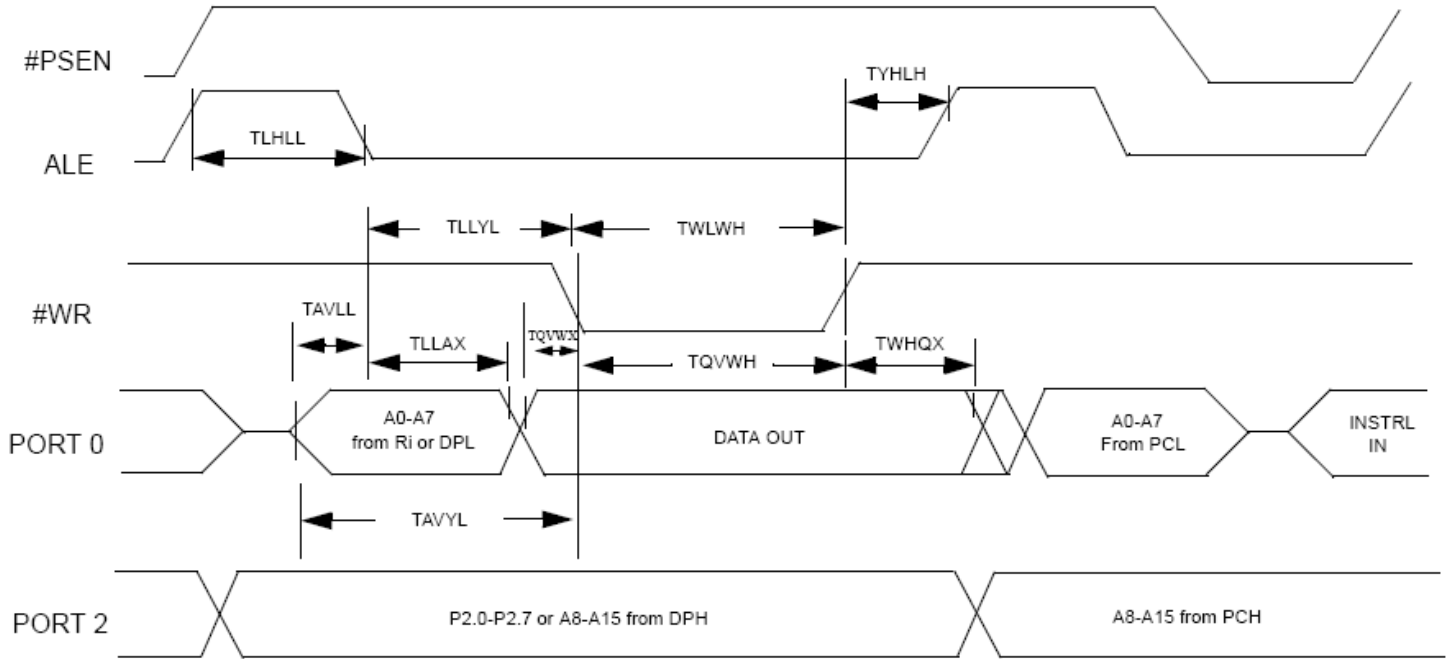
Tm.I External Program Memory Read Cycle



Tm.II External Data Memory Read Cycle



Tm.III External Data Memory Write Cycle



MCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	Lab Tool - 48XP/UXP Lab Tool – 848/848XP
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