FAIRCHILD SEMICONDUCTOR®

February 2010

FCM8201
3-Phase Sinusoidal Brushless DC Motor Controller

Features

- Support Space Vector Modulation (SVM)
- Supports Sine-wave & Square-wave solutions
- Built-in Clock Generator
- Built-in Error Amplifier for Torque Loop Control
- Direct Duty Control
- Square-wave 120°, Sine-wave 180° Turn-on
- PLL Angle Detection (hall-sensors)
- Programmable Current Leading Phase
- Serial Interface (SPI)
- Two Operation Modes (Stand-alone operation or controlled through SPI)
- Programmable Soft-switching (Dead Time)
- Synchronous Rectifying
- Over-voltage & Under-voltage Protections
- Motor & Power Transistors Over-voltage Protections
- Three Levels of Over-current Protections
- Programmable OC Timer
- Over-temperature Protection

Applications

- BLDC Motor Control
- Low Noise Motor Applications
- Fan, Pump, Tools, etc.

Description

FCM8201 is a 3-phase sinusoidal BLDC motor controller. It comes with the advanced hall sensor design. Using the hall sensor signals, the control system is able to execute the PWM commutation by switching the 3-phase inverter. There are two PWM modes for selection - the sine-wave mode and the square-wave mode. The square-wave mode includes PWM-PWM and PWM-ON approaches to improve the efficiency of the motor drive. Complete protection functions including over-voltage, over-current, over-temperature and short circuit protections prevent the control circuits and the motor from being damaged, particularly under stressed applications and demanding environments. To assist users on their operations, information like voltage, current, temperature is easily accessible through the SPI interface.

FCM8201 can be operated stand-alone or worked with microcontrollers for advanced BLDC motor control.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FCM8201QY	-40℃ to 85℃	Green	32LD,LQFP, JEDEC MS-026, VARIATION BCE, 7MM SQUARE	Tray

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Circuits

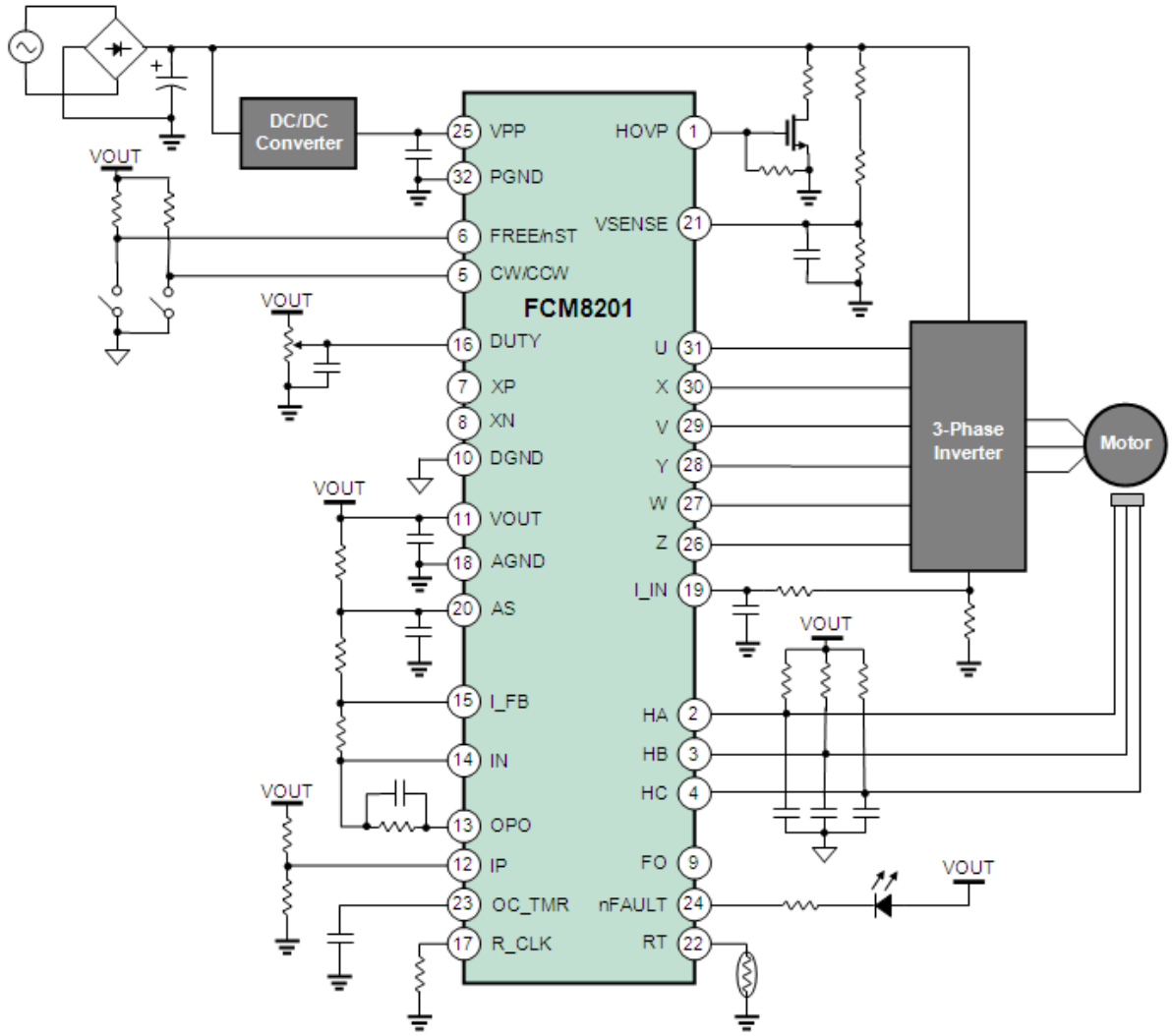


Figure 1. Stand-alone Application

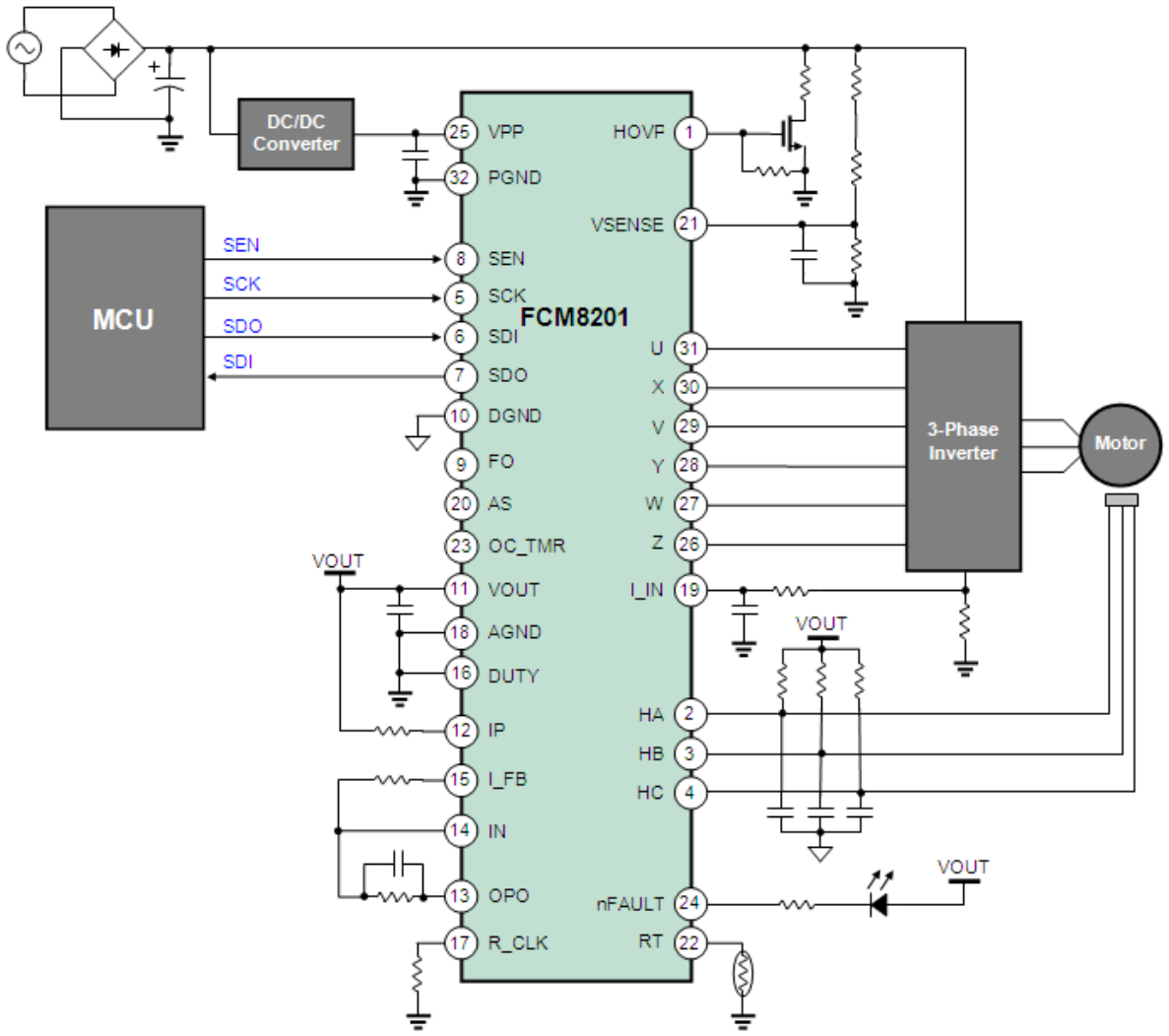


Figure 2. SPI Application

Block Diagram

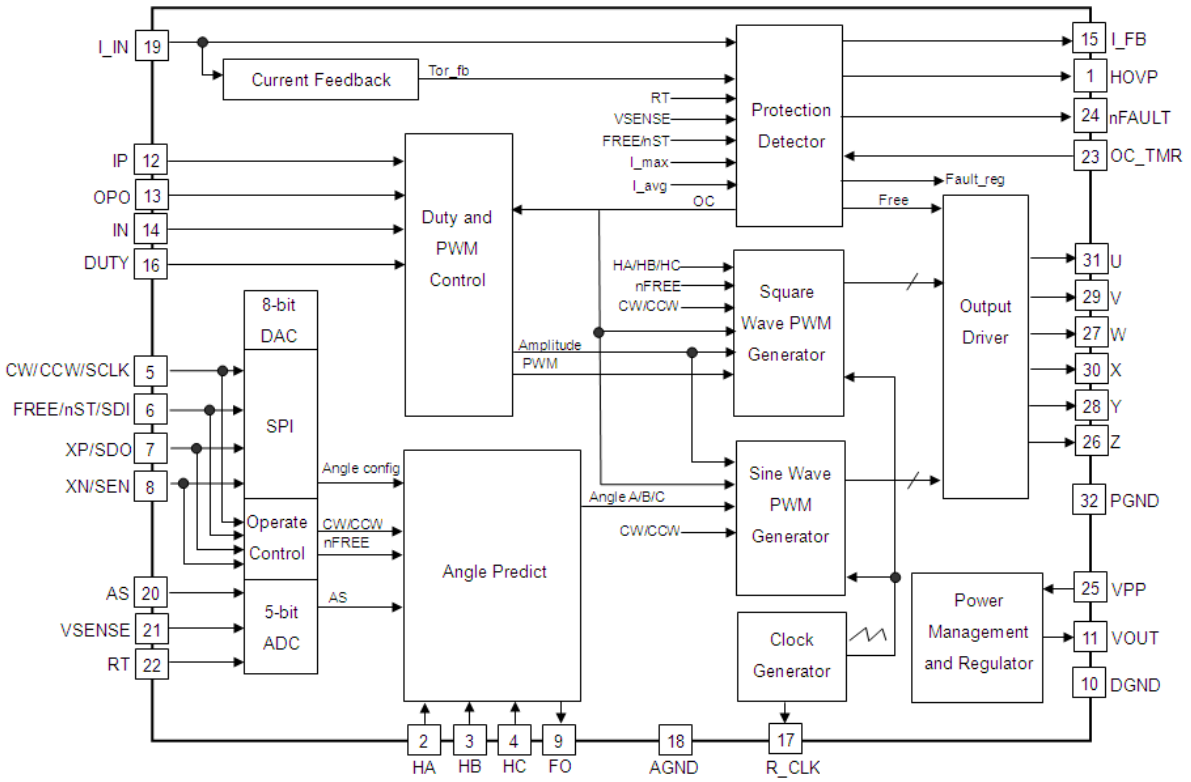
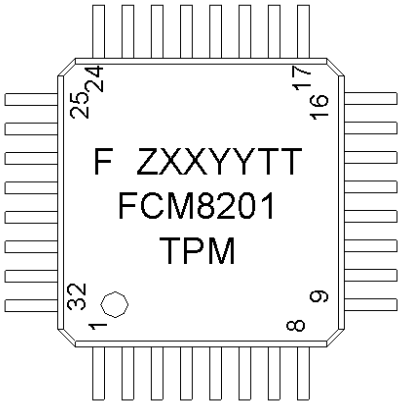


Figure 3. System block diagram

Marking Information



F- Fairchild logo
Z- Plant Code
X- 1 digit year code
Y- 1 digit week code
TT: 2 digits die run code
T: Package type (Q=LQFP)
P: Y=Green package
M: Die run code

Figure 4. Top Mark

Pin Configuration

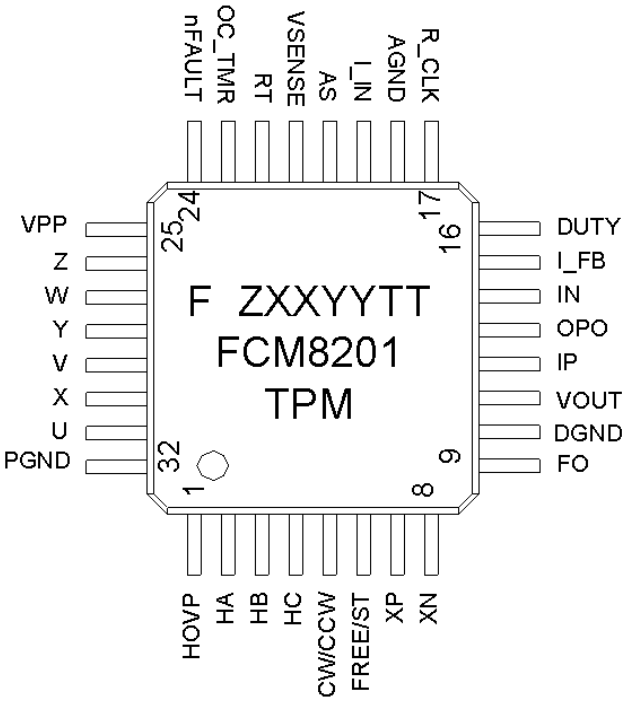


Figure 5. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	HOVP	**Motor Drive Over-voltage Protection Output**. It can be connected to an external power transistor for discharging the Back-EMF.
2	HA	**Hall A Sensor Input**. Phase-U magnetic field detection.
3	HB	**Hall B Sensor Input**. Phase-V magnetic field detection.
4	HC	**Hall C Sensor Input**. Phase-W magnetic field detection.
5	CW/CCW	**Direction Control Input**. Designed for stand-alone operation. High: CW, Low: CCW.
	SCLK	**Serial Clock Input**. Designed for SPI operation.
6	FREE/ST	**Free and Start Control Input**. Designed for stand-alone operation. High: Free, Low: Start.
	SDI	**Serial Data Input**. Designed for SPI operation.
7	XP	**Interface Selection P**, open-drain. Designed to configure the pin #5~8 work on stand-alone or SPI operation.
	SDO	**Serial Data Output**, open-drain. Designed for SPI operation.
8	XN	**Interface Selection N**, open-drain. Designed to configure the pin #5~8 work on stand-alone or SPI operation.
	SEN	**SPI Enable**, open-drain. Designed for SPI operation. High: SPI disable, Low: SPI enable.
9	FO	**Revolution Pulse Output**. Pulses per revolution = Motor Poles ÷ 2 × 3
10	DGND	**Digital Ground**.
11	VOUT	**Voltage Regulator Output.** A 0.1uF (minimum) capacitor should be connected between this

		pin and ground.
12	IP	**Positive Input of Torque Error Amp**.
13	OPO	**Output of Torque Error Amp**.
14	IN	**Negative Input of Torque Error Amp**.
15	I_FB	**Current Feedback Output**.
16	DUTY	**PWM Duty Control Input**. Designed to directly control the PWM duty cycle in stand-alone operation.
17	R_CLK	**External Resistor of Clock Generator**. Designed for determining the frequency of internal clock generator.
18	AGND	**Analog Ground**.
19	I_IN	**Current Feedback Input**.
20	AS	**Angle Shift Input**. Designed for correcting the lead angle of PWM output signals. The range is from 0° to 60° related to the induced magnetic voltage.
21	VSENSE	**Motor Drive Voltage Sensing Resistor**. Designed for determining the voltage level of over-voltage protections.
22	RT	**Thermistor Voltage Input**. Connect to a NTC (Negative Temperature Coefficient) Thermistor for the over-temperature protection.
23	OC_TMR	**Over-load Time-out programmable Input**. Connect to a capacitor for determining the time-delay of over-load protection.
24	nFAULT	**Fault Flag**. Open drain output, Low: system failure.
25	VPP	**Supply Voltage Input**.
26	Z	**PWM Output of W-phase Low-side**.
27	W	**PWM Output of W-phase High-side**.
28	Y	**PWM Output of V-phase Low-side**.
29	V	**PWM Output of V-phase High-side**.
30	X	**PWM Output of U-phase Low-side**.
31	U	**PWM Output of U-phase High-side**.
32	PGND	**High-voltage Ground**.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{VPP}	Supply Voltage	0	30	V
ESD	IEC 61000 Board Level		-	kV
	Human Body Model, JESD22-A114		2	
	Charged Device Model, JESD22-C101		1	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature		-40		+85	℃
V_{PP}	Supply Voltage		10	12	17.5	V
F_{SYS}	System Clock		0.96	1.28	1.92	MHz
R_CLK	Clock Generator External Resistor			12		kΩ
R_{I_IN}	I_IN Bias Resistor			10		kΩ

Electrical Characteristics

V_{PP}=12V and T_A=25℃ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VPP Section						
V_{VPP_ON}	Turn-on Threshold Voltage		8.5	9.0	9.5	V
$V_{VPP\_OFF\_HYS}$	Turn-off Hysteresis Voltage		0.7	0.85	1	V
I_{DD_OP}	Operating Supply Current	V_{PP}=12V, F_{SYS}=1.28MHz	4	5	6	mA
Voltage Regulator Section						
V_{VOUT}	Regulator Output Voltage	Output current 5mA	5.0	5.2	5.4	V
I_{VOUT}	Regulator Output Current	V_{VOUT}=5.2V			10	mA
C_{VOUT}	Regulator External Capacitor		0.1			uF
Digital I/O Section						
V_{IH_HALL}	Hall Signals Input High Level		4.0			V
V_{IL_HALL}	Hall Signals Input Low Level				1.0	V
V_{HYS_HALL}	Hall Signals Hysteresis Voltage		2.0	2.5	3.0	V
T_{DEB_HALL}	Hall Signals De-bounce Time			5		uS
V_{IH_SPI}	SPI Signals Input High Level		2.5		5.3	V
V_{IL_SPI}	SPI Signals Input Low Level		-0.3		1.0	V
V_{OH_SPI}	SPI Signals Output High Level	I_O=4mA	4			V
V_{OL_SPI}	SPI Signals Output Low Level	I_O=4mA			1	V
R_{DIO_UP}	Digital I/O Internal Pull High Resistor		150k	200k	250k	Ohm
High-voltage I/O Section						
V_{OH_PWM}	PWM Signals Output High Level (U/V/W/X/Y/Z)	V_{PP}=12V, I_O=4mA	10			V
V_{OL_PWM}	PWM Signals Output Low Level (U/V/W/X/Y/Z)	V_{PP}=12V, I_O=4mA			1	V
V_{OH_HOVP}	HOVP Output High Level	V_{PP}=12V, I_O=1mA	10			V
V_{OL_HOVP}	HOVP Output Low Level	V_{PP}=12V, I_O=1mA			1	V
PWM Control Section						
V_{FD}	Full Duty Voltage of DUTY Pin		4.4	4.5	4.6	V
V_{ZD}	Zero Duty Voltage of DUTY Pin		0.45	0.5	0.55	V
t_{PWM_MIN}	PWM Minimum On Time	R_CLK=12KΩ		1		uS
T_{DEAD0}	PWM Dead Time	DT[1:0] / PWM_REG=00 (default value)		2		uS
T_{DEAD1}	PWM Dead Time	DT[1:0] / PWM_REG=01		1.5		uS
T_{DEAD2}	PWM Dead Time	DT[1:0] / PWM_REG=10		3.0		uS
T_{DEAD3}	PWM Dead Time	DT[1:0] / PWM_REG=11		2.5		uS
REG_{ZD}	Zero Duty Value of DUTY_REG and IP_REG		0x00		0x07	

F_{PWM_MIN}	PWM Frequency	15KHz: R_CLK=16KΩ 20KHz: R_CLK=12KΩ 30KHz: R_CLK=8KΩ	15	20	30	KHz
I_{O_OPO}	Output Current of Torque Error Amp				0.5	mA
Av_{ERR}	Gain of Torque Error Amp			60		dB
GBW_{ERR}	Unit-gain Band Width of Torque Error Amp			10		MHz
Sine Wave PWM Generator						
V_{SIN_ENA}	Sine Wave Enable Threshold of DUTY Pin			0.75		V
V_{SIN_DIS}	Sine Wave Disable Threshold of DUTY Pin			0.65		V
t_{SIN_ENA}	Sine Wave Enable De-bounce Time			1		mS
t_{SIN_DIS}	Sine Wave Disable De-bounce Time			100		mS
Over-current Protections Section						
V_{OCP_SH}	Short Circuit Current Protection Threshold Voltage	$V_{I\_IN} \geqq V_{OCP\_SH}$		2.5		V
V_{OCP_CYC}	Cycle-by-cycle Current Protection Threshold Voltage	$V_{I\_IN} \geqq V_{OCP\_CYC}$		1.5		V
V_{OCP_OL}	Over-load Current Protection Threshold Voltage	$V_{I\_IN} \geqq V_{OCP\_OL}$		1.4		V
V_{OC_TMR}	OC_TMR Threshold Voltage			2.5		V
I_{TMR_CHG}	OC_TMR Charge Current	OC_TMR=0V		40		uA
I_{TMR_DIS}	OC_TMR Discharge Current	OC_TMR=5V		10		uA
$I_{BIAS\_I\_IN}$	Bias Current of I_IN	R_{I_IN}=10kΩ		50		uA
$I_{O\_I\_FB}$	I_FB Output Current				0.5	mA
G_{I_FB}	I_FB Output Gain			8		
Over/Under-voltage Protections (OVP/UVP) Section						
V_{OV_VPP}	System OVP Threshold Voltage	$V_{PP} > V_{OV\_VPP}$		18		V
$V_{OV\_VPP\_RLS}$	System OVP Release Voltage	$VPP < V_{OV\_VPP\_RLS}$		17		V
t_{OV_VPP}	System OVP De-bounce Time	$V_{PP} \geqq V_{OV\_VPP}$		100		uS
V_{UV_VPP}	System UVP Threshold Voltage	$V_{PP} \leqq V_{UV\_VPP}$		8		V
$V_{UV\_VPP\_RLS}$	System UVP Release Voltage	$VPP > V_{UV\_VPP\_RLS}$		9		V
V_{UV_VOUT}	VOUT UVP Threshold Voltage	$V_{VOUT} \leqq V_{UV\_VOUT}$		4		V
$V_{UV\_VOUT\_RLS}$	VOUT UVP Release Voltage	$VOUT > V_{UV\_VOUT\_RLS}$		4.5		V
V_{OV_MOTOR}	Motor Drive Voltage OVP Threshold Voltage	$V_{VSENSE} \geqq V_{OV\_MOTOR}$		4.5		V
V_{RL_MOTOR}	Motor Drive Voltage OVP Release Voltage	$V_{VSENSE} \leqq V_{RL\_MOTOR}$		4.0		V
Over-temperature Protection (OTP) Section						
V_{RT}	OTP Threshold Voltage	$RT < V_{RT}$		1		V
V_{RT_RLS}	OTP Release Voltage	$RT > V_{RT\_RLS}$		1.2		V

I_{RT}	RT Pin Source Current			50		uA
Pins Open/Short Protection Section						
V_{SHORT}	Pins Short Protection Level	R_CLK pin		0.2		V
V_{OPEN}	Pins Open Protection Level	R_CLK and RT pins		4.8		V

Functional Description

Power Management and Regulator

FCM8201 can be operated in a wide input voltage (VPP) range from 10V to 15V. The VOUT pin is the output terminal of an internal voltage regulator. The typical output voltage ranges between 5V and 5.2V. To stabilize the VOUT circuit, an external capacitor is required to be connected closely between this terminal and the ground of FCM8201. If the VPP voltage is lower than 8V threshold, FCM8201 will be shut-down and all the internal registers of FCM8201 will be reset.

Clock Generator

FCM8201 comes with a programmable oscillator. By determining an externally added resistor R_CLK, the system clock can be programmed from 960 KHz to 1920 KHz. The switching frequency of the PWM signal is equal to 1/64 (divided by ÷64) of the system clock. Therefore, when the system clock is configured as 960 KHz, PWM will be 960 KHz / 64 = 15 KHz. Similarly, if a 20 KHz PWM is intended, the system clock has to be set as 1.28 MHz.

PWM Commutation

FCM8201 supports both the square-wave PWM and the sine-wave PWM for the BLDC motor control. The controller comes with the hall-sensor design which is used to align the rotor position of the motor. For the square-wave PWM mode, the PWM output commutation (PWM-PWM and PWM-ON) is shown at Table 1 and Table 2. The square-wave PWM modes can be selected by setting an internal control register of FCM8201 through the SPI interface. The default value of PWM-PWM Commutation is shown at Table 1.

Table 1. Square Wave “PWM-PWM” Commutation

CW	Hall	Hall	U-V-W	X-Y-Z
X	000	0	0-0-0	0-0-0
X	111	7	0-0-0	0-0-0
1	001	1	P-0-0	Pb-1-0
1	011	3	0-0-P	0-1-Pb
1	010	2	0-0-P	1-0-Pb
1	110	6	0-P-0	1-Pb-0
1	100	4	0-P-0	0-Pb-1
1	101	5	P-0-0	Pb-0-1
0	101	5	0-0-P	1-0-Pb
0	100	4	0-0-P	0-1-Pb
0	110	6	P-0-0	Pb-1-0
0	010	2	P-0-0	Pb-0-1
0	011	3	0-P-0	0-Pb-1
0	001	1	0-P-0	1-Pb-0

Table 2. Square Wave “PWM-ON” Commutation

CW	Hall	Hall	U-V-W	X-Y-Z
X	000	0	0-0-0	0-0-0
x	111	7	0-0-0	0-0-0
1	001	1	1-Pb-0	0-P-0
1	011	3	0-0-P	0-1-Pb
1	010	2	Pb-0-1	P-0-0
1	110	6	0-P-0	1-Pb-0
1	100	4	0-1-Pb	0-0-P
1	101	5	P-0-0	Pb-0-1
0	101	5	0-0-P	1-0-Pb
0	100	4	0-Pb-1	0-P-0
0	110	6	P-0-0	Pb-1-0
0	010	2	1-0-Pb	0-0-P
0	011	3	0-P-0	0-Pb-1
0	001	1	Pb-1-0	P-0-0

Note:
P=PWM, Pb=PWM inverse.

HALL Signals Input

FCM8201 provides a 3~6 usec de-bounce time for each hall signal input in order to reduce the glitch of the hall signals. When the transition of the hall signal is slow, a glitch might be produced and an error may follow. Through a built-in hall signal regulation circuit, FCM8201 minimizes the risks of the glitches and the related errors. This function can be enabled or disabled through a control register of FCM8201 via the SPI interface.

The hall signals polarity can be configured by setting the levels of HA_INV, HB_INV and HC_INV. For example, if HA_INV=1, an internal hall-a signal will be the inverse of the HA pin. Otherwise, the internal hall-a signal will be the same as the signal on the HA pin.

PWM Duty Cycle and Operation

The PWM duty is proportional to the voltage levels on the “OPO pin” and “DUTY pin”. A FREE/nST pin is utilized to enable the PWM signals. When FREE/nST pin is set as logic-high, the PWM state will be in the free mode, and all PWM outputs (U, V, W, X, Y, Z pins) will be in logic-low. Once the FREE/nST pin goes logic-low, the FCM8201 will start operating the PWM. FCM8201 supports various PWM operation modes to fit different application needs. The detailed description is shown at “Register Map Table”.

Sine Wave Generator

FCM8201 includes a space vector modulation (SVM) for the sine-wave PWM. An angle-detect circuit will phase-lock the rotor position by using hall signals of the motor. The resolution is 32 steps per 60 degree. Through the PWM operation, the motor current of each phase will be sine-wave. The angle shift between each phase is 120 degree.

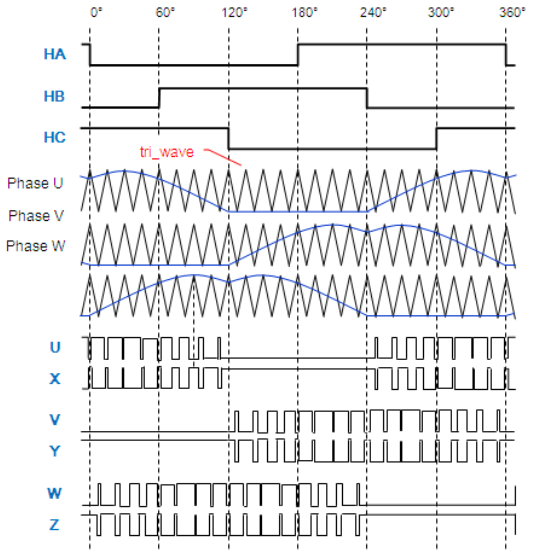


Figure 6. Sine Wave Output @ CW=1

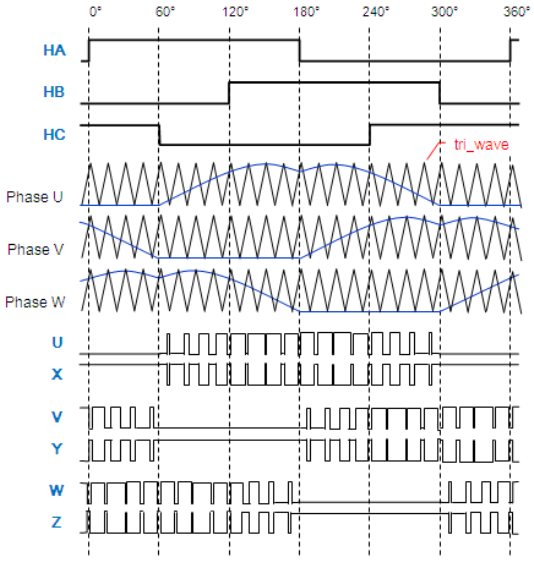
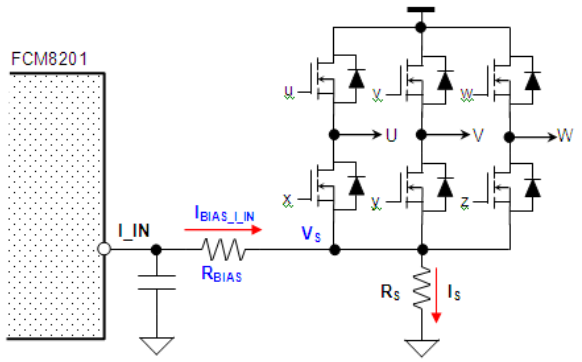


Figure 7. Sine Wave Output @ CW=0

Figure 8.

Current Feedback and Protections

The current feedback circuit provides two major functions: (1) for generating a current feedback signal for the motor control (2) for the over-current protections. The I_IN pin will output 50uA current to provide a DC bias on the I_IN terminal to prevent a negative voltage.. It is shown on equation (1) for the I_FB and the I_IN. A 0.5V DC bias on I_IN is recommended. The maximum average current signal is 1V. By using these parameters, the maximum I_FB signal swing will be 0.5V~4.5V.



$$V_{I\_FB} = (V_S \times 8) + (I_{BIAS\_I\_IN} \times R_{BIAS}) \quad (1)$$

FCM8201 provides three different levels of over-current (OC) protections. The 1st level is 1.4V; it is used for over-load current protection with OC timer delay. If the I_IN is higher than 1.4V, the OC timer will be triggered. The OC_Latch will be enabled once the timer is exceeds its time-out limit. The 2nd level is 1.5V. It is used for the cycle-by-cycle current limit. The PWM signal will be turned off immediately when the I_IN is > 1.5V. The 3rd level is 2.5V. It is designed for the short circuit protection. If th3 I_IN is > 2.5V with over 3 PWM pulses, all PWM outputs (U, V, W, X, Y, Z pins) will be turned off.

Protections and Faults

Table 3. Faults Table

Type	State	Trigger	Release
VPP OV	Free	VPP > 18V	
VPP UV	Free, Reset	VPP < 8V	
VOUT UV	Free	VOUT < 4V	
RT	Free	RT < 1.0V	RT > 1.2V
OS	Free	Open & Short	↑Run
Hall Error	Free	Hall = 000 or 111	
HOVP	Free	VSENSE > 4.5V	
OC_Latch	Free	I_IN > 1.4V	↑Run
Watch Dog	Free	WDT time out	Register
SHORT	Free	I_IN > 2.5V	↑Run

Digital to Analog Converter

FCM8201 has an 8-bit DAC (digital-to-analog converter) for controlling the DUTY and IP through the SPI interface.

Analog to Digital Converter

FCM8201 has a 5-bit ADC (analog-to-digital converter) for the signal on AS, VSENSE, I_FB and RT terminals. Its voltage can be read through the SPI interface.

I/O Optional Function

Two types of I/O for both stand-alone and microcontroller applications.

SPI Interface

The microcontroller can access FCM8201 through the SPI interface.

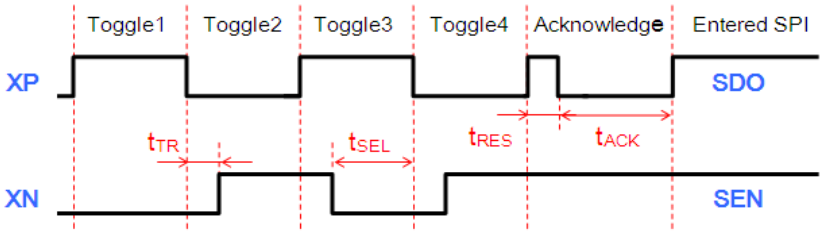


Figure 9. I/O Select Timing of Entering SPI Mode

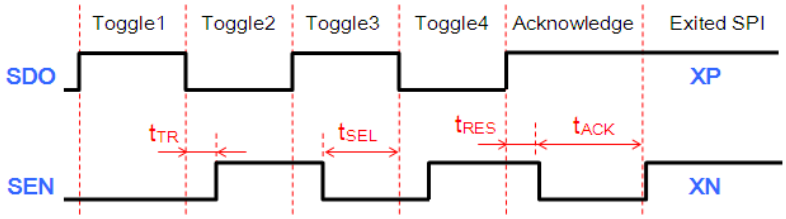


Figure 10. I/O Select Timing of Exiting SPI Mode

Table 4. Timing Specification of I/O Function Selection

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{SEL}	Select-bit Stable Time	F_{SYS}=1.28MHz	12		100	uS
t_{TR}	Select-bit Transient Time	F_{SYS}=1.28MHz	0		12	uS
t_{ACT}	Acknowledge Bit Pull Low Time	F_{SYS}=1.28MHz		1		mS
t_{RES}	FCM8201 Response Time	F_{SYS}=1.28MHz		4		uS

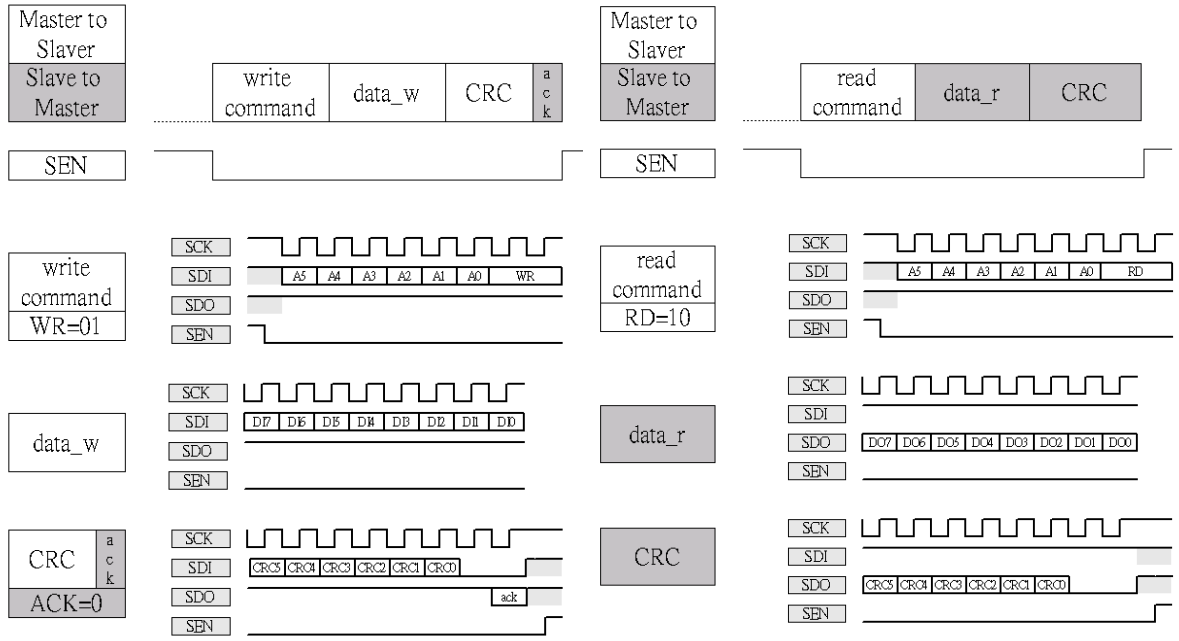


Figure 11. SPI Bit Definition

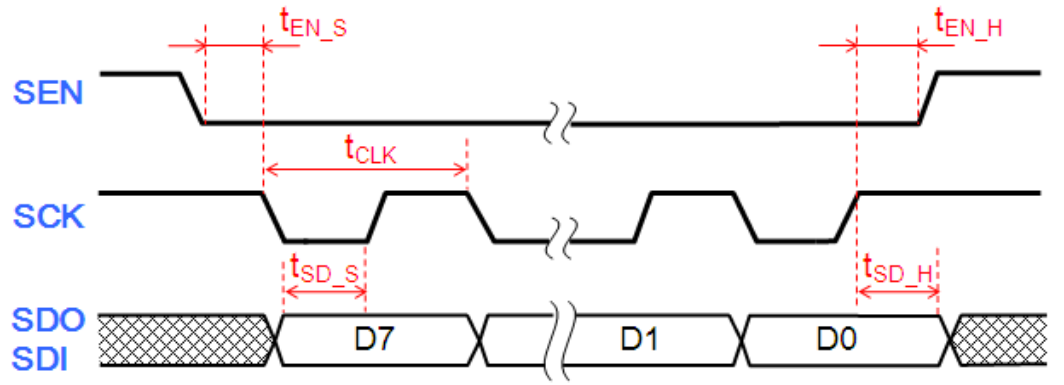


Figure 12. SPI Timing Specification

Table 5. Timing Specification of SPI

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{EN_S}	Setup Time of SEN	F_{SYS}=1.28MHz		2		uS
t_{EN_H}	Hold Time of SEN	F_{SYS}=1.28MHz		2		uS
t_{SD_S}	Setup Time of SDO/SDI	F_{SYS}=1.28MHz		0		uS
t_{SD_H}	Hold Time of SDO/SDI	F_{SYS}=1.28MHz		2		uS
t_{CLK}	Maximum Clock Rate of SPI	F_{SYS}=1.28MHz	12.5			uS
t_{TMR_OUT}	SCK Time Out	F_{SYS}=1.28MHz	90	100		mS

Table 6. SPI Register Table (Read/Write)

CNTL_REG : System Control Register

Addr.	Name	Type	b7	b6	b5	b4	b3	b2	b1	b0
0x00	CNTL	W/R	TMR_CLR	OC_TMR2	OC_TMR1	OC_TMR0	IP_EA	DT_EA	CW	FREE/nST
		Reset	0	0	0	0	0	0	1	1

b7	TMR_CLR	OC Timer Clear. 1= OC timer clear, 0= OC time is normal function
b[6:4]	OC_TMR[2:0]	Over-load Current Protection Timer Configuration. 000= OC timer configure by OC_TMR pin 001= OC timer configure to 2^18 ÷ F_{SYS} 010= OC timer configure to 2^19 ÷ F_{SYS} 011= OC timer configure to 2^20 ÷ F_{SYS} 100= OC timer configure to 2^21 ÷ F_{SYS} 101= OC timer configure to 2^22 ÷ F_{SYS} 110= OC timer configure to 2^23 ÷ F_{SYS} 111= OC timer configure to 2^24 ÷ F_{SYS}
b3	IP_EA	IP_REG Enable. 1= duty control by IP_REG, 0= duty control by IP pin
b2	DT_EA	DUTY_REG Enable. 1= duty control by DUTY_REG, 0= duty control by DUTY pin
b1	CW	Output Driving Current Direction. 1= CW, 0= CCW
b0	FREE/nST	FREE or START. 1= FREE (PWM outputs disable), 0= START (PWM outputs enable)

PWM_REG : PWM Control Register

Addr.	Name	Type	b7	b6	b5	b4	b3	b2	b1	b0
0x01	PWM	W/R	PMOD	n/a	DT1	DT0	SEQ_TBL	SYNCOFF	EXT_SYN	LPWM
		Reset	0	0	0	0	0	0	0	0

b7	PMOD	PWM Mode Select. 0= sine wave PWM drive after angle detector locked 1= square wave PWM drive after angle detector locked
b[5:4]	DT[1:0]	Soft Switching Dead Time Setting. 00= 2uS, 01= 1.5uS, 10= 1uS, 11= 0.5uS
b3	SEQ_TBL	Square Wave Sequencer Table Select. 0= “PWM-PWM” commutation, 1= “PWM-ON” commutation
b2	SYNCOFF	Synchronous Rectifier (SR) Disable. 0= SR enable, 1= SR disable
b1	EXT_SYN	External Synchronous Rectifier Configure. 0= SR function control by SYNCOFF bit. 1= SR function control by OC_TMR pin. In this selection, the OC_TMR[2:0] bits of CNTL_REG can’t be set to 0, too. OC_TMR pin: high= SR enable, low= SR disable
b0	LPWM	Low Side Minimum PWM Output Enable. This function is working only on square wave PWM driving. 0= Low side minimum PWM duty output disable 1= Low side minimum PWM duty output enable

ANG_REG : Angle Shift Control Register

Addr.	Name	Type	b7	b6	B5	b4	b3	b2	b1	b0
0x02	ANG	W/R	ANG_SEL	ARNG1	ARNG0	ANG4	ANG3	ANG2	ANG1	ANG0

		Reset	0	0	0	0	0	0	0	0
		b7	ANG_SEL	Angle Shift Control Input Select. 0= Set by AS pin, 1= Set by ANG[4:0]						
		b[6:5]	ARNG[1:0]	Angle Predictor Working Range Select. 0,0= Work in 0.8 ~ 80Hz Hall Frequency, 48 ~ 4800 rpm @ 2 poles motor. 0,1= Work in 0.4 ~ 40Hz Hall Frequency, 24 ~ 2400 rpm @ 2 poles motor. 1,x= Work in 3.2 ~ 320Hz Hall Frequency, 192 ~ 19200 rpm @ 2 poles motor.					
		b[4:0]	ANG[4:0]	Angle Setting of Angle Shift Function. 0~31= 0 ~ 60 degree						

SVM_REG : Sine Wave Generator Control Register

Addr.	Name	Type	b7	b6	B5	b4	b3	b2	b1	b0
0x03	SVM	W/R	SIN_MAU	SIN_EA	n/a	n/a	n/a	n/a	n/a	n/a
		Reset	0	0	0	0	0	0	0	0
		b7	SIN_MAU	Sine Wave Driving Force Active. 0= Sine wave automatic active 1= Sine wave active by SIN_EA bit and ignore AS<0.2V						
		b6	SIN_EA	Sine Wave Enable. (This function only active on while SIN_MAU=1) 0= Sine wave disable, 1= Sine wave enable						

HALL_REG : Hall Signals Control Register

Addr.	Name	Type	b7	b6	B5	b4	b3	b2	b1	b0
0x04	HALL	W/R	n/a	n/a	n/a	n/a	HREG	HC_INV	HB_INV	HA_INV
		Reset	0	0	0	0	0	0	0	0
		b3	HREG	Hall Signals Regulation Enable. 0= disable, 1= enable.						
		b2	HC_INV	Hall C Input Invert. 0= non-invert, 1= invert						
		b1	HB_INV	Hall B Input Invert. 0= non-invert, 1= invert						
		b0	HA_INV	Hall A Input Invert. 0= non-invert, 1= invert						

WDT_REG : Watch Dog Timer Control Register

Addr.	Name	Type	b7	b6	b5	b4	b3	b2	b1	b0
0x06	WDT	W/R	OSL_DIS	OTL_DIS	n/a	CRC_ON	WDT_EN	CLR	W_TMR1	W_TMR0
		Reset	0	0	0	0	0	0	0	0
		b7	OSL_DIS	Open Short (OS) Fault Latch Disable. 0= OS protect will not latch 1= OS protect will latch, and clear by FREE/nST pin rising edge or FREE/nST bit = 1						
		b6	OTL_DIS	Over Temperature Fault Latch Disable. 0= OTP protect will not latch 1= OTP protect will latch, and clear by FREE/nST pin rising edge or FREE/nST bit = 1						
		b4	CRC_ON	SPI CRC Check Enable. 0= SPI CRC check disable 1= SPI CRC check enable						
		b3	WDT_EN	Watch Dog Timer Enable. 0= watch dog timer disable 1= watch dog timer enable, and outputs will be faulty when the counter reaches time-out.						

	b2	CLR	Watch Dog Timer Clear. This bit is effective only when WDT_EN=1. 1= WDT counter reset. After counter is cleared to zero, this bit will be auto-reset to 0.
	b[1:0]	W_TMR[1:0]	Watch Dog Timer Counter Select. 0,0= 0.25 sec. @ F_{SYS}=1.28MHz 0,1= 0.5 sec. @ F_{SYS}=1.28MHz 1,0= 1 sec. @ F_{SYS}=1.28MHz 1,1= 2 sec. @ F_{SYS}=1.28MHz

DUTY_REG : Duty Control Register

Addr.	Name	Type	b7	b6	b5	b4	b3	b2	b1	b0
0x08	DUTY	W/R	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0
		Reset	0	0	0	0	0	0	0	0
		b[7:0]	DUTY[7:0]	DUTY Level Configure. 0 ~ 255 = 0.5 ~ 4.5V						

IP_REG : Error Amp IP Pin Control Register

Addr.	Name	Type	b7	b6	b5	b4	b3	b2	b1	b0
0x09	IP	W/R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
		Reset	0	0	0	0	0	0	0	0
		b[7:0]	IP[7:0]	IP Pin Level of Error Amp Configure. 0 ~ 255 = 0.5 ~ 4.5V						

Table 7. SPI Registers Table (Read Only)

AS_REG : AS Pin Voltage Level Read Register										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x20	AS	R	n/a	n/a	n/a	AS4	AS3	AS2	AS1	AS0
b[4:0]		AS[4:0]	AS voltage = (AS[4:0] × 0.125) + 0.5V							
VSENSE_REG : VSENSE Pin Voltage Level Read Register										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x21	VSENSE	R	n/a	n/a	n/a	VS4	VS3	VS2	VS1	VS0
b[4:0]		VS[4:0]	VSENSE voltage = (VS[4:0] × 0.125) + 0.5V							
I_FB_REG : I_FB Pin Voltage Level Read Register										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x22	I_FB	R	n/a	n/a	n/a	IFB4	IFB3	IFB2	IFB1	IFB0
b[4:0]		IFB[4:0]	I_FB voltage = (IFB[4:0] × 0.125) + 0.5V							
RT_REG : RT Pin Voltage Level Read Register										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x23	RT	R	n/a	n/a	n/a	RT4	RT3	RT2	RT1	RT0
b[4:0]		RT[4:0]	RT voltage = (RT[4:0] × 0.125) + 0.5V							
HPERH_REG : Hall Period Counter High Byte										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x26	HPERH	R	HP15	HP14	HP13	HP12	HP11	HP10	HP9	HP8
b[7:0]		HP[15:8]	Hall period count high byte, bit [15:8]							
HPERL_REG : Hall Period Counter Low Byte										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x27	HPERL	R	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
b[7:0]		HP[7:0]	Hall period count low byte, bit [7:0]							
STATUS_REG : System Status Register										
Addr.	**Name**	**Type**	**b7**	**b6**	**b5**	**B4**	**b3**	**b2**	**b1**	**b0**
0x28	STATUS	R	OT	OC	OS	OV	H_ERR	DIR	WDT	SHORT
b7		OT	1= Over-temperature protection was triggered. (RT pin voltage $<$ V_{RT})							
b6		OC	1= Over-load current protection was triggered.							
b5		OS	1= Open/Short protection was triggered.							
b4		OV	1= Motor drive over-voltage protection was triggered. (VSENSE pin voltage $>$ V_{OV_MOTOR})							
b3		H_ERR	1= Hall signals error. (HA/B/C=1/1/1 or 0/0/0)							
b2		DIR	1= Hall direction was different from that on the PWM sequencer table.							
b1		WDT	1= Watch dog time-out was triggered.							
b0		SHORT	1= Short circuit current protection was triggered.							

Physical Dimensions

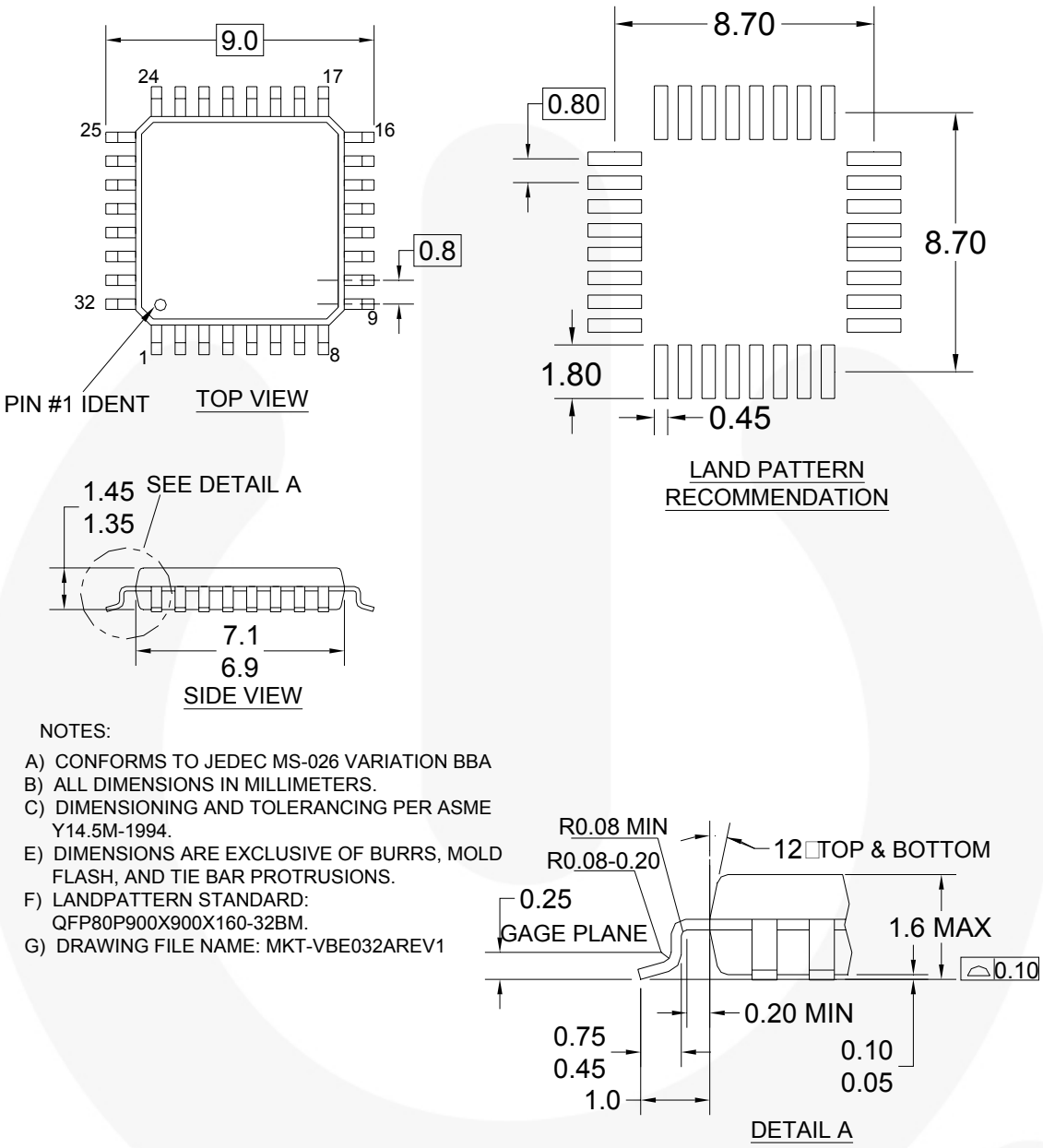


Figure 13. FCM8201QY Outline Dimension

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
Auto-SPM™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TriFault Detect™
TRUECURRENT™*
µSerDes™
SerDes
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I47