MicrOne 微盟电子

High Performance Off-Line Controller ME8100

General Description

ME8100 Series is a high performance green-energy offline power supply controller. It features a scalable driver for driving external NPN or MOSFET transistors for line voltage switching. This proprietary architecture enables many advanced features to be integrated into a small package(TO-92),resulting in lowest total cost solution.

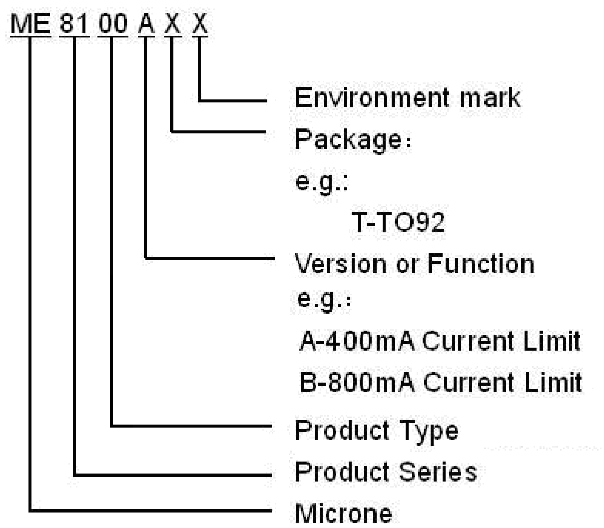
The ME8100 design has 6 internal terminals and is a pulse frequency and width modulation IC with many flexible packaging options. One combination of internal terminals is packaged in the space-saving TO-92 package (A/B versions) for 65kHz switching frequency and with 400mA or 800mA current limit. Consuming only 0.15W in standby, the IC features over-current, hiccup mode short circuit, and under-voltage protection mechanisms.

The ME8100 is ideal for use in high performance universal adaptors and chargers.

Features

- Lowest Total Cost Solution
- 0.15W Standby Power
- Emitter Drive Allows Safe NPN Flyback Use
- Hiccup Mode Short Circuit
- Current Mode Operation
- Over-Current Protection
- Under-voltage Protection with Auto-restart
- Proprietary Scalable Output Driver
- Flexible Packaging Options(including TO-92)
- 65kHz Switching Frequency
- Selectable 0.4A to 0.8A Current Limit

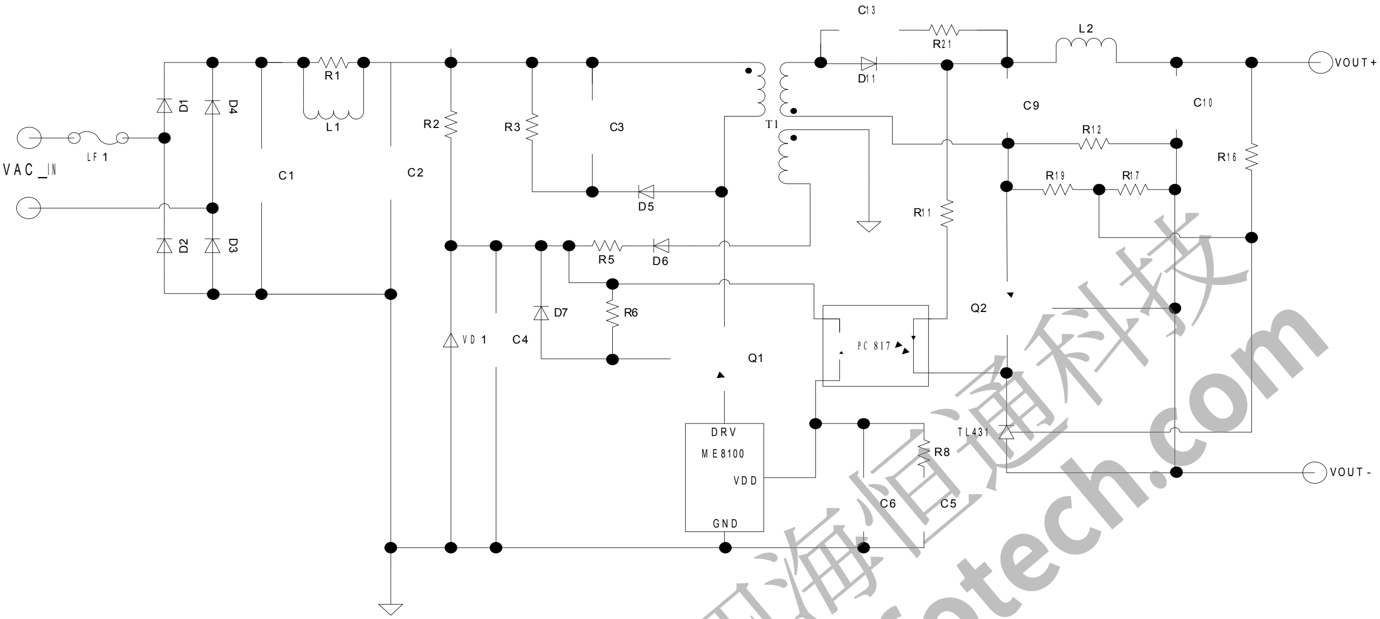
Selection Guide



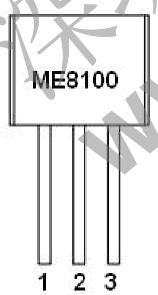
Typical Application

- Battery Chargers
- Power Adaptors
- Standby Power Supplies
- Appliances
- Universal Off-line Power Supplies

Typical Application Circuit



Pin Configuration& Pin Assignment



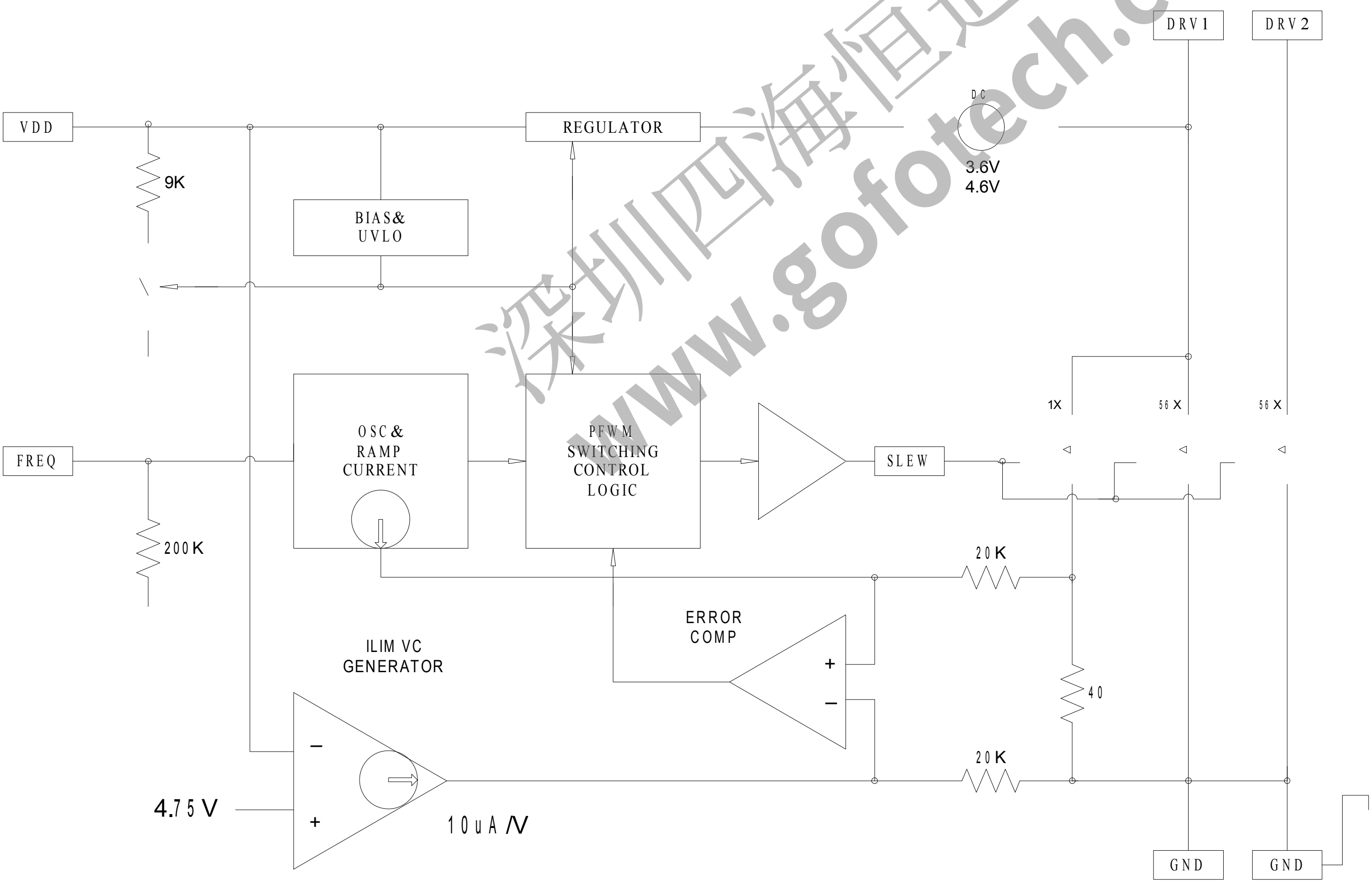
TO-92

Pin Number	Pin Name	Function
TO-92		
1	VDD	Power Supply Pin. Connect to optocoupler's emitter. Internally limited to 5.5V max. Bypass to GND with a proper compensation network.
2	GND	Ground
3	DRV	Driver Output (TO-92 Only). Connect to emitter of the high voltage NPN or MOSFET.

Absolute Maximum Ratings

Parameter		Symbol	Ratings	Units
VDD Pin Voltage		V_{DD}	-0.3 to 6	V
DRV Pin voltage		V_{DRV}	-0.3 to 18	V
VDD current		I_{DD}	20	mA
Continuous Total Power Dissipation	TO-92	P_D	500	mW
Operating Ambient Temperature		T_{OPR}	-25~+125	℃
Storage Temperature		T_{STG}	-40~+125	℃
Soldering temperature and time		T_{SOLDER}	260℃, 10s	

Block Diagram



Electrical Characteristics

ME8100AXX/BXX((Measuring conditions：Unless otherwise specified , V_{IN}=4V，T_{OPT}=25℃)

Symbol	Parameter	Conditions		Min	Typ.	Max	Units
V_{START}	VDD Star Voltage	Rising edge		4.75	5	5.25	V
V_{DRVST}	DRV Start Voltage	DRV must be higher than this voltage to star up			9	11	V
V_{SCDRV}	DRV Short-Circuit Detect Threshold				5.8		V
V_{UV}	VDD Under-voltage Threshold	Falling edge		3.17	3.35	3.53	V
	VDD Clamp Voltage	10mA		5.15	5.45	5.75	V
I_{DDST}	Startup Supply Current	VDD=4V before V_{UV}			0.15	0.45	mA
I_{DD}	Supply Current				0.4	1.0	mA
F_{SW}	Switching Frequency	F_{REQ}=0		50	60	80	KHz
D_{MAX}	Maximum Duty Cycle	VDD=4V	ME8100A	67	75	83	%
			ME8100B	60			
D_{MIN}	Minimum Duty Cycle	VDD=4.6V			5.5		
I_{LIM}	Effective Current Limit	VDD=V_{UV} +0.1v	ME8100A		400		mA
			ME8100B		800		
G_{GAIN}	VDD to DRV Current Coefficient				-0.2		A/V
R_{VDD}	VDD Dynamic Impedance				9		kΩ
	DRV Rise Time	1nF load,15Ω pull-up			30		ns
	DRV Fall Time	1nF load,15Ω pull-up			20		ns

Function Description

As the Functional Block Diagram of the ME8100. The main components include switching control logic, two on-chip Medium-voltage power-MOSFETs with parallel current sensor, driver, oscillator and ramp generator, current limit VC generator, error comparator, hiccup control, bias and undervoltage-lockout, and regulator circuitry.

The design has 6 internal terminals. VDD is the power supply terminal.DRV1 and DRV2 are linear driver outputs that can drive the emitter of an external high voltage NPN transistor or N-channel MOSFET. This emitter-drive method takes advantage of the high VCBO of the transistor, allowing a low cost transistor such as 13003 (VCBO＝700V) or 13002 (VCBO＝600V) to be used for a wide AC input range. The slew-rate limited driver coupled with the turn-off characteristics of an external NPN result in lower EMI.

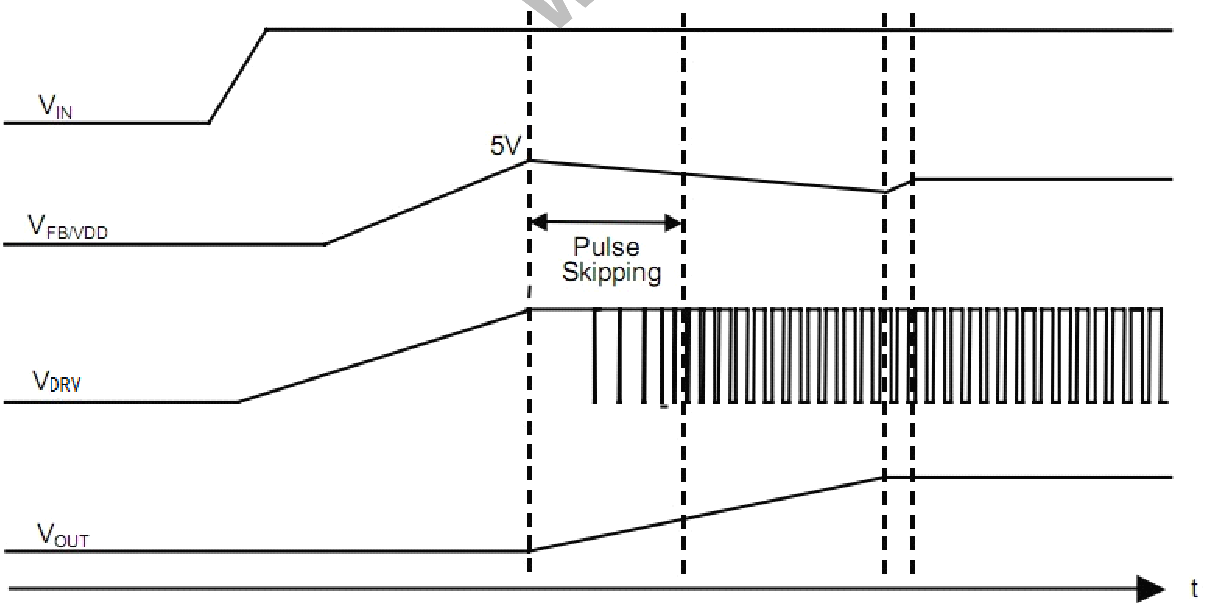
The driver peak current is designed to have a negative voltage coefficient with respect to supply voltage VDD, so that lower supply voltage automatically results in higher DRV1 peak current. This way, the optocoupler can control VDD directly to affect driver current.

Startup Sequence

As the typical application Circuit for the ME8100. Initially, the small current through resistor R2 charges up the capacitor C4, and the BJT acts as a follower to bring up the DRV1 voltage. An internal regulator generates a VDD voltage equal to VDRV1－3.6V for ME8100A (VDRV1－4.6V for ME8100B) but limits it to 5.5VMAX. As VDD crosses 5V, the regulator sourcing function stops and VDD begins to drop due to its current consumption. As VDD voltage decreases below 4.75V, the IC starts to operate with increasing driver current. When the output voltage reaches regulation point, the optocoupler feedback circuit stops VDD from decreasing further. The switching action also allows the auxiliary windings to take over in supplying the C4 capacitor. The following sketch map shows a typical startup sequence for the ME8100.

To limit the auxiliary voltage, use a 12V zener diode for ME8100A or a 13V zener for ME8100B (VD1 diode in Typical Application).

Even though up to 2MΩ startup resistor (R2) can be used due to the very low startup current, the actual R2 value should be chosen as a compromise between standby power and startup time delay.



Normal Operation

In normal operation, the feedback signal from the secondary side is transmitted through the optocoupler as a current signal into VDD pin, which has dynamic impedance of 9kΩ. The resulting VDD voltage affects the switching of the IC. As seen from the Functional Block Diagram, the Current Limit VC Generator uses the VDD voltage difference with 4.75V to generate a proportional offset at the negative input of the Error Comparator.

The drivers turn on at the beginning of each switching cycle. The current sense resistor current, which is a fraction of the transformer primary current, increases with time as the primary current increases. When the voltage accross this current sense resistor plus the oscillator ramp signal equals Error Comparator's negative input voltage, the drivers turn off. Thus, the peak DRV1 current has a negative voltage coefficent of -0.29A/V and can be calculated from the following:

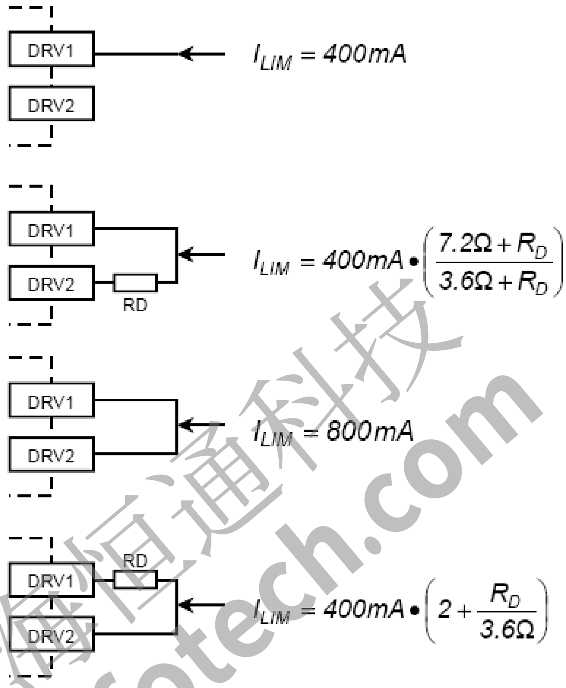
IDRV1PEAK = 0.2A/V×(4.75V – VDD)

for VDD<4.75V and duty cycle<50%.When the output voltage is lower than regulation, the current into VDD pin is zero and VDD voltage decreases. At VDD = VUV = 3.35V, the peak DRV1 current has maximum value of 400mA.

Pulse skipping

The PFWM Switching Control Logic block operates in different modes depending on the output load current level. At light load, the V_{DD} voltage is around 4.75V. The energy delivered by each switching cycle (with minimum on time of 500ns) to the output causes V_{DD} to increase slightly above 4.75V. The FPWM Switching Control Logic block is able to detect this condition and prevents the IC from switching until V_{DD} is below 4.75V again. This results in a pulse-skipping action with fixed pulse width and varying frequency, and low power consumption because the switching frequency is reduced.Typical system standby power

Current limit adjustment



Driver output configurations

The IC's proprietary driver arrangement allows the current limit to be easily adjusted between 400mA and 1.2A. To understand this, the drivers have to be utilized as linear resistive devices with typically 3.6Ω (rather than as digital output switches). The current limit can then be calculated through linear combination as shown in the front. For TO-92 package, the ME8100A are preprogrammed to 400mA current limit and the ME8100 are preprogrammed to 800mA current limit.

Short circuit hiccup

When the output is short circuited, the ME8100 enters hiccup mode operation. In this condition,the auxiliary supply voltage collapses. An on-chip detector compares DRV1 voltage during the off-time of each cycle to 6.8V. If DRV1 voltage is below 6.8V, the IC will not start the next cycle, causing both the auxiliary supply voltage and VDD to reduce further. The circuit enters startup mode when VDD drops below 3.35V. This hiccup behaviour continues until the short circuit is removed. In this behavior, the effective duty cycle is very low resulting in very low short circuit current.

To make sure that the IC enters hiccup mode easily, the transformer should be constructed so that there is close coupling between secondary and auxiliary, so that the auxiliary voltage is low when the output is short-circuited. This can be achieved with the primary/auxiliary/secondary sequencing from the bobbin.

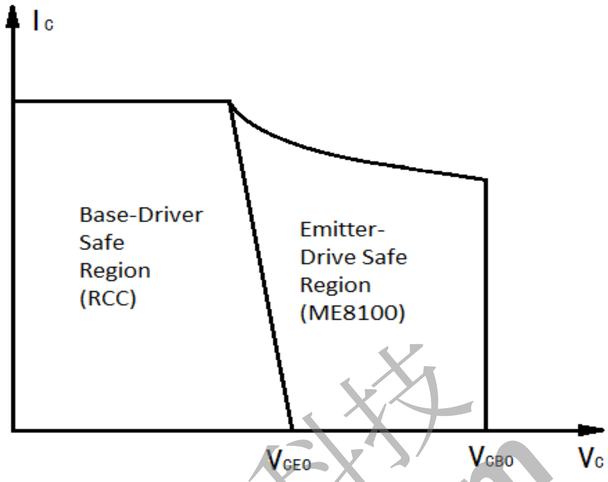
Application information

- **External power transistor**

The ME8100 allows a low-cost high voltage power NPN transistor such as 13003 or 13002 to be used safely in flyback configuration. The required collector voltage rating for VAC＝265V with full output load is at least 600V to 700V. As seen from follow map, NPN Reverse Bias Safe Operation Area, the breakdown voltage of an NPN is significantly improved when it is driven at its emitter. Thus, the ME8100+13002 or 13003 combination meet the necessary breakdown safety requirement even though RCC circuits using 13002 or 13003 do not. The follow table lists the breakdown voltage of some transistors appropriate for use with the ME8100.

Recommended Power Transistors List：

Device	V_{CBO}	V_{CEO}	I_C	h_{FEMIN}	Package
MJE13002	600V	300V	1.5A	8	TO-126
MJE13003	700V	400V	1.5A	8	TO-126
STX13003	700V	400V	1A	8	TO-92



NPN Reverse Bias Safe Operation Area

The power dissipated in the NPN transistor is equal to the collector current times the collector-emitter voltage. As a result, the transistor must always be in saturation when turned on to prevent excessive power dissipation. Select an NPN transistor with sufficiently high current gain (hFEMIN>8) and a base drive resistor low enough to ensure that the transistor easily saturates.

- **Layout considerations**

The following should be observed when doing layout for the ME8100:

1. Use a "star point" connection at the GND pin of ME8100 for the VDD bypass components (C5 and C6 in typical application), the input filter capacitor (C2 in typical application) and other ground connections on the primary side.

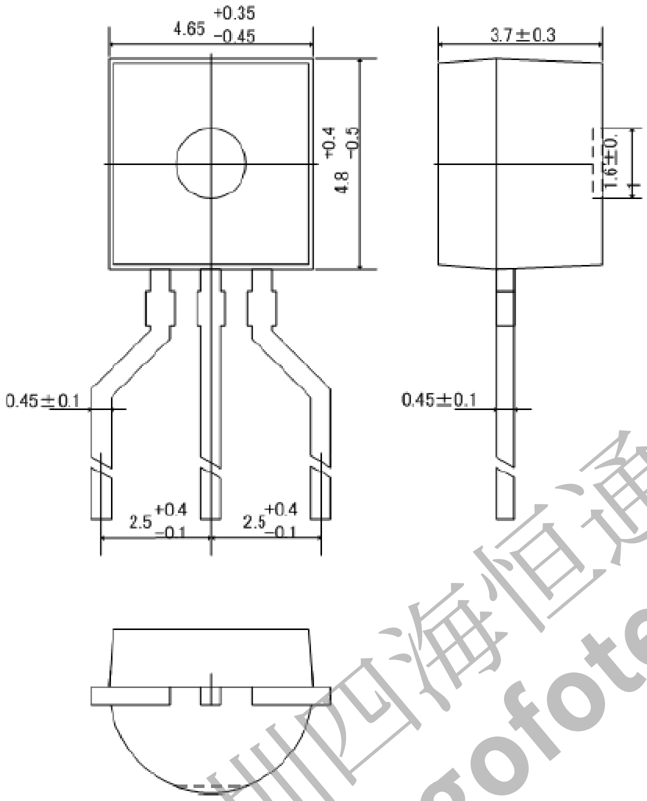
2．Keep the loop across the input filter capacitor, the transformer primary windings, and the high voltage transistor, and the ME8100 as small as possible.

3.Keep ME8100 pins and the high voltage transistor pins as short as possible.

4．Keep the loop across the secondary windings, the output diode, and the output capacitors as small as possible.

5．Allow enough copper area under the high voltage transistor, output diode, and current shunt resistor for heat sink.

TO-92



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