ALPHA & OMEGA SEMICONDUCTOR

AO4952

30V Dual Asymmetric N-Channel AlphaMOS

General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Integrated Schottky Diode (SRFET) on Low-Side
- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

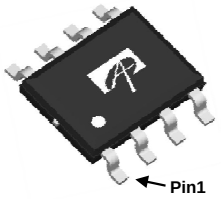
	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	11A	11A
$R_{DS(ON)}$ (at V_{GS}=10V)	<10.5mΩ	<11.5mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	<15.5mΩ	<16.5mΩ

100% UIS Tested
100% Rg Tested

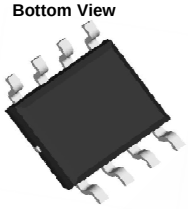
Green Product

SOIC-8

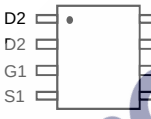
Top View



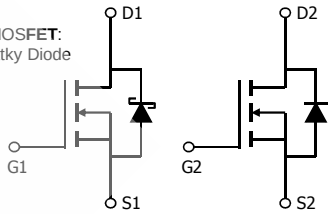
Bottom View



Top View



Q1:
SRFET™
Soft Recovery MOSFET:
Integrated Schottky Diode



Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_A=25℃	I_D	11	11	A
	T_A=70℃		9	9	
Pulsed Drain Current [C]		I_{DM}	75	74	
Avalanche Current [C]		I_{AS}	18	15	A
Avalanche Energy L=0.1mH [C]		E_{AS}	16	11	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	36	V
Power Dissipation [B]	T_C=25℃	P_D	2	2	W
	T_C=70℃		1.3	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		74	90	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JL}$	32	40	℃/W

Q1 Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.5	mA
		T_J=55℃			100	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.8	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=11A		8.3	10.5	mΩ
		T_J=125℃		11.8	15	
		V_{GS}=4.5V, I_D=9A		12.2	15.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=11A		52		S
V_{SD}	Diode Forward Voltage	I_S=0.2A,V_{GS}=0V		0.45	0.65	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		605		pF
C_{oss}	Output Capacitance			275		pF
C_{rss}	Reverse Transfer Capacitance			37		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1	2	3	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=11A		10.2	15	nC
Q_g(4.5V)	Total Gate Charge			4.9	8	nC
Q_{gs}	Gate Source Charge			2		nC
Q_{gd}	Gate Drain Charge			2.3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.36Ω, R_{GEN}=3Ω		5		ns
t_r	Turn-On Rise Time			3		ns
$t_{D(off)}$	Turn-Off DelayTime			17.5		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=11A, dI/dt=500A/µs		11		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=11A, dI/dt=500A/µs		12.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current limited by package.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

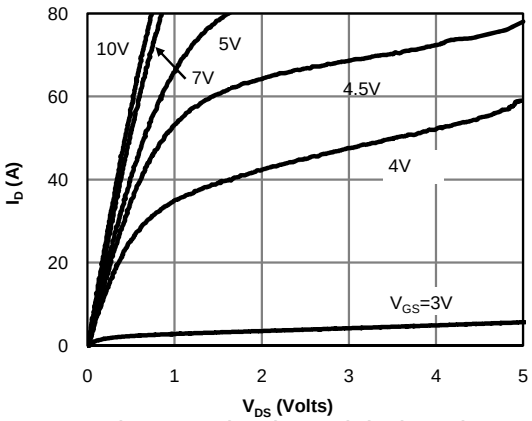


Fig 1: On-Region Characteristics (Note E)

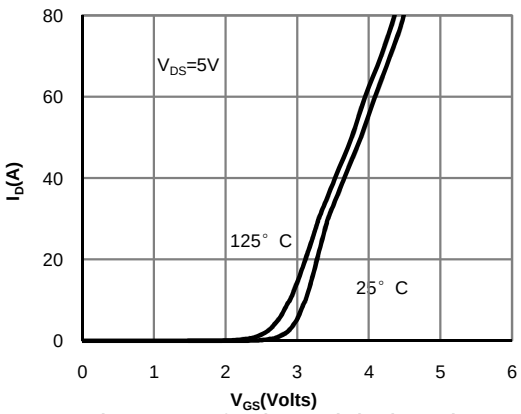


Figure 2: Transfer Characteristics (Note E)

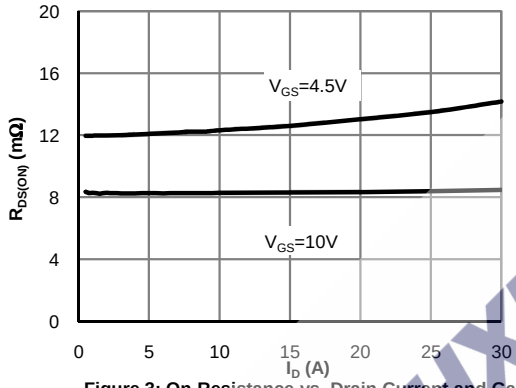


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

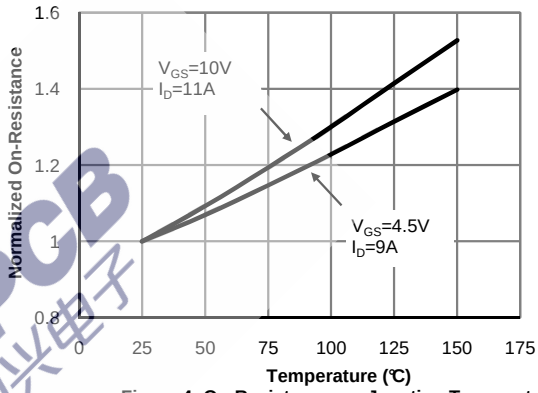


Figure 4: On-Resistance vs. Junction Temperature (Note E)

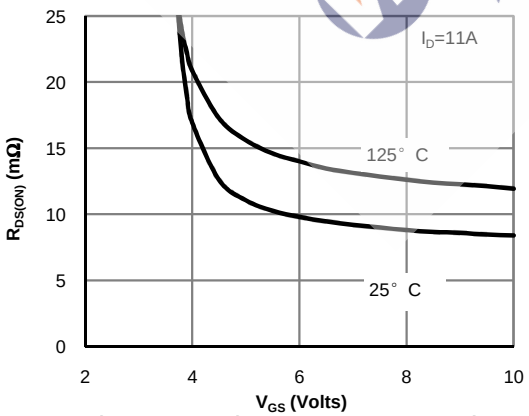


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

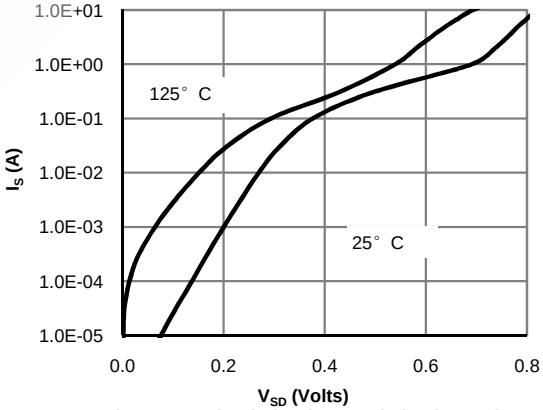


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

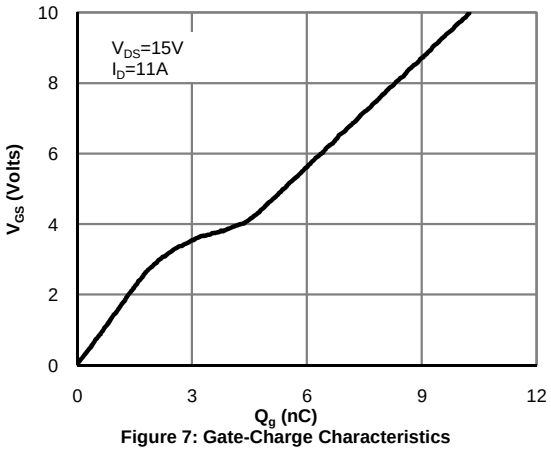


Figure 7: Gate-Charge Characteristics

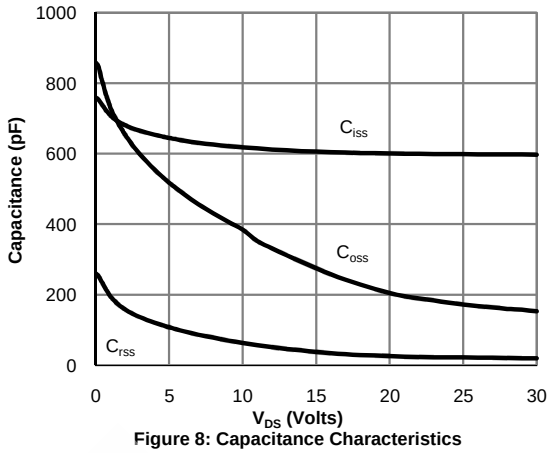
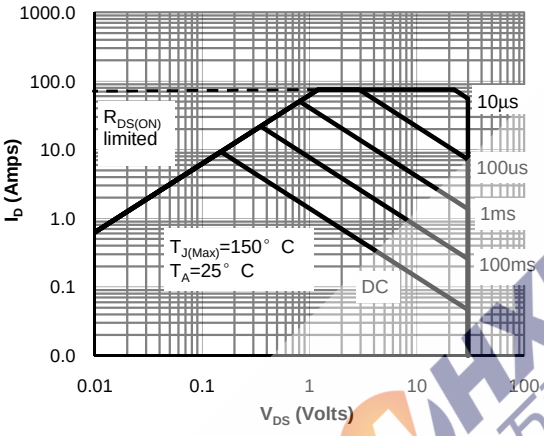


Figure 8: Capacitance Characteristics



VGS> or equal to 4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

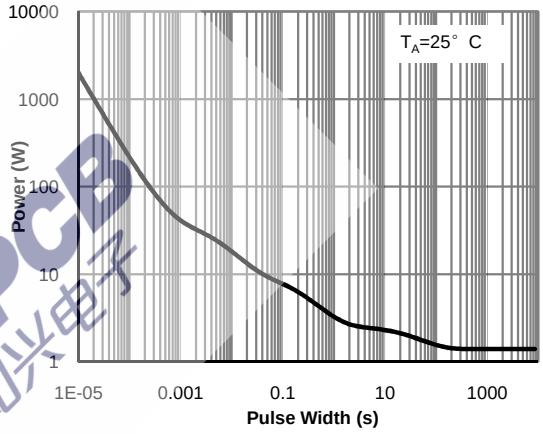


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

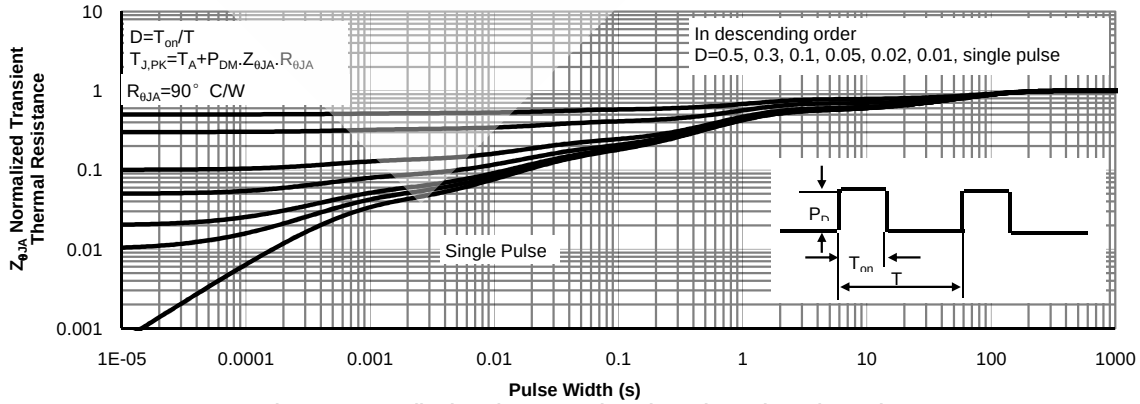


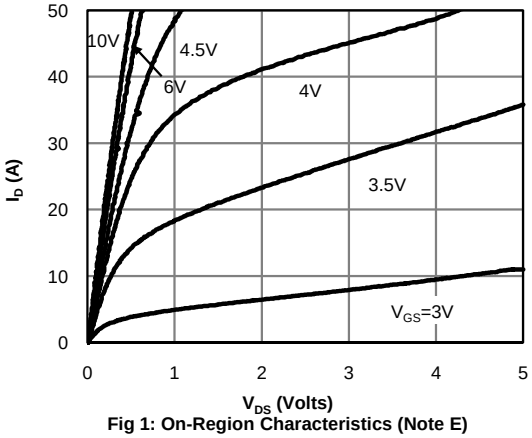
Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.8	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=11A		9	11.5	mΩ
		T_J=125℃		12.4	15.8	
		V_{GS}=4.5V, I_D=9A		12.8	16.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=11A		40		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		542		pF
C_{oss}	Output Capacitance			233		pF
C_{rss}	Reverse Transfer Capacitance			31		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1	2	3	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=11A		9	12.5	nC
Q_g(4.5V)	Total Gate Charge			4.3	6	nC
Q_{gs}	Gate Source Charge			2.2		nC
Q_{gd}	Gate Drain Charge			1.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.36Ω, R_{GEN}=3Ω		4		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			18		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=11A, dI/dt=500A/µs		9.7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=11A, dI/dt=500A/µs		11.5		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current limited by package.

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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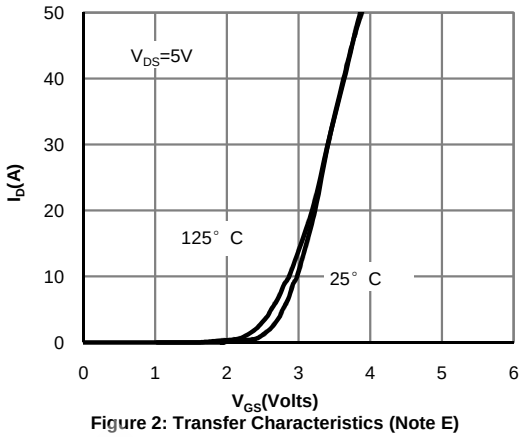


Figure 2: Transfer Characteristics (Note E)

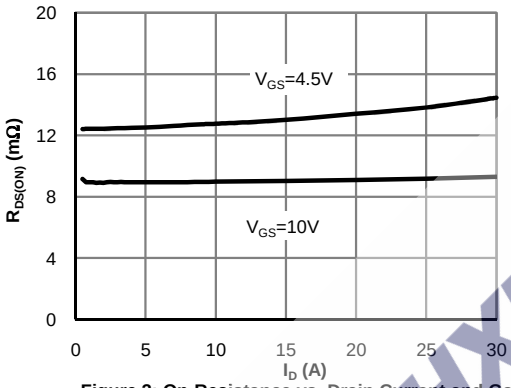
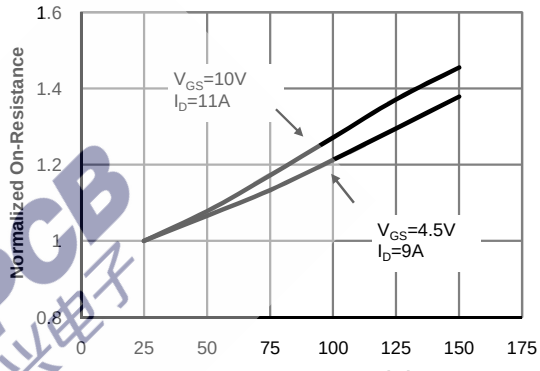


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)



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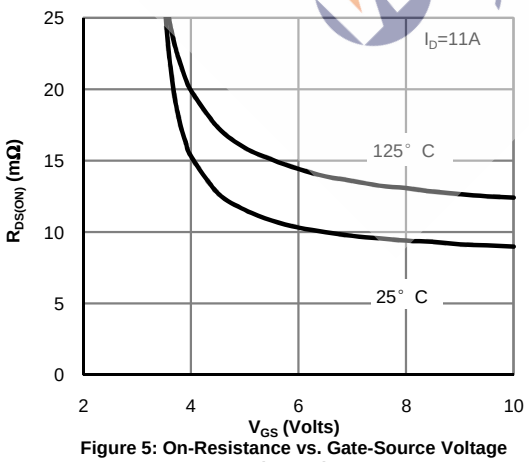

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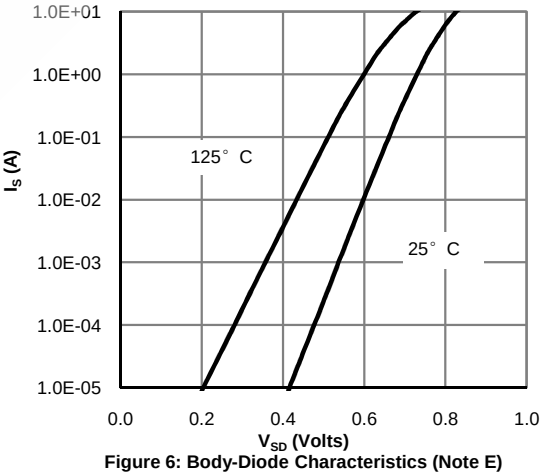
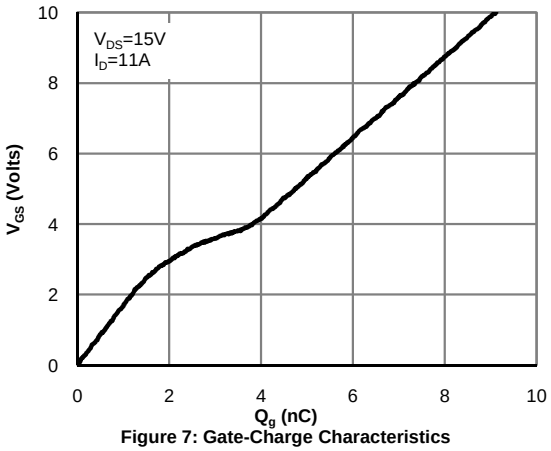


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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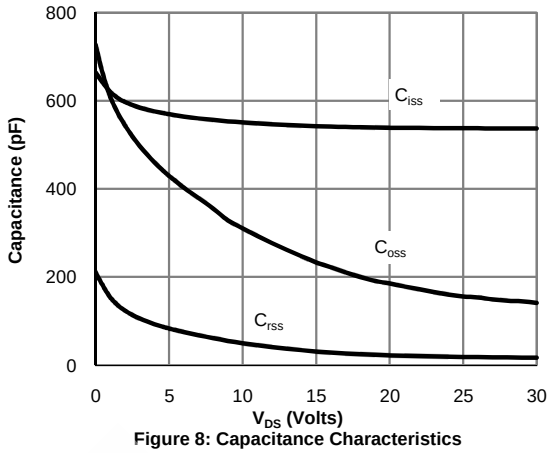

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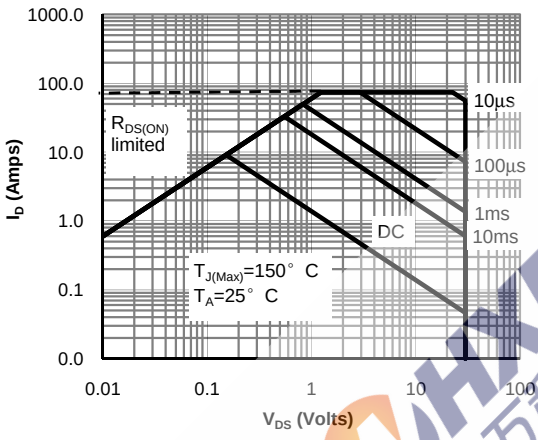

VGS> or equal to 4.5V

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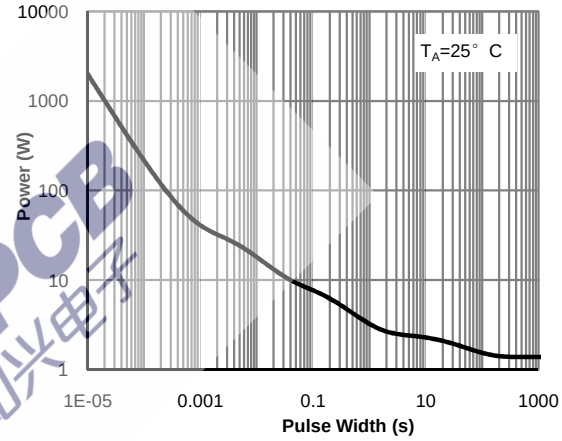

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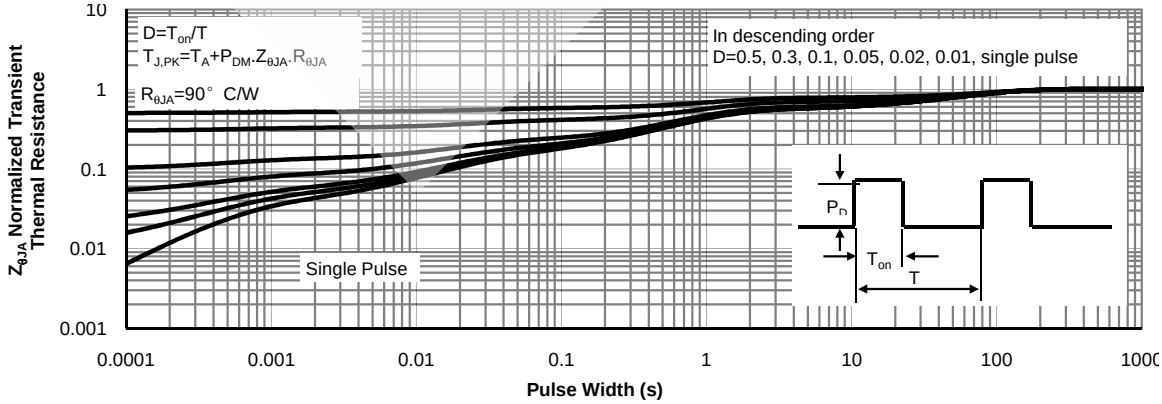
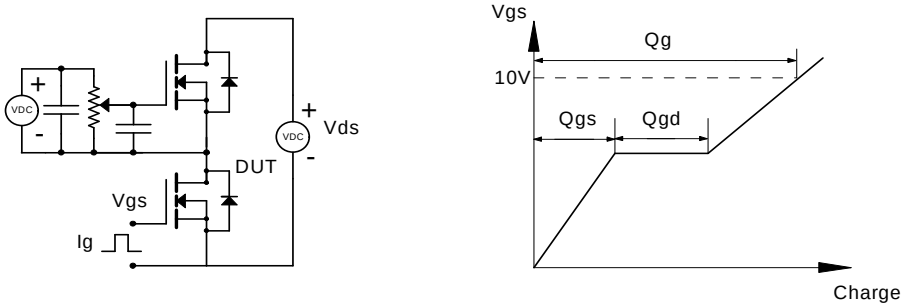
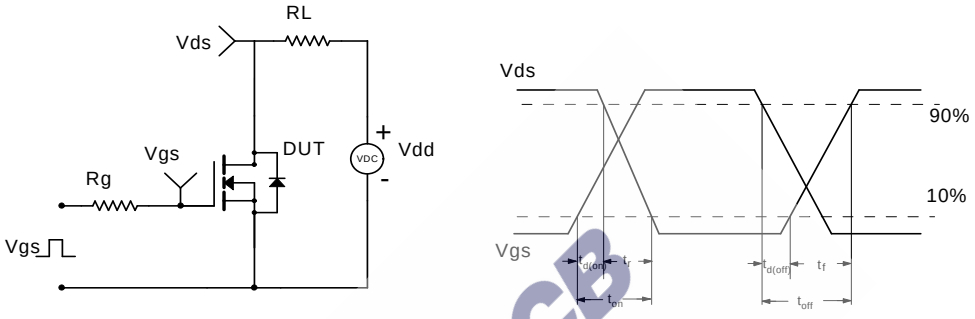


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

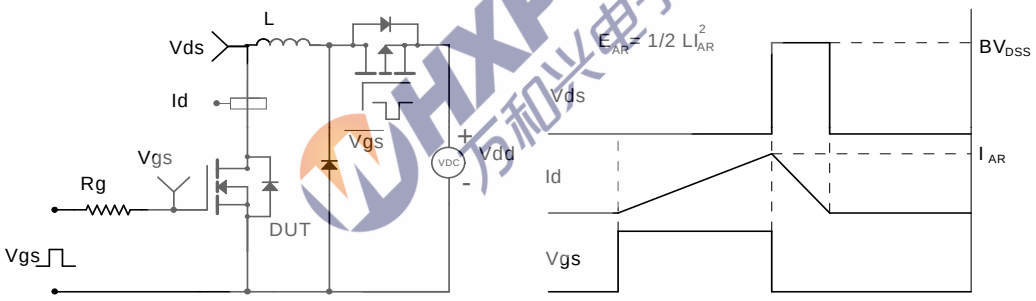
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms