Device Features

- Fully Qualified Bluetooth system
- Bluetooth v.1 and v1.2 specification compliant
- Full Speed Bluetooth operation with piconet and scatternet support
- 6Mbit on-chip flash
- Low Power 1.8V operation
- Integrated switch-mode regulator
- Integrated battery charger
- 8 x 8mm 96-ball TFBGA package
- Minimum external components
- UART port
- 15-bit Linear Audio CODEC
- 4.2V tolerant LED driver

BlueCore™3-Audio Flash

Single Chip Bluetooth® v1.2 System

Production Information Data Sheet for

BC31A223A

BC31A223B

June 2005

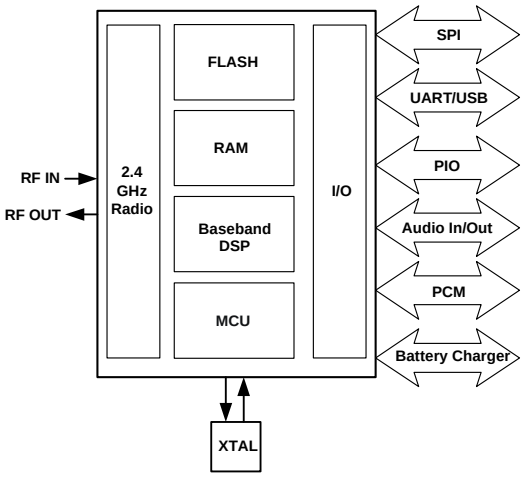
General Description

BlueCore3-Audio Flash is a single chip radio and baseband IC for Bluetooth 2.4GHz systems.

BlueCore3-Audio Flash contains 6Mbit of internal Flash memory. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v1.2 of the specification for data and voice communications.

Applications

- Headsets
- Automotive Hands-Free Kits
- General purpose Bluetooth systems requiring an on-chip audio CODEC



BlueCore3-Audio Flash System Architecture

BlueCore3-Audio Flash has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and built-in self-test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v1.2 Specification.

The battery charger has a nominal charge current of 90mA for part number BC31A223A, and 40mA for part number BC31A223B.

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Status Information

The status of this Data Sheet is **Production Information**.

Note:

Part BC31A223B is pre-production.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers on the target specification for a CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications. Production Data Sheets supersede all previous document versions.

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

1 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs available
- Bluetooth v1.2 Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class1 support using external power amplifier, with RF power controlled by an internal 8-bit DAC.

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals between 8 and 32MHz (in multiples of 250kHz) or an external clock
- Accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shut down, wake up commands with an integrated low power oscillator for ultra-low power Hold/Sniff/Park mode
- Clock request output to control an external clock
- On-chip high efficiency switch-mode regulator 1.8V output from 2.5V to 4.2V input.
- On-chip linear regulator; 1.8V output from a 2.2V to 4.2V input, can also be used to generate microphone bias
- Power-on-reset cell detects low supply voltage

Auxiliary Features (continued)

- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications
- Fully integrated battery charger for Lithium Ion/Polymer battery
- LED driver

Baseband and Software

- Internal 6Mbit Flash for complete system solution
- Internal 32Kbyte RAM, allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air

Physical Interfaces

- Synchronous peripheral interface operating up to 4M baud for system debugging
- UART interface with programmable baud rate up to 1.5M baud with an optional bypass mode
- Full speed USB v1.1 (v2.0 compatible) interface supports OHCI and UHCI host interfaces
- Optional I^2C™ compatible interface

Audio CODEC

- 15-bit resolution, 8kHz sampling frequency
- Designed for use in voice applications such as headsets and hands-free kits
- Integrated microphone amplifier and audio power amplifier

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded RFCOMM
- Customised builds with embedded application code

Package Options

- 96-ball TFBGA, 8 x 8 x 1.2mm, 0.65mm pitch

2 8 x 8mm TFBGA Package Information

2.1 BlueCore3-Audio Flash Pinout Diagram

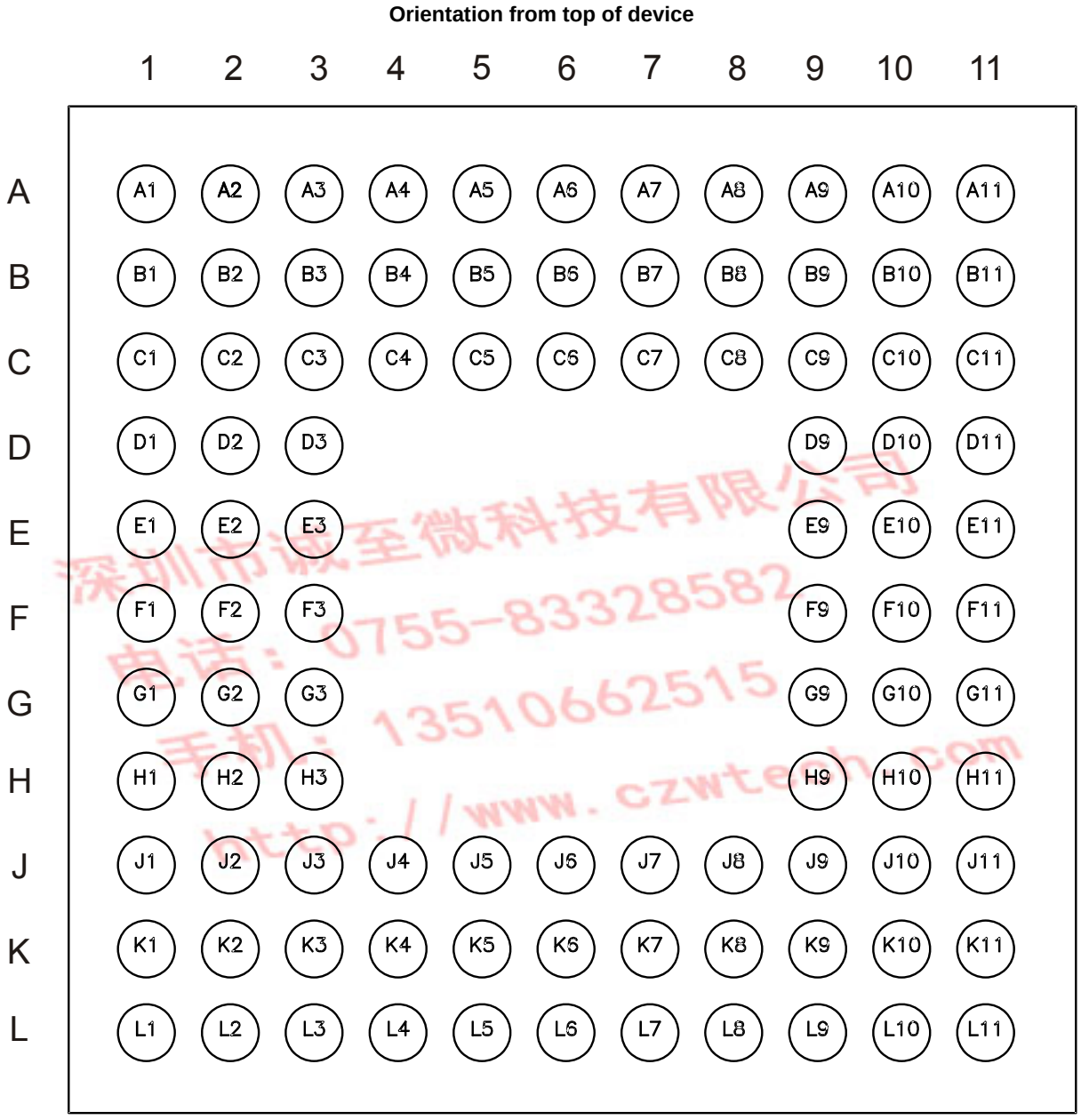


Figure 2.1: BlueCore3-Audio Flash Device Pinout

2.2 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	D1	Analogue	Single ended receiver input
PIO[0]/RXEN	A1	Bi-directional with programmable strength internal pull-up/down	Control output for external TX/RX switch (if fitted)
PIO[1]/TXEN	B2	Bi-directional with programmable strength internal pull-up/down	Control output for external PA (If fitted)
TX_A	F1	Analogue	Transmitter output/switched receiver input
TX_B	E1	Analogue	Complement of TX_A
AUX_DAC	C3	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L4	Analogue	For crystal or external clock input
XTAL_OUT	K4	Analogue	Drive for crystal

USB and UART	Ball	Pad Type	Description
UART_TX	K9	CMOS output, tri-state, with weak internal pull-up	UART data output
UART_RX	K10	CMOS input with weak internal pull-down	UART data input
UART_RTS	L8	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
UART_CTS	K11	CMOS input with weak internal pull-down	UART clear to send active low
USB_DP	L10	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	L9	Bi-directional	USB data minus

PCM Interface	Ball	Pad Type	Description
PCM_OUT	G11	CMOS output, tri-state, with weak internal pull-down	Synchronous data output
PCM_IN	J11	CMOS input, with weak internal pull-down	Synchronous data input
PCM_SYNC	H9	Bi-directional with weak internal pull-down	Synchronous data sync
PCM_CLK	H11	Bi-directional with weak internal pull-down	Synchronous data clock

PIO Port	Ball	Pad Type	Description
PIO[2]	A2	Bi-directional with programmable strength internal pull-up/down	PIO or external clock request
PIO[3]	B3	Bi-directional with programmable strength internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or clock request input from host controller
PIO[4]	F9	Bi-directional with programmable strength internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore3-Audio Flash)
PIO[5]	F10	Bi-directional with programmable strength internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[6]	F11	Bi-directional with programmable strength internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[7]	G9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line or programmable frequency clock output
PIO[8]	A5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[9]	A4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[10]	B4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
PIO[11]	A3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
AIO[0]	J6	Bi-directional	Programmable input/output line
AIO[1]	L6	Bi-directional	Programmable input/output line
AIO[2]	L7	Bi-directional	Programmable input/output line
LED[0]	A9	Open drain output	Current sink to drive LED
LED[1]	A10	Open drain output	Current sink to drive LED

Audio CODEC	Ball	Pad Type	Description
MIC_P	L2	Analogue	Microphone input positive
MIC_N	L3	Analogue	Microphone input negative
SPKR_P	J2	Analogue	Speaker output positive
SPKR_N	J1	Analogue	Speaker output negative

Test and Debug	Ball	Pad Type	Description
RESETB	D10	CMOS input, with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	B9	CMOS input with weak internal pull-up	Chip select for Synchronous Peripheral Interface active low
SPI_CLK	C11	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	C9	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B11	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	C10	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)
TEST[1]	K7	Analogue	For test purposes only (leave unconnected)
TEST[2]	J8	Analogue	For test purposes only (leave unconnected)

Power Supplies and Control	Ball	Pad Type	Description
VREG_EN	H3	CMOS input	Regulator control pin
VREG_IN	H1	Regulator input	Linear regulator input
VREG_OUT	K1	Regulator output	Linear regulator output
VDD_CHG	A11	Charger input	Lithium Ion battery charger input
BAT_P	A8	Battery terminal +	Lithium Ion battery positive terminal. Battery charger output and input to switch-mode regulator
BAT_N	A7	Battery terminal -	Lithium Ion battery negative terminal/ Ground connection for switch mode regulator
LX	A6	Switch-mode regulator output	Switch-mode power regulator output
VDD_USB	L11	VDD	Positive supply for UART/USB ports
VDD_PIO	B1	VDD	Positive supply for PIO and AUX DAC(1)
VDD_PADS	D11	VDD	Positive supply for all other digital Input/Output ports(2)
VDD_CORE	E11	VDD	Positive supply for internal digital circuitry
VDD_RADIO	C1	VDD/Regulator sense	Positive supply for RF circuitry
VDD_VCO	H2	VDD	Positive supply for local oscillator circuitry
VDD_ANA	L1, L5	VDD	Positive supply for analogue circuitry and 1.8V regulated output
VDD_MEM	B6, B8, J7, K8	VDD	Positive supply for memory. Connect to VDD_CORE to provide pin compatibility with future devices
VSS_PADS	C4, C8, D9, J9	VSS	Ground connections for input/output ports
VSS_CORE	E9	VSS	Ground connection for internal digital circuitry
VSS_RADIO	C2, D2, E2, F2	VSS	Ground connections for RF circuitry
VSS_VCO	G1, G2	VSS	Ground connections for local oscillator
VSS_ANA	J3, J4, J5, K2, K3	VSS	Ground connections for analogue circuitry
VSS_MEM	C5, C7	VSS	Ground connections for memory. Connect to provide pin compatibility with future devices
VSS	E3	VSS	Ground connection

Unconnected Terminals	Ball	Description
	B5, B7, B10, C6, D3, E10, F3, G3, G10, H10, J10, K5, K6	Leave unconnected

Notes:

(1) Positive supply for PIO[3:0] and PIO[11:6].

(2) Positive supply for SPI/PCM ports and PIO[7:4].

3 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Minimum**	**Maximum**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_MEM, VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE	-0.4V	2.2V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	-0.4V	3.7V
Supply Voltage: VREG_IN	-0.4V	5.6V
Supply Voltage: VREG_EN	-0.4V	5.6V
Supply Voltage: BAT_P	-0.4V	4.25V
Supply Voltage: VDD_CHG	-0.4V	5.75V
Other Terminal Voltages	VSS-0.4V	VDD+0.4V

Recommended Operating Conditions		
Operating Condition	**Minimum**	**Maximum**
Operating Temperature Range	-40°C	+85°C
Guaranteed RF performance range (1)	-25°C	+85°C
Supply Voltage: VDD_MEM, VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE	1.7V	1.9V
Supply Voltage: VDD_PADS, VDD_PIO and VDD_USB	1.7V	3.6V
Supply Voltage: VREG_IN	2.2V	4.2V(2)
Supply Voltage: VREG_EN	2.2V	4.2V
Supply Voltage: BAT_P	2.5V	4.25V
Supply Voltage: VDD_CHG	4.35V	5.75V

Note:

(1) Typical figures are given for RF performance between -40°C and +85°C

(2) The device will operate without damage with VREG_IN as high as 5.6V, however the RF performance is not guaranteed above 4.2V

Input/Output Terminal Characteristics				
Linear Regulator	**Minimum**	**Typical**	**Maximum**	**Unit**
Normal Operation				
Input Voltage	2.2	-	4.2[6]	V
Dropout Voltage (Iload = 70 mA)	-	-	350	mV
Output Voltage (Iload = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Output Noise[1][2]	-	-	1	mV rms
Load Regulation (Iload < 100 mA)	-	-	50	mV/A
Settling Time[1][3]	-	-	50	µs
Maximum Output Current	100	-	-	mA
Minimum Load Current	5	-	-	µA
Quiescent Current (excluding load, Iload < 1mA)	25	35	50	µA
Low Power Mode[4]				
Quiescent Current (excluding load, Iload < 100µA)	4	7	10	µA
Disabled Mode[5]				
Quiescent Current	1.5	2.5	3.5	µA

Notes:

(1) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

(2) Frequency range 100Hz to 100kHz

(3) 1mA to 70mA pulsed load

(4) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode

(5) Regulator is disabled when VREG_EN is pulled low. It can also be disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA

(6) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore3, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.2V

Input/Output Terminal Characteristics (Continued)				
Switch-mode Regulator	**Minimum**	**Typical**	**Maximum**	**Unit**
Input Voltage	2.5	-	4.2	V
Output Voltage (Iload = 70 mA)	1.70	1.78	1.85	V
Temperature Coefficient	-250	-	+250	ppm/°C
Normal Operation				
Output ripple	-	-	1	mV rms
Transient Settling Time(1)	-	-	50	µs
Maximum Load Current	100	-	-	mA
Conversion Efficiency (Iload = 70 mA)	-	90	-	%
Switching Frequency(2)	-	1.333	-	MHz
Startup Current Limit(3)	-	60	-	mA
Low Power Mode(4)				
Output Ripple	-	-	1	mV rms
Transient Settling Time(5)	-	-	700	µs
Maximum Load Current	20	-	-	mA
Minimum Load Current	0	-	-	mA
Conversion Efficiency (Iload = 1mA)	-	80	-	%
Switching Frequency(6)	50	-	150	kHz
Disabled Mode				
Quiescent Current			1	µA

Notes:

(1) 1mA to 70mA pulsed load

(2) Locked to crystal frequency

(3) Current is limited on start-up to prevent excessive stored energy in the filter inductor. The regulator will operate with reduced efficiency until the current limiter is disabled during the firmware boot-up sequence

(4) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode

(5) 100µA to 1mA pulsed load

(6) Defines minimum period between pulses. Pulses are skipped at low current loads.

Input/Output Terminal Characteristics (Continued)				
Battery Charger (BC31A223A)	**Minimum**	**Typical**	**Maximum**	**Unit**
Input Voltage	4.5	-	6.5	V
Charging Mode (BAT_P rising to 4.25V)				
Supply Current[1]	-	2	-	mA
Flat Battery Charge Current[2][9]	-	4	-	mA
Battery Trickle Charge Current[3][9]	-	10	-	mA
Battery Fast Charge Current[4][9]				
(VDD_CHG - BAT_P > 0.7V)	-	90	-	mA
(VDD_CHG - BAT_P = 0.15V)	-	30	-	mA
Trickle Charge Voltage Threshold	-	2.9	-	V
Float Voltage (with correct trim value set)[5]	4.17	4.2	4.23	V
Float Voltage trim step size[5]	-	50	-	mV
Battery Charge Termination Current[6]	-	10	-	%
Standby Mode (BAT_P falling from 4.25V)				
Supply Current[1]	-	80	-	µA
Battery Current[7]	-	-40	-	µA
Battery Recharge Hysteresis[8]	100	-	150	mV
Shutdown Mode (VDD_CHG too low)				
VDD_CHG Under-voltage Threshold	80	-	150	mV
VDD_CHG – BAT_P Lockout Threshold	3.6	-	3.7	V
Supply Current[1]	-	-	100	µA
Battery Current[7]	-1	-	0	µA
Battery Charger (BC31A223B)[10]				
Charging Mode (BAT_P rising to 4.25V)				
Flat Battery Charge Current[2][9]	-	2	-	mA
Battery Trickle Charge Current[3][9]	-	4	-	mA
Battery Fast Charge Current[4][9]				
(VDD_CHG - BAT_P > 0.7V)	-	40	-	mA
(VDD_CHG - BAT_P = 0.15V)	-	13	-	mA

Notes:

(1) Current into VDD_CHG; does not include current delivered to battery ($I_{(V\_CHG)} – I_{(BAT\_P)}$)

(2) BAT_P < 1.8V approx.

(3) 1.8V < BAT_P < Trickle charge threshold

(4) Trickle charge threshold < BAT_P < Float voltage

(5) Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

(6) Specified as a percentage of the Fast charge current

(7) Negative current is specified as flowing into the BlueCore device

(8) Hysteresis of (V_{FLOAT} – BAT_P) for charging to restart

(9) Charge current can also be modified as a customer variant of a standard BC31A223A or BC31A223B device. Fast charge current can be set to nominal values between 25mA -110mA. Trickle and Flat Battery current will be modified proportionately.

(10) With the exception of the values shown here, the values for Battery Charger (BC31A223B) are the same as those for Battery Charger (BC31A223A).

Input/Output Terminal Characteristics (Continued)					
Digital Terminals		**Minimum**	**Typical**	**Maximum**	**Unit**
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	+0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	+0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, (I_o = 4.0mA), 2.7V ≤ VDD ≤ 3.0V		-	-	0.2	V
V_{OL} output logic level low, (I_o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V		-	-	0.4	V
V_{OH} output logic level high, (I_o = -4.0mA), 2.7V ≤ VDD ≤ 3.0V		VDD-0.2	-	-	V
V_{OH} output logic level high, (I_o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V		VDD-0.4	-	-	V
Input and Tri-state Current with:					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		+10	+40	+100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		+0.2	+1.0	+5.0	µA
I/O pad leakage current		-1	0	+1	µA
C_I Input Capacitance		1.0	-	5.0	pF

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Minimum**	**Typical**	**Maximum**	**Unit**
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V
Input leakage current				
VSS_PADS < V_{IN} < VDD_USB[1]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage levels **To correctly terminated USB Cable**				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Power-on reset	**Minimum**	**Typical**	**Maximum**	**Unit**
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Input/Output Terminal Characteristics (Continued)					
Auxiliary ADC		**Minimum**	**Typical**	**Maximum**	**Unit**
Resolution		-	-	8	Bits
Input voltage range (LSB size = VDD_ANA/255)		0	-	VDD_ANA	V
Accuracy	INL	-1	-	1	LSB
(Guaranteed monotonic)	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate(2)		-	-	700	Samples/s

Auxiliary DAC	**Minimum**	**Typical**	**Maximum**	**Unit**
Resolution	-	-	8	Bits
Average output step size(3)	12.5	14.5	17.0	mV
Output Voltage		monotonic(2)		
Voltage range (I_O=0mA)	VSS_PADS	-	VDD_PIO	V
Current range	-10.0	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity(3)	-2	-	+2	LSB
Settling time (50pF load)	-	-	10	µs

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Minimum**	**Typical**	**Maximum**	**Unit**
Crystal frequency(4)	8.0	-	32.0	MHz
Digital trim range(5)	5.0	6.2	8.0	pF
Trim step size(5)	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance(6)	870	1500	2400	Ω
External Clock	**Minimum**	**Typical**	**Maximum**	**Unit**
Input frequency(7)	7.5	-	40.0	MHz
Clock input level(8)	0.2	-	VDD_ANA	V pk-pk
Allowable jitter	-	-	15	ps rms
XTAL_IN input impedance	-	-	-	kΩ
XTAL_IN input capacitance	-	7	-	pF

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_USB are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled

(2) Access of ADC is through VM function and therefore sample rate given is achieved as part of this function

(3) Specified for an output voltage between 0.2V and VDD_PIO -0.2V

(4) Integer multiple of 250kHz

(5) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim

(6) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF

(7) Clock input can be any frequency between 8 and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz

(8) Clock input can either be sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA a DC blocking capacitor is required between the signal and XTAL_IN

Input/Output Terminal Characteristics (Continued)				
Audio CODEC, 15Bit Resolution	**Minimum**	**Typical**	**Maximum**	**Unit**
Microphone Amplifier				
Input full scale at maximum gain	-	3	-	mV rms
Input full scale at minimum gain	-	350	-	mV rms
Gain resolution (1)	2.8	3	3.2	dB
Distortion at 1kHz	-	-	-78	dB
Input referenced rms noise (2)	-	5	-	μV rms
Bandwidth	-	20	-	kHz
Mic mode input impedance	-	20	-	kΩ
Input mode input impedance	-	130	-	kΩ
Analog to Digital Converter				
Input sample rate (3)	-	1	-	MSamples/s
Output sample rate (4)	-	8	-	KSamples/s
Distortion and noise at 1kHz (relative to full scale)	-	-78	-75	dB
Digital to Analog Converter				
Gain Resolution	2.8	3	3.2	dB
Min Gain (5)	-	-18	-	dB
Max Gain (5)	-	+3	-	dB
Loudspeaker Driver				
Output voltage full scale swing (differential)	-	2.0	-	V Pk-Pk
Output current drive (at full scale swing) (6)	10	20	40	mA
Output full scale current (at reduced swing) (7)	-	75	-	mA
Output –3dB bandwidth	-	18.5	-	kHz
Distortion and noise (relative to full scale) (32Ωload	-	-75	-	dB
Allowed Load: resistive	8(8)	-	OC	Ω
Allowed Load: capacitive	-	-	500	pF

Note:

(1) 42dB range of gain control (under software control)

(2) Noise in bandwidth from 100Hz to 4kHz gain setting >17dB

(3) Single bit, 2nd order Σ–Δ ADC clocked at 1MHz

(4) This is the decimated and filtered output at 15-bit resolution

(5) 21dB gain range (under software control)

(6) Output for 0.1% THD, signal level of 2V Pk-Pk

(7) Output for 1%THD, Signal level of 1V Pk-Pk

(8) Output swing reduced to 1.2V Pk-Pk differential with 1%THD or 0.5V Pk-Pk differential with 0.1%THD

3.1 Power Consumption

Typical Average Current Consumption		
VDD=1.8V Temperature = +20°C Output Power = +4dBm		
Mode	**Average**	**Unit**
SCO connection HV3 (30ms interval Sniff Mode) (Slave)	19.6	mA
SCO connection HV3 (30ms interval Sniff Mode) (Master)	20.1	mA
SCO connection HV3 (No Sniff Mode) (Slave)	24.2	mA
SCO connection HV1 (Slave)	37.4	mA
SCO connection HV1 (Master)	37.6	mA
ACL data transfer 115.2kbps UART no traffic (Master)	7.9	mA
ACL data transfer 115.2kbps UART no traffic (Slave)	17.1	mA
ACL data transfer 921kbps UART (Master)	27.7	mA
ACL data transfer 921kbps UART (Slave)	30.9	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART (Master)	2.16	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART (Slave)	1.92	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART (Master)	0.33	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART (Slave)	0.35	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.28	mA
Standby Mode (Connected to host, no RF activity)	0.10	mA
Reset (RESETB low)	57	µA
CODEC		
Microphone inputs and ADC	0.85	mA
DAC and loudspeaker driver, no signal[1]	1.4	mA

Note:

(1) Increase is <+5% for maximum signal

Typical Peak Current at 20°C	
Device Activity/State	**Current (mA)**
Peak Current during cold boot (100ms sampling interval)	-
Peak TX Current Average across burst)	-
Peak RX Current	-
Average RX Current across burst	-

Conditions	**-**
REG_IN, VDD_PIO, VDD_PADS	-
Host Interface	-
Baud Rate	-
Clock Source	-
Output Power	-
Receive Sensitivity	-
Device Mode	-
Packet Type	-

4 Radio Characteristics

BlueCore3 Audio Flash meets the Bluetooth specification v2.0 when used in a suitable application circuit between -40°C and +85°C. TX output is guaranteed to be unconditionally stable over the guaranteed temperature range.

4.1 Temperature +20°C

4.1.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +20°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power[1][2]	-	4.5	-	-6 to +4[3]	dBm
Variation in RF power over temperature range with compensation enabled (±)[4]	-	0.5	-	-	dB
Variation in RF power over temperature range with compensation disabled (±)[4]	-	3	-	-	dB
RF power control range	-	35	-	≥16	dB
RF power range control resolution [5]	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0$ ±2MHz[6][7]	-	-40	-	≤-20	dBm
Adjacent channel transmit power $F=F_0$ ±3MHz[6][7]	-	-45	-	≤-40	dBm
Adjacent channel transmit power $F=F_0$>±3MHz[6][7]	-	<-50	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	164	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	146	-	≥115	kHz
Δf2avg / Δf1avg	-	0.95	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50µs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	9	-	≤40	kHz
2nd Harmonic content	-	-70	-	≤30	dBm
3rd Harmonic content	-	-50	-	≤30	dBm

Note

(1) BlueCore3 Audio Flash firmware maintains the transmit power to be within the Bluetooth specification v2.0 limits.

(2) Measurement made using a PSKEY_LC_MAX_TX_POWER setting corresponds to a PSKEY_LC_POWER_TABLE power table entry of 63.

(3) Class 2 RF transmit power range, Bluetooth specification v2.0.

(4) To some extent these parameters are dependent on the matching circuit used, and its behaviour over temperature. Therefore these parameters may be beyond CSR’s direct control.

(5) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for TX Level >20.

(6) Measured at F_0 = 2441MHz.

(7) Up to three exceptions are allowed in v2.0 of the Bluetooth specification. BlueCore3 Audio Flash is guaranteed to meet the ACP performance as specified by the Bluetooth specification v2.0.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Emitted power in cellular bands measured at the unbalanced port of the balun. Output power =4.5dBm	0.869 – 0.894[1]	-	-125	-	GSM 850	dBm/Hz
	0.869 – 0.894[2]	-	-128	-	CDMA 850	
	0.925 – 0.960[1]	-	-128	-	GSM 900	
	1.570 – 1.580[3]	-	-133	-	GPS	
	1.805 – 1.880[1]	-	-132	-	GSM 1800 / DCS 1800	
	1.930 – 1.990[4]	-	-131	-	PCS 1900	
	1.930 – 1.990[1]	-	-130	-	GSM 1900	
	1.930 – 1.990[2]	-	-132	-	CDMA 1900	
	2.110 – 2.170[2]	-	-130	-	W-CDMA 2000	
	2.110 – 2.170[5]	-	-134	-	W-CDMA 2000	

Notes:

(1) Integrated in 200kHz bandwidth and then normalised to a 1Hz bandwidth.

(2) Integrated in 1.2MHz bandwidth and then normalised to a 1Hz bandwidth.

(3) Integrated in 1MHz bandwidth. and then normalised to a 1Hz bandwidth.

(4) Integrated in 30kHz bandwidth and then normalised to a 1Hz bandwidth.

(5) Integrated in 5MHz bandwidth and then normalised to a 1Hz bandwidth.

4.1.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-85.0	-82.0	≤-70	dBm
	2.441	-	-85.5	-82.5		
	2.480	-	-84.5	-81.5		
Maximum received signal at 0.1% BER		-20	>10	10	≥-20	dBm
	Frequency (MHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Continuous power required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the	30 – 2000	-	-	-	-10	dBm
	2000 – 2400	-	-	-	-27	
	2500 – 3000	-	-	-	-27	
C/I co-channel		-	6	-	≤11	dB
Adjacent channel selectivity C/I $F=F_0+1MHz$ (1) (2)		-	-5	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0-1MHz$ (1) (2)		-	-4	-	≤0	dB
Adjacent channel selectivity C/I $F=F_0+2MHz$ (1) (2)		-	-35	-	≤-30	dB
Adjacent channel selectivity C/I $F=F_0-2MHz$ (1) (2)		-	-22	-	≤-20	dB
Adjacent channel selectivity C/I $F\geq F_0+3MHz$ (1) (2)		-	-42	-	≤-40	dB
Adjacent channel selectivity C/I $F\leq F_0-5MHz$ (1) (2)		-	-40	-	≤-40	dB
Adjacent channel selectivity C/I $F=F_{Image}$ (1) (2)		-	-22	-	≤-9	dB
Maximum level of intermodulation interferers (3)		-	-	-	≥-39	dBm
Spurious output level (4)		-	-150	-	-	dBm/Hz

Notes:

(1) Up to five exceptions are allowed in v2.0 of the Bluetooth specification. BlueCore3 Audio Flash is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.0.

(2) Measured at F_0 = 2441MHz

(3) Measured at f1-f2 = 5MHz. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c, i.e., wanted signal at -64dBm

(4) Measured at the unbalanced port of the balun. Integrated in 100kHz bandwidth, then normalised to 1Hz. Actual figure is typically below -150dBm/Hz except for peaks of -100dBm at 0.8GHz, -80dBm at 1600MHz, -65dBm inband at 2.4GHz and -85dBm at 3.2GHz.

Radio Characteristics VDD = 1.8V Temperature = +20°C (Continued)						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Cellular Band**	**Unit**
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -67dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	-	-	GSM 850	dBm
	0.824 – 0.849	-	-	-	CDMA	
	0.880 – 0.915	-	-	-	GSM 900	
	1.710 – 1.785	-	-	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	-	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-	-	CDMA 1900	
	1.920 – 1.980	-	-	-	W-CDMA 2000	
Continuous power in cellular bands required to block Bluetooth reception (for sensitivity of -72dBm with 0.1% BER) measured at the unbalanced port of the balun.	0.824 – 0.849	-	-	-	GSM 850	dBm
	0.824 – 0.849	-	-	-	CDMA	
	0.880 – 0.915	-	-	-	GSM 900	
	1.710 – 1.785	-	-	-	GSM 1800 / DCS 1800	
	1.850 – 1.910	-	-	-	GSM 1900 / PCS 1900	
	1.850 – 1.910	-	-	-	CDMA 1900	
	1.920 – 1.980	-	-	-	W-CDMA 2000	

4.2 Temperature -40°C

4.2.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -40°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	5.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-42	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-46	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	164	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	144	-	115	kHz
Δf2avg / Δf1avg	-	0.94	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50μs
Drift (single slot packet)	-	9	-	≤25	kHz
Drift (five slot packet)	-	11	-	≤40	kHz

Notes:

(1) BlueCore3 Audio Flash firmware maintains the transmit power to be within the Bluetooth specification v2.0 limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0.

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0 of the Bluetooth specification

4.2.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -40°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-87.0	-	≤-70	dBm
	2.441	-	-87.5	-		
	2.480	-	-86.5	-		
Maximum received signal at 0.1% BER		-20	>10	-	≥-20	dBm

4.3 Temperature -25°C

4.3.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = -25°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	5.2	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	790	-	≤1000	kHz
Adjacent channel transmit power $F=F_0 \pm 2MHz$(3) (4)	-	-42	-	≤-20	dBm
Adjacent channel transmit power $F=F_0 \pm 3MHz$(3) (4)	-	-45	-	≤-40	dBm
Δf1avg “Maximum Modulation”	-	164	-	$140<\Delta f1_{avg}<175$	kHz
Δf2max “Minimum Modulation”	-	145	-	115	kHz
Δf2avg / Δf1avg	-	0.95	-	≥0.80	-
Initial carrier frequency tolerance	-	6	-	±75	kHz
Drift Rate	-	7	-	≤20	kHz/50μs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore3 Audio Flash firmware maintains the transmit power to be within the Bluetooth specification v2.0 limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0.

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0 of the Bluetooth specification

4.3.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = -25°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-86.5	-	≤-70	dBm
	2.441	-	-87.0	-		
	2.480	-	-86.0	-		
Maximum received signal at 0.1% BER		-	10	-	≥-20	dBm

4.4 Temperature +85°C

4.4.1 Transmitter

Radio Characteristics VDD = 1.8V Temperature = +85°C					
	Min	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Maximum RF transmit power(1)	-	2.5	-	-6 to +4(2)	dBm
RF power control range	-	35	-	≥16	dB
RF power range control resolution	-	0.5	-	-	dB
20dB bandwidth for modulated carrier	-	780	-	≤1000	kHz
Adjacent channel transmit power F=F_0 ±2MHz(3) (4)	-	-42	-	≤-20	dBm
Adjacent channel transmit power F=F_0 ±3MHz(3) (4)	-	-48	-	≤-40	dBm
Δf1avg "Maximum Modulation"	-	164	-	140<$\Delta f1_{avg}$<175	kHz
Δf2max "Minimum Modulation"	-	140	-	≥115	kHz
Δf2avg / Δf1avg	-	0.92	-	≥0.80	-
Initial carrier frequency tolerance	-	8	-	±75	kHz
Drift Rate	-	8	-	≤20	kHz/50μs
Drift (single slot packet)	-	8	-	≤25	kHz
Drift (five slot packet)	-	10	-	≤40	kHz

Notes:

(1) BlueCore3 Audio Flash firmware maintains the transmit power to be within the Bluetooth specification v2.0 limits

(2) Class 2 RF transmit power range, Bluetooth specification v2.0

(3) Measured at F_0 = 2441MHz

(4) Up to three exceptions are allowed in v2.0 of the Bluetooth specification

4.4.2 Receiver

Radio Characteristics VDD = 1.8V Temperature = +85°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER for all packet types	2.402	-	-83.0	-	≤-70	dBm
	2.441	-	-83.0	-		
	2.480	-	-83.0	-		
Maximum received signal at 0.1% BER		-	10	-	≥-20	dBm

5 Device Diagram

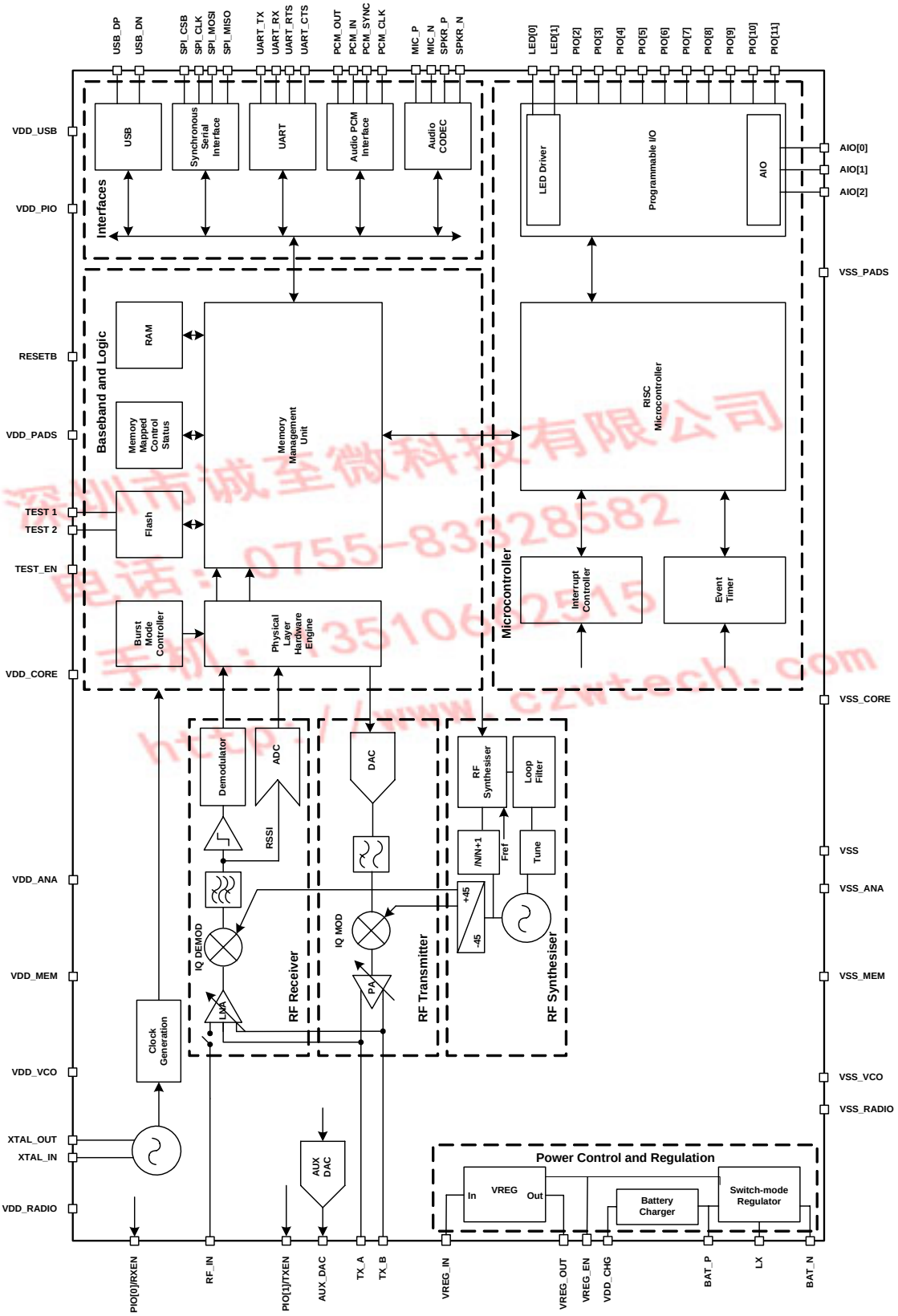


Figure 5.1: BlueCore3-Audio Flash Device Diagram

6 Description of Functional Blocks

6.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated on to the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore3-Audio Flash to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

6.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

6.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

6.2 RF Transmitter

6.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

6.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm allowing BlueCore3-Audio Flash to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

6.2.3 Auxiliary DAC

An 8-bit voltage Auxiliary DAC is provided for power control of an external PA for Class 1 operation.

6.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth specification v1.2.

6.4 Power Control and Regulation

6.4.1 Switch-Mode Regulator

BlueCore3-Audio Flash contains a high efficiency step-down switch mode 1.8V regulator, which can be used to power the complete chip from a single Lithium Ion battery (or other external voltage source). The circuit requires only two external passive filter components and has an internal PID feedback for very low supply ripple.

6.4.2 Linear Regulator

As an alternative, BlueCore3-Audio Flash also contains a 1.8V linear regulator which can be used to power the complete chip. This is less efficient than the switch-mode regulator, but requires less space for external components and can run at lower input voltages.

6.4.3 Integrated Battery Charger Circuit

BlueCore3-Audio Flash contains a fully integrated battery charger circuit, suitable for charging a Lithium Ion/Polymer battery. The circuit requires no external components.

Important Notes:

Protection Module

Lithium Ion/Polymer batteries are capable of delivering high currents of several amperes when short-circuited. This can damage connecting wires, and Printed Circuit Board (PCB) components. More seriously, pressure can build up in the cell envelope, causing it to explode and injure the user.

CSR strongly suggests that Lithium Ion/Polymer batteries incorporate an integral protection module. This is typically a small Integrated Circuit (IC) and Field Effect Transistor (FET) interposed between the battery body and its connecting wires. The protection module limits the short circuit current. Good modules will also prevent over-charge and over-discharge, which can also cause damage to the battery.

Additional Precautions

CSR also suggests that the following additional precautions are observed:

- The Direct Current (DC) inlet socket used on the appliance should be of a proprietary design, preventing users from attaching the charger or supply connector for another appliance (e.g. a mobile phone or laptop computer). The use of popular 2.1mm and 2.5mm DC jack sockets must be avoided for this reason.
- Include a voltage limiting circuit (clamp) on the charger inlet. Remember that this circuit could be exposed to voltages as high as 30V (of either polarity) if a laptop computer power supply has been connected. Include a small fuse in series with the DC inlet, but prior to the clamp.
- Never bring the Lithium Ion/Polymer battery connections directly to charging pins on the outside of the appliance casing, where they could be short-circuited by keys in the user's pocket, for example.

Temperature Extremes

Some Lithium Ion/Polymer cells can be damaged by charging at temperature extremes (e.g. below 0°C or above 50°C). Consult the battery manufacturer for guidance.

For more information, see the CSR document Lithium Ion/Polymer Battery Safety Information Note.

6.5 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8 and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

6.6 Baseband and Logic

6.6.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data which is in transit between the host and the air or vice versa. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

6.6.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped

registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

6.6.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

6.6.4 RAM

32Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

6.6.5 Flash Memory

6Mbits of internal Flash is available on the BC31A223A. The Flash memory is provided for system firmware and the DSP co-processor code implementation. There are three pads for testing the Flash memory, these should not be connected.

6.6.6 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore3-Audio Flash acts as a USB peripheral, responding to requests from a Master host controller such as a PC.

6.6.7 Synchronous Peripheral Interface

This is a synchronous serial port interface (SPI) for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory.

6.6.8 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

6.7 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

6.7.1 Programmable I/O

BlueCore3-Audio Flash has a total of 16 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

6.7.2 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded voice data over Bluetooth. It also contains support for PCM master CODECs that require an external system clock. The interface shares the same pins as the digital audio interface.

6.7.3 Audio CODEC

BlueCore3-Audio Flash has a 15-bit Audio CODEC that has a 8kHz sampling frequency. This has been designed for use in voice applications such as headsets and hands-free kits. The CODEC has integrated input/output amplifiers capable of driving a microphone and speaker with minimum external components.

6.7.4 LED Driver

Two 4.2V tolerant LED output pads are provided to control LED indicators. The pads are open drain pull-downs, controlled by firmware running on the device. LED[0] is also hard wired to indicate battery charging.

7 CSR Bluetooth Software Stacks

BlueCore3-Audio Flash is supplied with Bluetooth v1.2 stack firmware, which runs on the internal RISC microcontroller.

The BlueCore3-Audio Flash software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

7.1 BlueCore HCI Stack

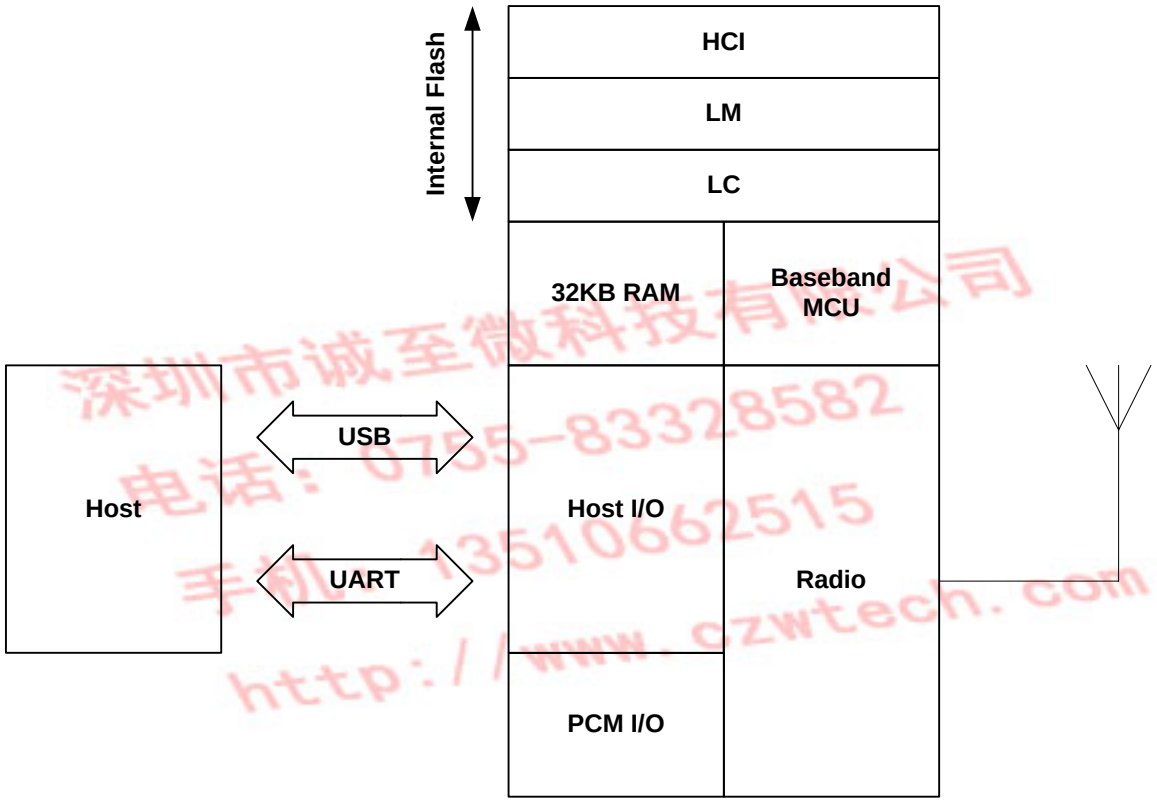


Figure 7.1: BlueCore HCI Stack

In the implementation shown in Figure 7.1 the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

7.1.1 Key Features of the HCI Stack - Standard Bluetooth Functionality

New Bluetooth v1.2 Mandatory Functionality:

- Adaptive frequency hopping (AFH), including Packet Loss Rate (PLR) and RSSI classification.
- Faster connections
- Flow and flush timeout
- LMP improvements
- Parameter ranges

Optional v1.2 functionality supported:

- Extended SCO (eSCO), eV3, eV4 and eV5
- Quality of Service and SCO handle
- L2CAP flow and error control
- Synchronisation

The firmware has been written against the Bluetooth Core Specification v1.2.

- Bluetooth components:
- Baseband (including LC)
- LM
- HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, up to 723.2kbps asymmetric(1)
- Operation with up to 7 active slaves(1)
- Operation as slave to one master while master of several slaves (Scatternet “2.0”)
- Page and Inquiry scanning while slave and master (Scatternet “2.5”)
- Maximum number of simultaneous active ACL connections: 7(2)
- Maximum number of simultaneous active SCO connections: 3(2)
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding
- Standard operating modes: page, inquiry, page-scan and inquiry-scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including “Forced Hold”
- Dynamic control of peers’ transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth Test Modes
- Standard firmware upgrade via USB (DFU)

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from http://www.csr.com.

Note:

(1) Maximum allowed by Bluetooth specification v1.2

(2) BlueCore3-Audio Flash supports all combinations of active ACL and SCO channels for both Master and Slave operation, as specified by the Bluetooth specification v1.2

7.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP) – a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set (called BCCMD – "BlueCore Command"), provides:
  - Access to the chip's general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware's random number generator
- Controls to set the default and maximum transmit powers – these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Radio transmitter enable/disable – a simple command connects to a dedicated hardware switch that determines whether the radio can transmit
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART "break" condition can be used in three ways:

1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
3. With BCSP, the firmware can be configured to send a break to the host before sending data – normally used to wake the host from a Deep Sleep state

- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of "radio test" or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and "RFCOMM builds" (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three audio channels can be routed over the chip's single PCM port (at the same time as routing any remaining audio channels over HCI) and eSCO audio.

7.2 BlueCore RFCOMM Stack

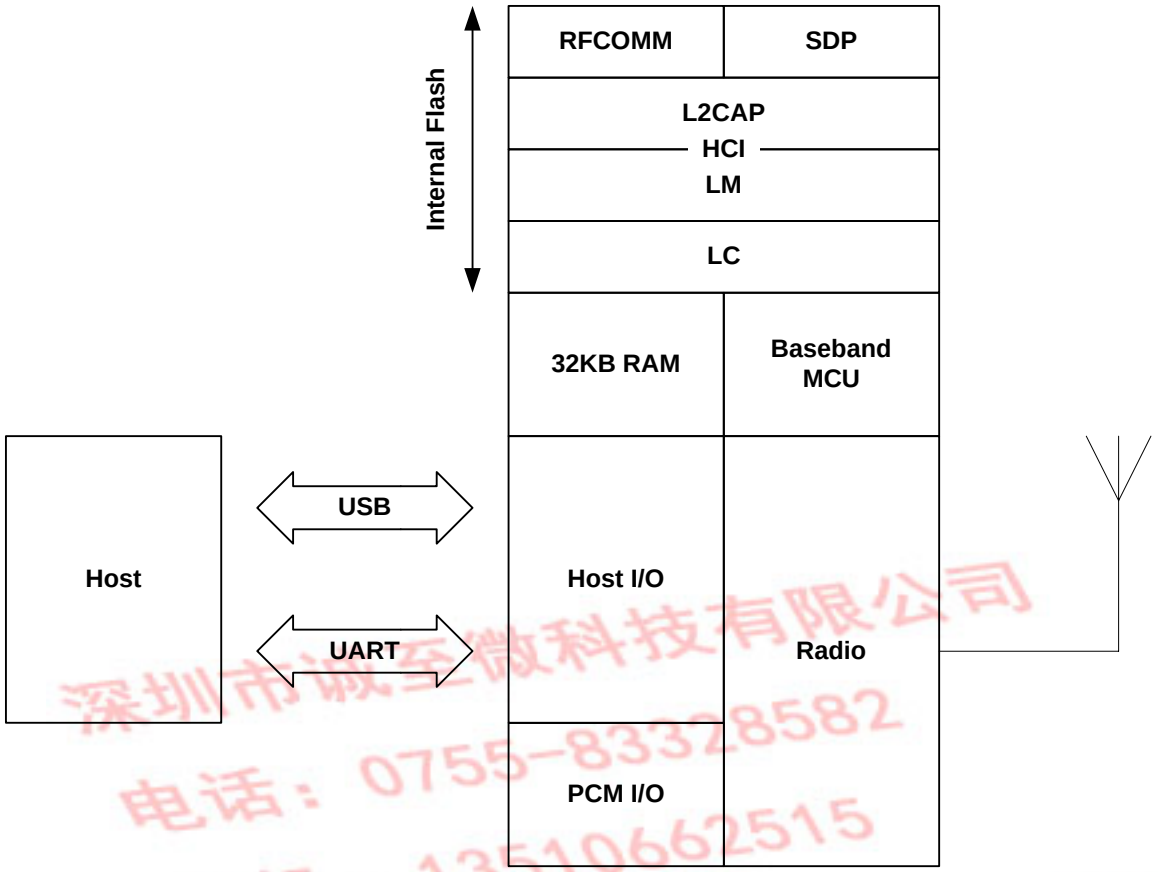


Figure 7.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 7.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

7.2.1 Key Features of the BlueCore3-Audio Flash RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: 3
- Maximum number of simultaneous active ACL connections: 3
- Maximum number of simultaneous active SCO connections: 3
- Data Rate: up to 350 Kbps

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

7.3 BlueCore Virtual Machine Stack

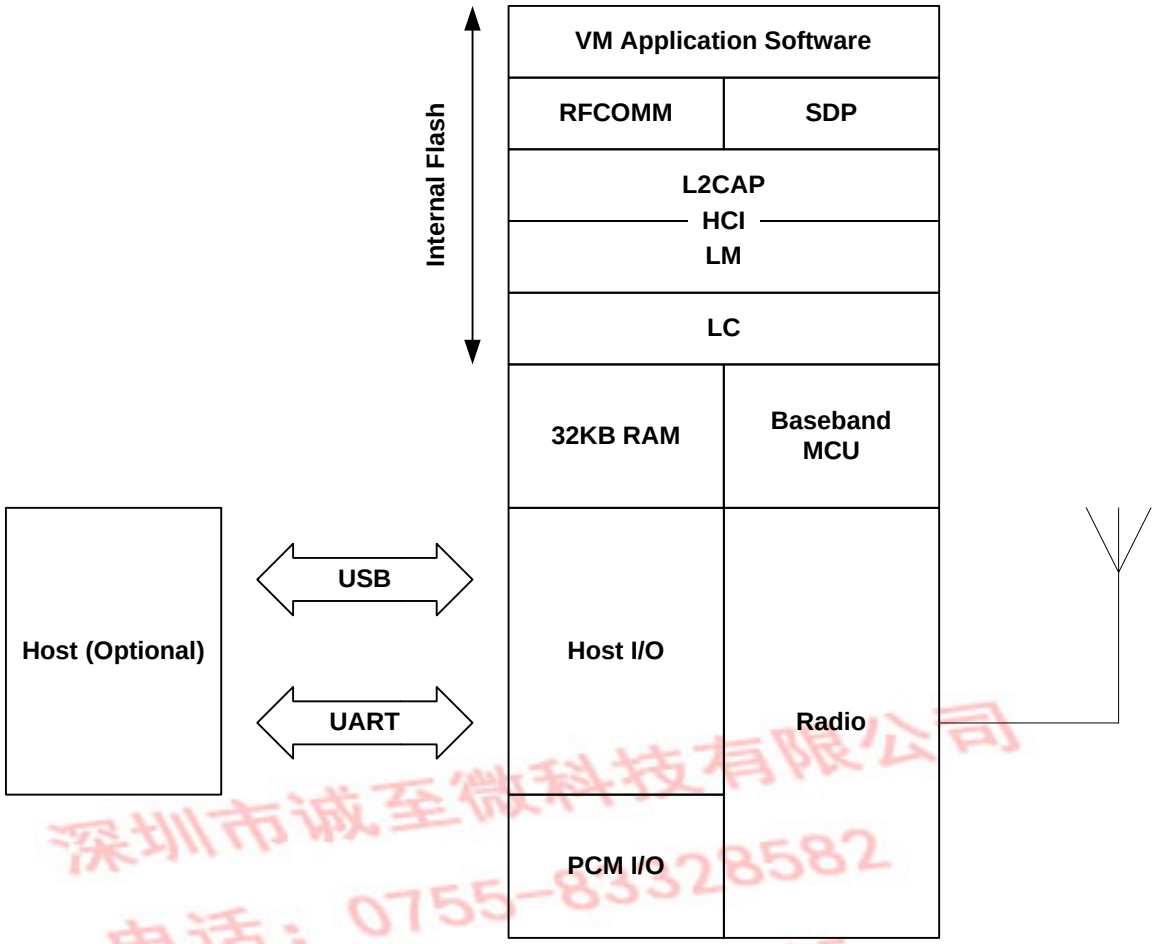


Figure 7.3: Virtual Machine

In Figure 7.3, this version of the stack firmware shown requires no host processor (but can use a host processor for debugging etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab™ software development kit (SDK) supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless headset or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the headset profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

7.4 Host-Side Software

BlueCore3-Audio Flash can be ordered with companion host-side software:

- BlueCore3-PC includes software for a full Windows®98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.
- BlueCore3-Mobile includes software for a full host-side stack designed for modern ARM based mobile handsets together with IC hardware described in this document.

7.5 Device Firmware Upgrade

BlueCore3-Audio Flash is supplied with boot loader software, which implements a Device Firmware Upgrade (DFU) capability. This allows new firmware to be uploaded to the Flash memory through BlueCore3-Audio Flash UART or USB ports.

7.6 BlueCore HID Stack

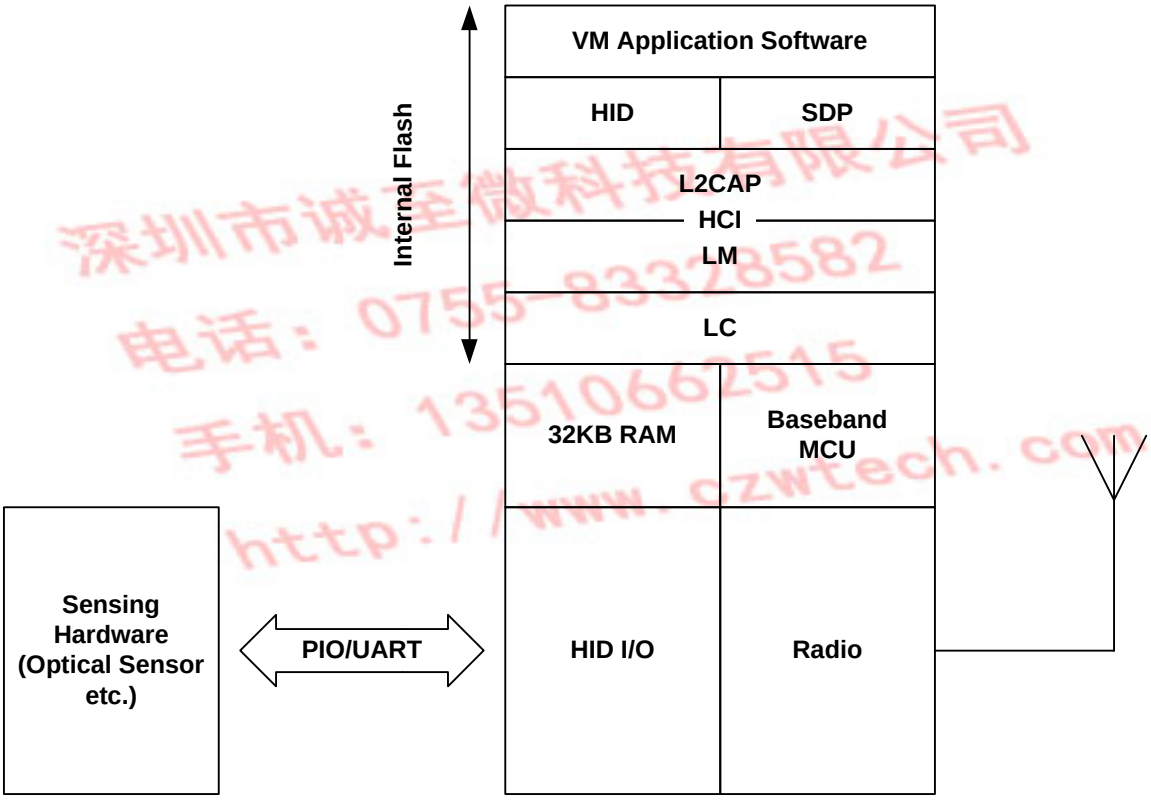


Figure 7.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional software development kit (SDK) supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include 5 mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

7.7 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application e.g. a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains 3 elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). With BCHS also come example applications in ANSI C, which makes the process of writing the application easier.

7.8 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore3-Audio Flash, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

7.9 CSR Development Systems

CSR's BlueLab and Casira development kits are available to allow the evaluation of the BlueCore3-Audio Flash hardware and software, and as toolkits for developing on-chip and host software.

8 Device Terminal Descriptions

8.1 RF Ports

The BlueCore3-Audio Flash RF_IN terminal can be configured as either a single ended or differential input. The operational mode is determined by the setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x20).

8.1.1 TX_A and TX_B

TX_A and TX_B form a complementary balanced pair. On transmit, their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive, their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip side), the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

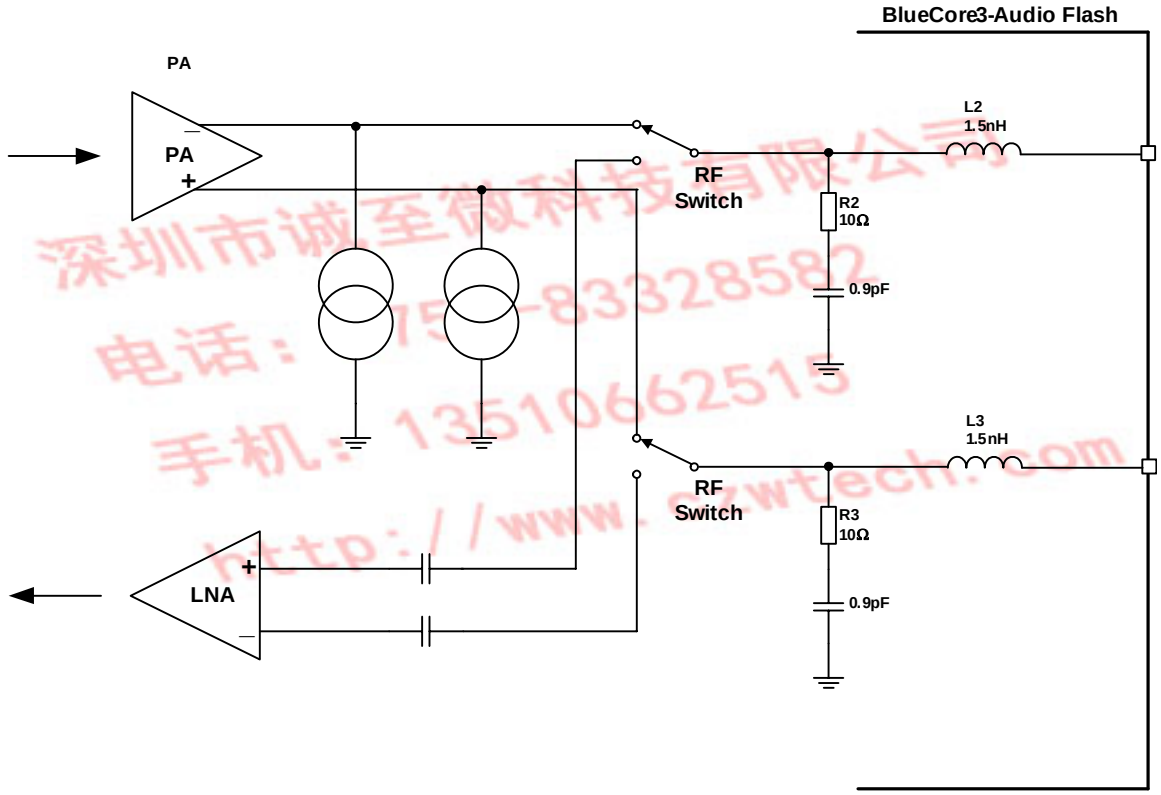


Figure 8.1: Circuit TX/RX_A and TX/RX_B

Note:

Both terminals must be externally DC biased to VDD_RADIO.

8.1.2 Single-Ended Input (RF_IN)

This is the single ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

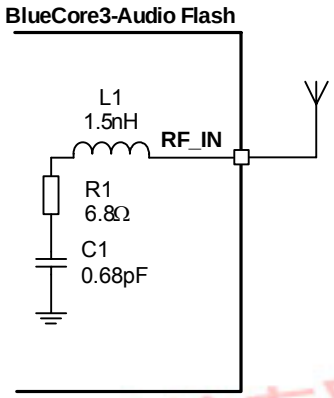


Figure 8.2: Circuit RF_IN

8.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. The output voltage is given by:

$$V_{DAC} = \mathrm{MIN}\left(\left(3.3v \times \frac{\mathrm{CNTRL\_WORD}}{255}\right), (\mathrm{VDD\_PIO} - 0.3v)\right)$$

Equation 8.1: Output Voltage with Load Current ≤ 10mA

for a load current ≤10mA (sourced from the device).

or

$$V_{DAC} = \mathrm{MIN}\left(\left(3.3v \times \frac{\mathrm{CNTRL\_WORD}}{255}\right), \mathrm{VDD\_PIO}\right)$$

Equation 8.2: Output Voltage with No Load Current

for no load current.

BlueCore3-Audio Flash enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.

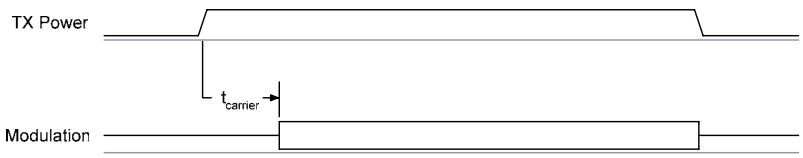


Figure 8.3: Internal Power Ramping

The Persistent Store Key (PS Key) PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits[15:8] define a delay, $t_{carrier}$, (in units of μs) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

8.1.4 Control of External RF Components

A PS Key TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as indicated in Table 8.1.

TXRX_PIO_CONTROL Value	AUX_DAC Use
0	PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 8.1: TXRX_PIO_CONTROL Values

8.2 External Reference Clock Input (XTAL_IN)

The BlueCore3-Audio Flash RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore3-Audio Flash XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in Section 8.3.

8.2.1 External Mode

BlueCore3-Audio Flash can be configured to accept an external reference clock (from another device, such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN. A square wave reference clock gives superior noise immunity as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 9.5:

	Min	Typ	Max
Frequency(1)	7.5MHz	16MHz	40MHz
Duty cycle	20:80	50:50	80:20
Edge Jitter (At Zero Crossing)	-	-	15ps rms
Signal Level	400mV pk-pk	-	VDD_ANA(2)(3)

Table 8.2: External Clock Specifications

Notes:

(1) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(2) VDD_ANA is 1.8V nominal

(3) If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk

8.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

8.2.3 Clock Timing Accuracy

As Figure 8.4 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v1.2 specification. Radio activity may occur after 11ms, therefore at this point, the timing accuracy of the external clock source must be within 20ppm.

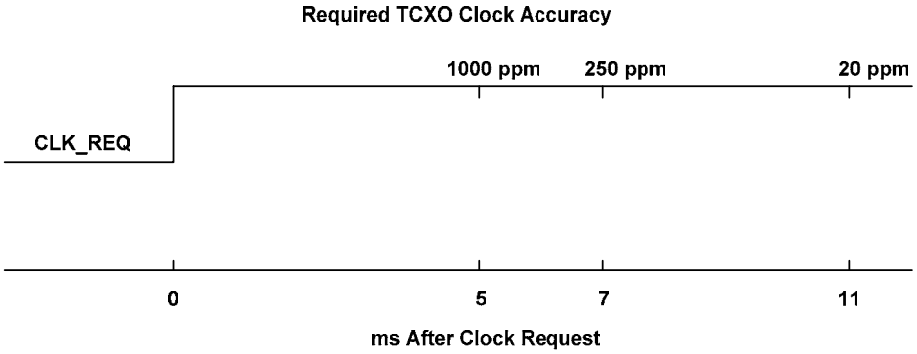


Figure 8.4: TCXO Clock Accuracy

8.2.4 Clock Start-Up Delay

BlueCore3-Audio Flash hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore3-Audio Flash firmware provides a software function which will extend the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 5-31ms.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore3-Audio Flash as low as possible. BlueCore3-Audio Flash will consume about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

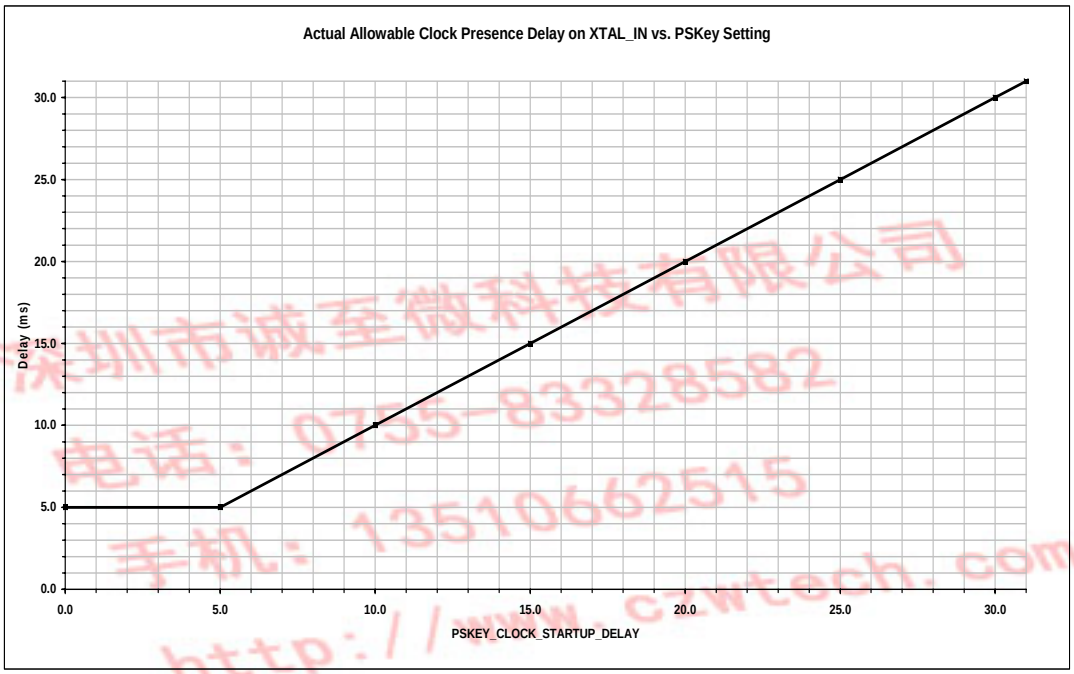


Figure 8.5: Actual Allowable Clock Presence Delay on XTAL_IN vs. PS Key Setting

8.2.5 Input Frequencies and PS Key Settings

BlueCore3-Audio Flash should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250KHz. The input frequency default setting in BlueCore3-Audio Flash is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. This is accomplished by also changing PSKEY PLLX_FREQ_REF (0xabc).

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz)
7.68	7680
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 250kHz	-
+26.00 Default	26000

Table 8.3: PS Key Values for CDMA/3G Phone TCXO Frequencies

8.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

The BlueCore3-Audio Flash RF local oscillator and internal digital clocks are derived from the reference clock at the BlueCore3-Audio Flash XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The external reference clock mode is described in Section 8.1.

8.3.1 XTAL Mode

BlueCore3-Audio Flash contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

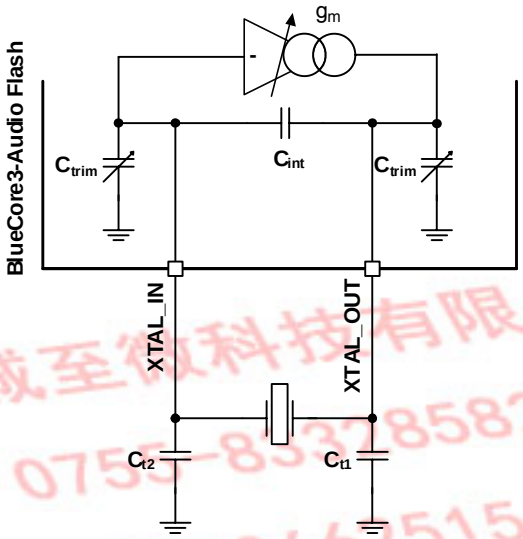


Figure 8.6: Crystal Driver Circuit

Figure 8.7 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

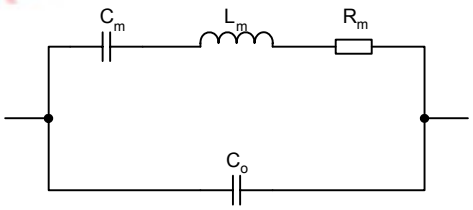


Figure 8.7: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore3-Audio Flash contains variable internal capacitors to provide a fine trim.

	Min	Typ	Max
Frequency	8MHz	16MHz	32MHz
Initial Tolerance	-	±25ppm	-
Pullability	-	±20ppm/pF	-

Table 8.4: Crystal Specification

The BlueCore3-Audio Flash driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

8.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore3-Audio Flash provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN, to which all on-chip clocks are referred. Crystal load capacitance, C_l is calculated with the following equation:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Equation 8.3: Load Capacitance

Where:

Ctrim = 3.4pF nominal (Mid range setting)

C_{int} = 1.5pF

Note:

C_{int} does not include the crystal internal self capacitance, it is the driver self capacitance

8.3.3 Frequency Trim

BlueCore3-Audio Flash enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110\ \text{fF} \times \text{PSKEY\_ANA\_FTRIM}$$

Equation 8.4: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 8.5:

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 55 \times 10^{-3} (\text{ppm/LSB})$$

Equation 8.5: Frequency Trim

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 8.6:

$$\frac{\partial(F_x)}{\partial(C)} = F_x \cdot \frac{C_m}{4(C_l + C_0)^2}$$

Equation 8.6: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 8.7.

Note:

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

8.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore3-Audio Flash uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than 3. The transconductance required for oscillation is defined by the following relationship:

$$g_m > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{(2\pi F_x)^2 R_m((C_0+C_{int})(C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 8.7: Transconductance Required for Oscillation

BlueCore3-Audio Flash guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk–pk. The drive level is determined by the crystal driver transconductance, by setting the PS Key PSKEY_XTAL_LVL (0x241).

8.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore3-Audio Flash crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with Equation 8.8:

$$R_{neg} > \frac{3(C_{t1}+C_{trim})(C_{t2}+C_{trim})}{g_m(2\pi F_x)^2(C_0+C_{int})((C_{t1}+C_{t2}+2C_{trim})+(C_{t1}+C_{trim})(C_{t2}+C_{trim}))^2}$$

Equation 8.8: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore3-Audio Flash driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

8.3.6 Crystal PS Key Settings

See tables in Section 8.2.5.

8.3.7 Crystal Oscillator Characteristics

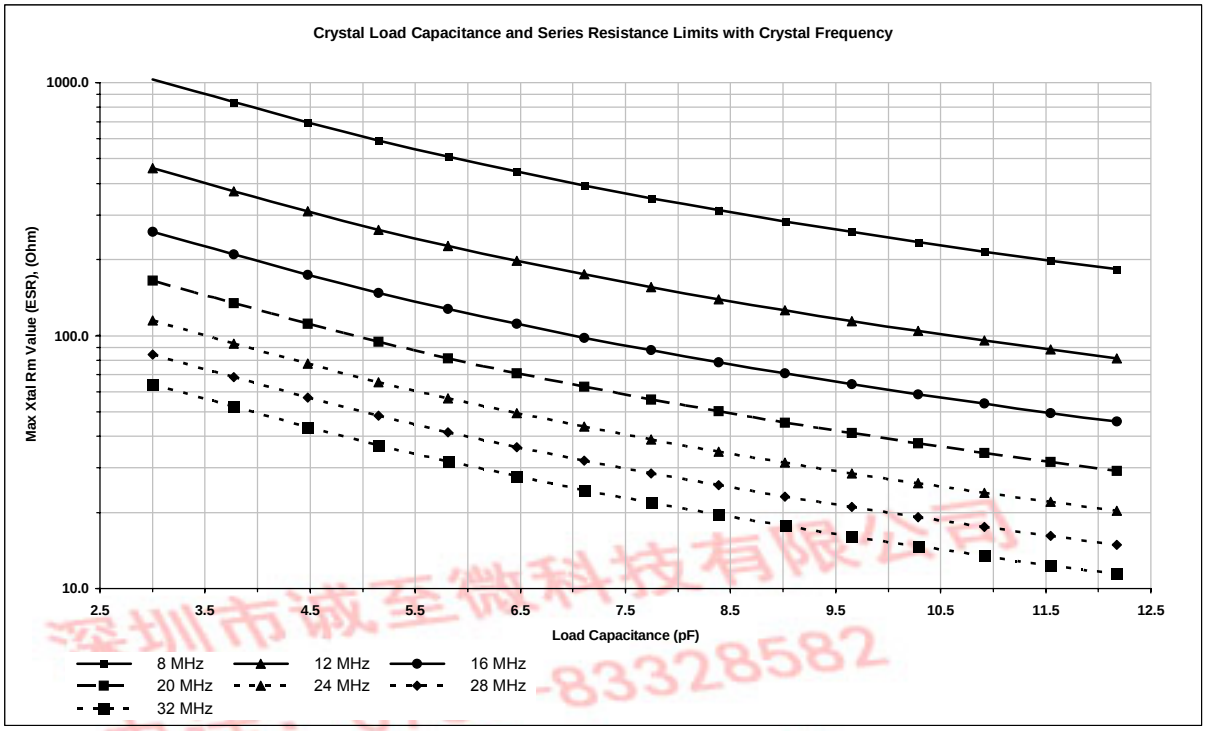


Figure 8.8: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore3-Audio Flash crystal driver at maximum drive level.

Conditions:

C_{trim} = 3.4pF centre value

Crystal C_o = 2pF

Transconductance setting = 2mA/V

Loop gain = 3

C_{t1}/C_{t2} = 3

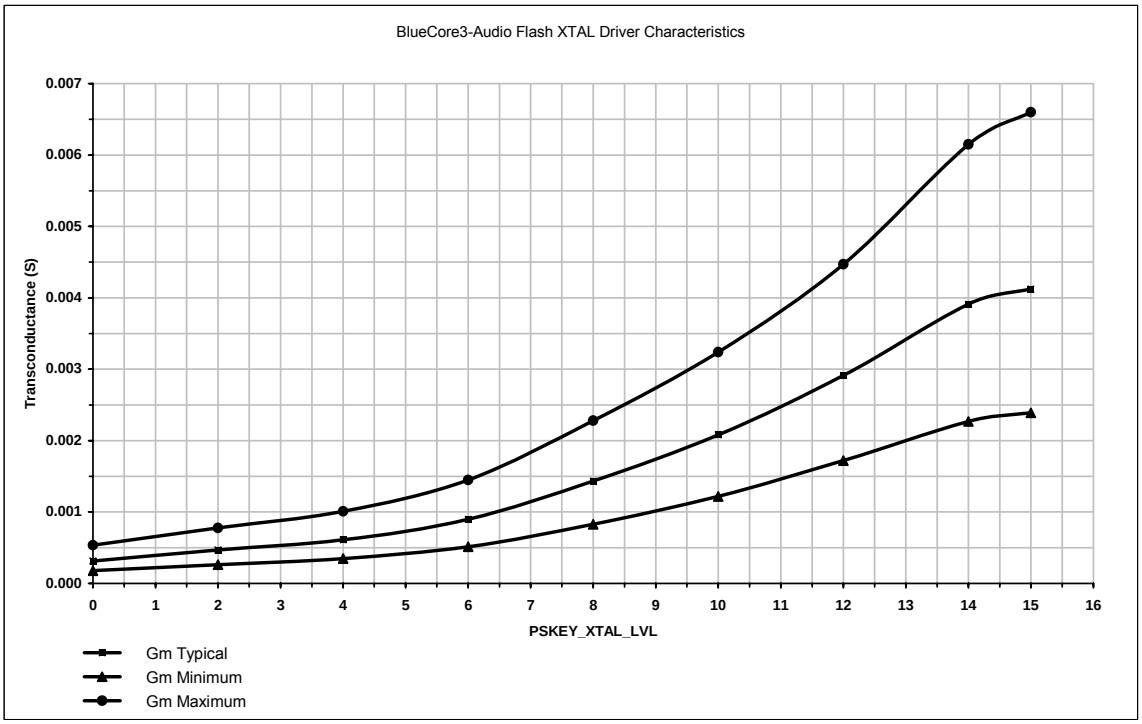


Figure 8.9: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PS Key PSKEY_XTAL_LVL (0x241).

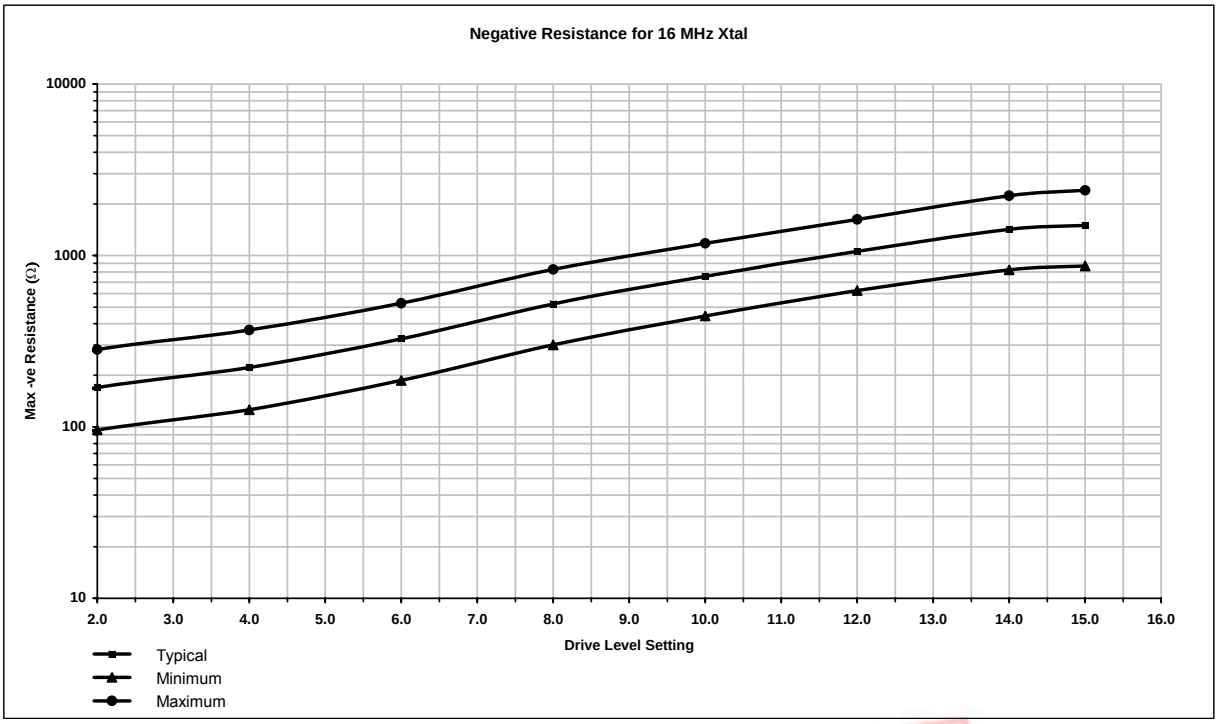


Figure 8.10: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (Please refer to your software build release note for frequencies supported);

Crystal C_0 = 0.75pF

Circuit parameters:

C_{trim} = 8pF, maximum value

C_{t1},C_{t2} = 5pF (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

8.4 UART Interface

The BlueCore3-Audio Flash Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices.(1)

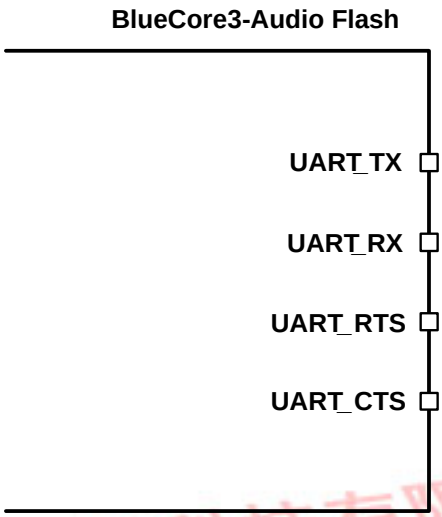


Figure 8.11: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 8.11. When BlueCore3-Audio Flash is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as baud rate and byte format, are set using BlueCore3-Audio Flash software.

Notes:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

(1) Uses RS232 protocol but voltage levels are 0V to VDD_USB, and are inverted (requires external RS232 transceiver chip)

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	1.5M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Table 8.5: Possible UART Settings

The UART interface is capable of resetting BlueCore3-Audio Flash upon reception of a break signal. A Break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 8.12. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore3-Audio Flash can emit a Break character that may be used to wake the Host.

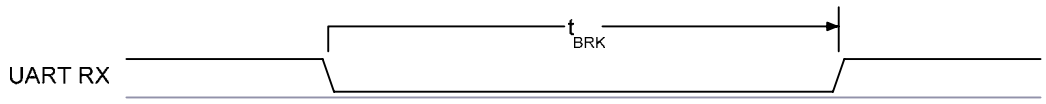


Figure 8.12: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 8.6 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 8.9.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUD\_RATE}}{0.004096}$$

Equation 8.9: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%

Table 8.6: Standard Baud Rates

8.4.1 UART Bypass

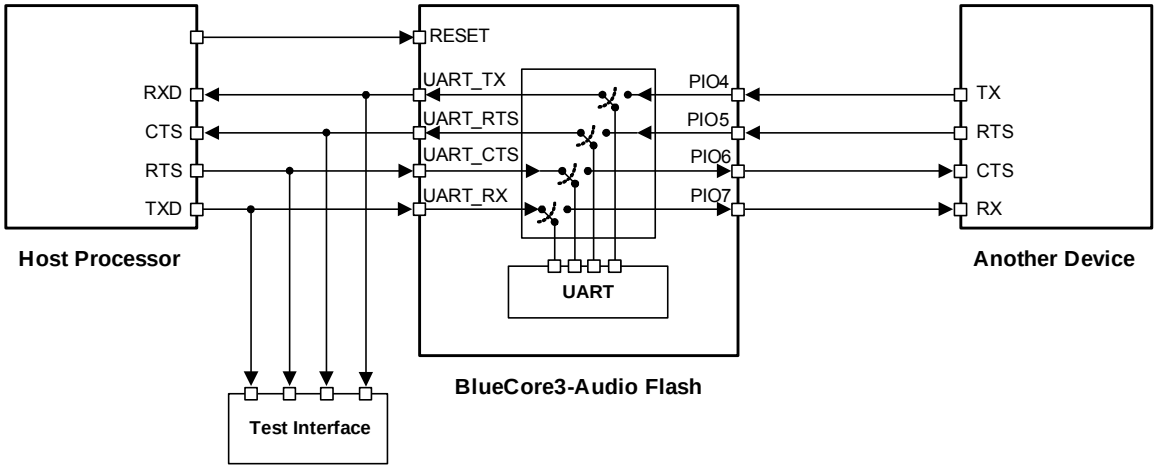


Figure 8.13: UART Bypass Architecture

8.4.2 UART Configuration While RESET is Active

The UART interface for BlueCore3-Audio Flash while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore3-Audio Flash reset is de-asserted and the firmware begins to run.

8.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore3-Audio Flash can be used. The default state of BlueCore3-Audio Flash after reset is de-asserted, this is for the host UART bus to be connected to the BlueCore3-Audio Flash UART, thereby allowing communication to BlueCore3-Audio Flash via the UART.

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore3-Audio Flash upon this, it will switch the bypass to PIO[7:4] as shown in Figure 8.13. Once the bypass mode has been invoked, BlueCore3-Audio Flash will enter the Deep Sleep state indefinitely.

In order to re-establish communication with BlueCore3-Audio Flash, the chip must be reset so that the default configuration takes affect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore it is not possible to have active Bluetooth links while operating the bypass mode.

8.4.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART Bypass Mode is equal to the values quoted for a device in standby mode.

8.5 USB Interface

BlueCore3-Audio Flash devices contain a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v1.2.

As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore3-Audio Flash only supports USB Slave operation.

8.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore3-Audio Flash and therefore have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP / USB_DN and the cable.

8.5.2 USB Pull-Up Resistor

BlueCore3-Audio Flash features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore3-Audio Flash is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with Section 7.1.5 of the USB specification v1.1. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD_PADS=3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

8.5.3 Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

8.5.4 Self Powered Mode

In self powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design for, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore3-Audio Flash via a resistor network (R_{vb1} and R_{vb2}), so BlueCore3-Audio Flash can detect when VBUS is powered up. BlueCore3-Audio Flash will not pull USB_DP high when VBUS is off.

Self powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self powered mode. The internal pull-up in BlueCore is only suitable for bus powered USB devices.

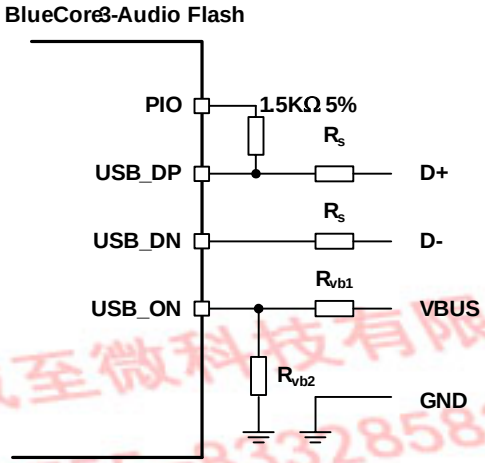


Figure 8.14: USB Connections for Self Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

8.5.5 Bus Powered Mode

In bus powered mode the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore3-Audio Flash negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus powered mode, BlueCore3-Audio Flash requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification (see USB specification v1.1, Section 7.2.4.1). Some applications may require soft start circuitry to limit inrush current if more than 10μF is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore3-Audio Flash will result in reduced receive sensitivity and a distorted RF transmit signal.

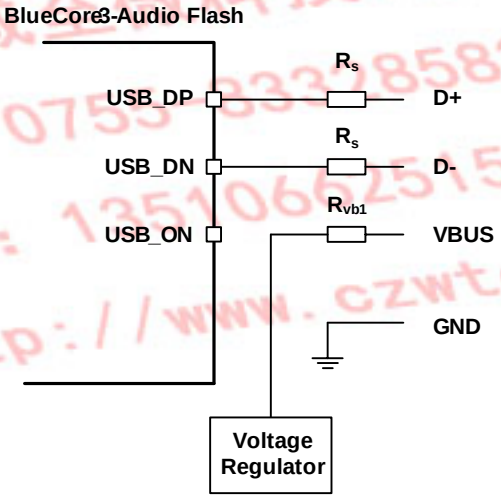


Figure 8.15: USB Connections for Bus Powered Mode

Note:

USB_ON is shared with BlueCore3-Audio Flash PIO terminals

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Table 8.7: USB Interface Component Values

8.5.6 Suspend Current

All USB devices must permit the USB host controller to place them into USB suspend mode. While in USB suspend mode, bus powered devices must not draw more than 0.5mA from USB VBUS (self powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100μA) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore3-Audio Flash. The entire circuit must be able to enter the suspend mode. (For more details on USB Suspend, see separate CSR documentation).

8.5.7 Detach and Wake_Up Signalling

BlueCore3-Audio Flash can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore3-Audio Flash into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore3-Audio Flash to put USB_DN and USB_DP in a high-impedance state and turn off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore3-Audio Flash will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable), and cannot be sent while BlueCore3-Audio Flash is effectively disconnected from the bus.

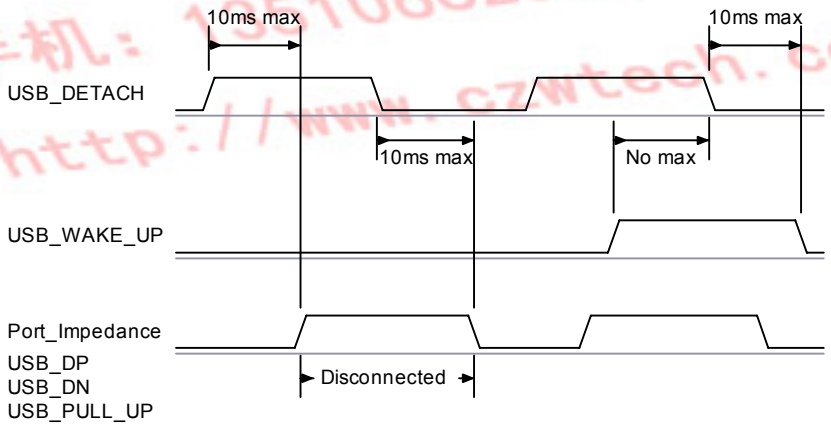


Figure 8.16: USB_DETACH and USB_WAKE_UP Signal

8.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore3-Audio Flash and Bluetooth software running on the host computer. Many PC software stacks already incorporate this driver as standard.

8.5.9 USB 1.1 Compliance

BlueCore3-Audio Flash is qualified to the USB specification v1.1, details of which are available from http://www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore3-Audio Flash meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification 2.0 (Chapter 7) electrical requirements.

8.5.10 USB 2.0 Compatibility

BlueCore3-Audio Flash is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

8.6 Serial Peripheral Interface

BlueCore3-Audio Flash uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore3-Audio Flash via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

8.6.1 Instruction Cycle

The BlueCore3-Audio Flash is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The instruction cycle for a SPI transaction is shown in Table 8.8.

1	Reset the SPI interface	Hold SPI_CSB high for two SPI_CLK cycles
2	Write the command word	Take SPI_CSB low and clock in the 8 bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CSB high

Table 8.8: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore3-Audio Flash on the rising edge of the clock line SPI_CLK. When reading, BlueCore3-Audio Flash will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is teminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore3-Audio Flash offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.6.2 Writing to BlueCore3-Audio Flash

To write to BlueCore3-Audio Flash, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

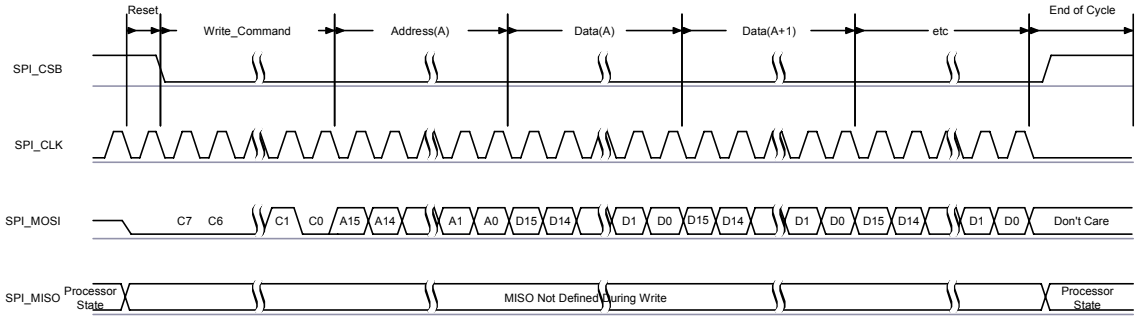


Figure 8.17: Write Operation

8.6.3 Reading from BlueCore3-Audio Flash

Reading from BlueCore3-Audio Flash is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore3-Audio Flash then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

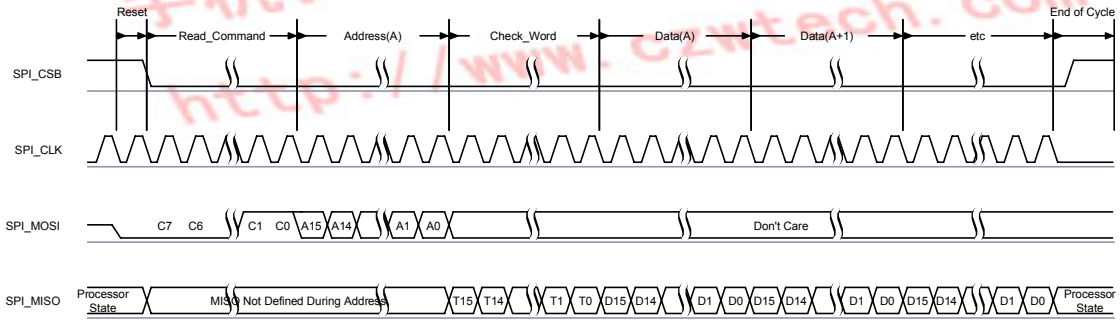


Figure 8.18: Read Operation

8.6.4 Multi Slave Operation

BlueCore3-Audio Flash should not be connected in a multi slave arrangement by simple parallel connection of slave MISO lines. When BlueCore3-Audio Flash is deselected (SPI_CSB = 1), the SPI_MISO line does not float, instead, BlueCore3-Audio Flash outputs 0 if the processor is running or 1 if it is stopped.

8.7 Mono Audio CODEC

The BlueCore3-Audio Flash audio CODEC is compatible with the direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single 1.8 Volt power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 15-bit/sample linear PCM with a data rate of 8kHz.

The CODEC has an input stage containing a microphone amplifier, variable gain amplifier and a Σ-Δ ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The CODEC functional diagram is shown below.

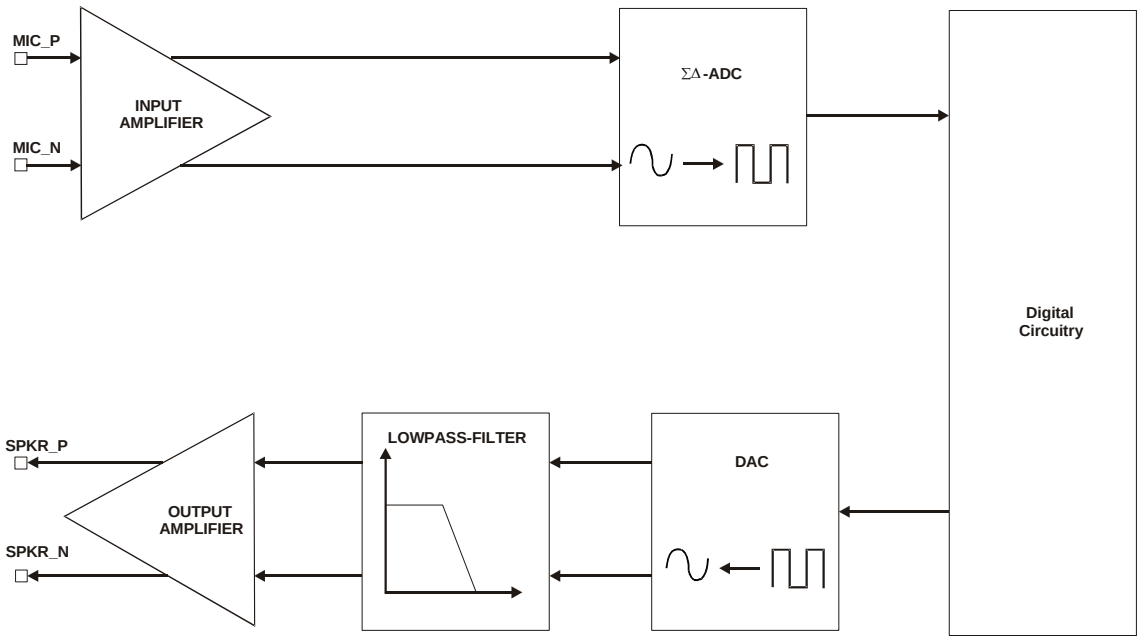


Figure 8.19: BlueCore3-Audio Flash CODEC Diagram

8.7.1 Input Stage

A low noise variable gain amplifier amplifies the signal difference between inputs MIC_N and MIC_P. The input may be from either a microphone or line input. The amplified signal is then digitised by a second order Σ-Δ ADC. The high frequency single bit output from the ADC is converted to 15-bit 8kHz linear PCM data.

The gain is programmable via a PSKEY and has a 42dB range with 3dB resolution. At maximum gain the full scale input level is 3mV rms. A bias network is required for operation with a microphone whereas the line input may be simply a.c. coupled. The following sections explain each of these modes. Single ended signals are supported by BlueCore3-Audio Flash: a single ended signal may be driven into either MIC_N or MIC_P with the undriven input coupled to ground by a capacitor.

The signal to noise ratio is better than 60dB and distortion is less than –75dB.

8.7.2 Microphone Input

The BlueCore3-Audio Flash audio CODEC has been designed for use with microphones that have sensitivities between –60 and –40dBV. The sensitivity of –60dBV is equivalent to a microphone output of 1μA when presented with an input level of 94dB SPL and loaded with 1kΩ. The microphone should be biased as shown in Figure 8.20.

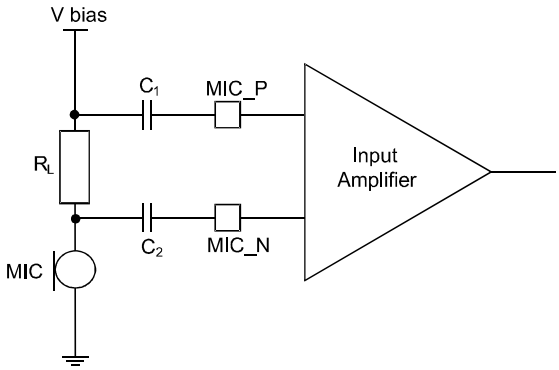


Figure 8.20: BlueCore3-Audio Flash Microphone Biasing

The input impedance at MIC_N and MIC_P is typically 20kΩ. C1 and C2 should be 47nF. R_L sets the microphone load impedance and is normally between 1 and 2kΩ. V bias should be chosen to suit the microphone and have sufficient low noise. It may be obtained by filtering the output of a PIO line.

8.7.3 Line Input

If the input gain is set to less than 21dB BlueCore3-Audio Flash automatically selects line input mode. In this mode the input impedance at MIC_N and MIC_P is increased to 130kΩ typical. At the minimum gain setting the maximum input signal level is 380 mV rms. Figure 8.21 and Figure 8.22 show two circuits for line input operation and show connections for either differential or single ended inputs.

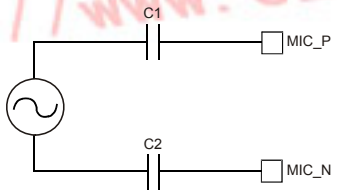


Figure 8.21: Differential Microphone Input

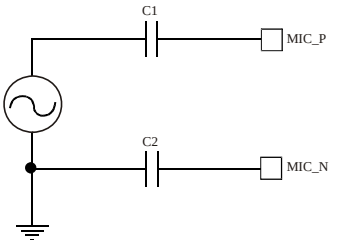


Figure 8.22: Single-ended Microphone Input

Note:

C1 and C2 should be 15nF.

8.7.4 Output Stage

The digital data is converted to an analogue value by a DAC, then it is filtered prior to amplification by the output amplifier and it is available as a differential signal between SPKR_P and SPKR_N. The output amplifier is capable of driving a speaker directly if its impedance is greater than 8Ω. The amplifier is stable with capacitive loads up to 500pF.

The gain is programmable with a range of 21dB and a resolution of 3dB. Maximum output level is typically 700 mV rms for high impedance loads, or 20mA rms for low impedance loads. The signal to noise is better than 70dB and the distortion is less than –75dB.

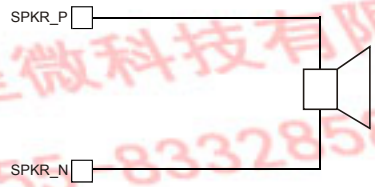


Figure 8.23: Speaker Output

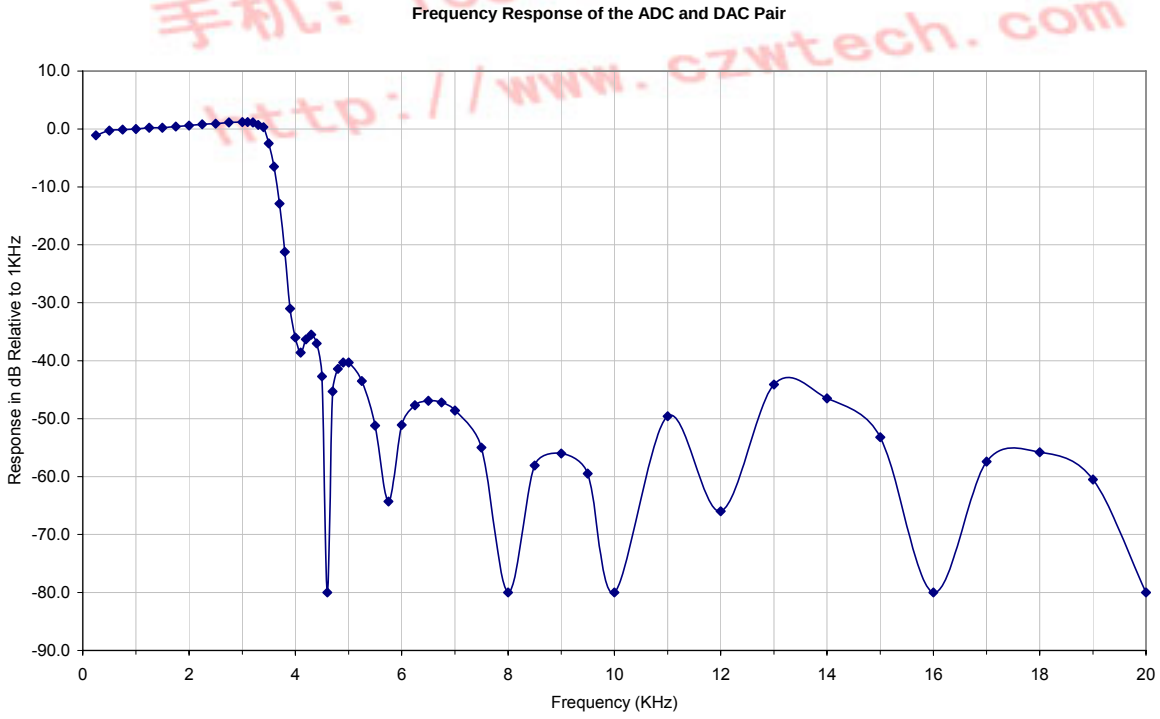


Figure 8.24: Frequency Response of the ADC and DAC Pair

8.7.5 Audio CODEC Outline and Audio Gains

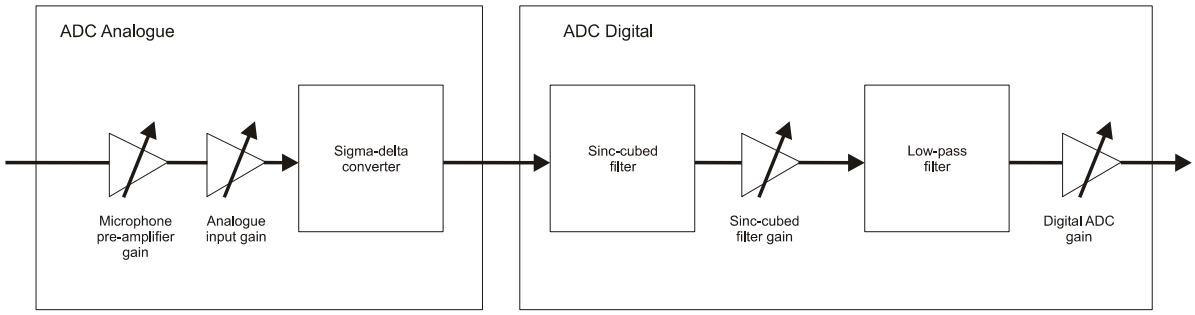


Figure 8.25: ADC Outline and Applicable Gains

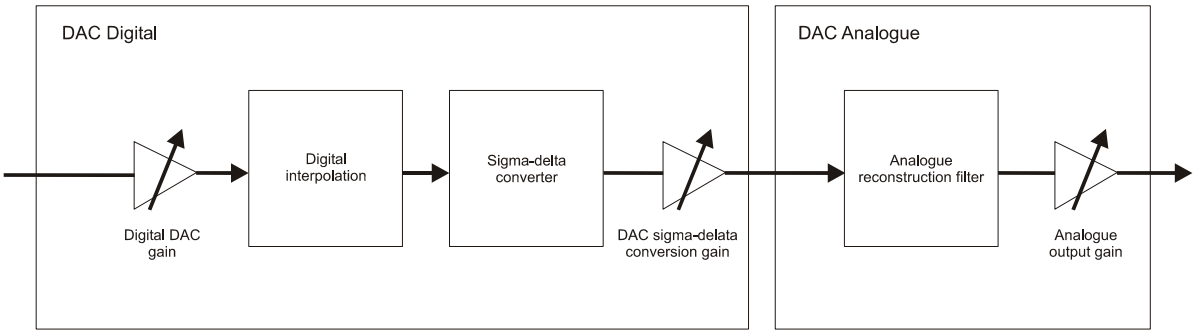


Figure 8.26: DAC Outline and Applicable Gains

Gain Name	PS Key Control Bits	Recommended Usage	Settings
Microphone pre-amplifier gain	CODEC_IN_GAIN[3]	Use to select between line input and microphone input	0 = 0 dB, 1 = 21 dB
Analogue input gain	CODEC_IN_GAIN[2:0]	Use to control the audio input gain	0 = 0dB, 1 = 3dB 2 = 6dB, 3 = 9dB 4 = 12dB, 5 = 15dB 6 = 18 dB, 7 = 21 dB
Sinc-cubed filter gain	CODEC_IN_GAIN[8]	Set to zero	0 = 0 dB, 1 = -6 dB
Digital ADC gain	CODEC_IN_GAIN[7:4]	Use to control the audio input gain, if the analogue ADC gain is exhausted	0 = 0 dB, 1 = 3.5 dB 2 = 6 dB, 3 = 9.5 dB 4 = 12 dB, 5 = 15.5 dB 6 = 18 dB, 7 = 21.5 dB 8 = -24 dB, 9 = -20.5 dB 10 = -18 dB, 11 = -14.5 dB 12 = -12 dB, 13 = -8.5 dB 14 = -6 dB, 15 = -2.5 dB
Digital DAC gain	CODEC_OUT_GAIN[7:4]	Use to control the audio output gain, if the analogue DAC gain is exhausted	Same as for the digital ADC gain
DAC sigma-delta conversion gain	CODEC_OUT_GAIN[9:8]	Set to 3	0 = 0dB, 1 = 2 dB 2 = 3.5 dB, 3 = 4.9 dB
Analogue output gain	CODEC_OUT_GAIN[2:0]	Use to control the audio output gain. Do not use setting 7.	Same as for the analogue ADC gain

Table 8.9: Recommended Settings for Audio CODEC

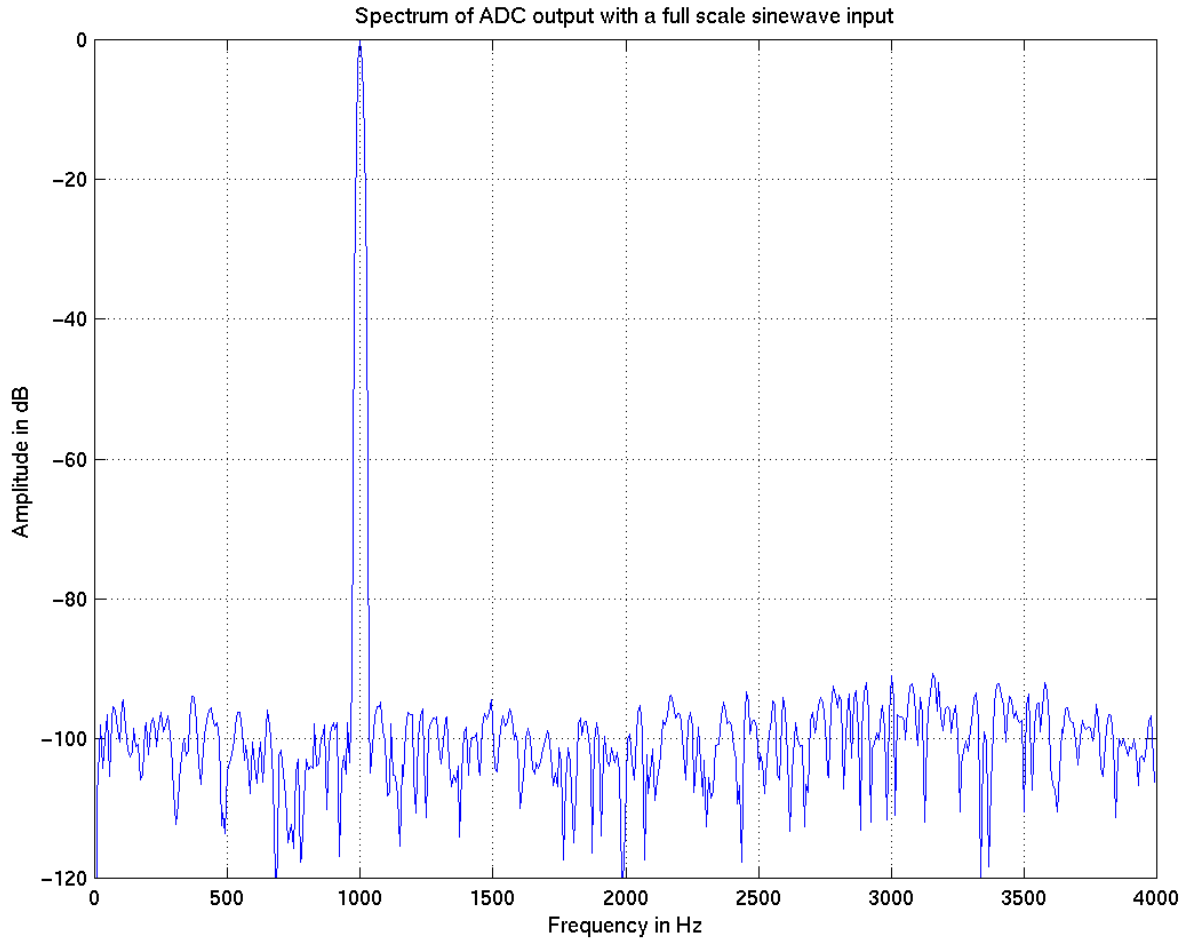


Figure 8.27: Spectrum of Analogue and Digital ADC Output with a Full Scale Sine Wave Input

(300mV RMS) sine into analogue mic amp – output from digital ADC (extracted from BlueCore3-Audio Flash voice buffer)

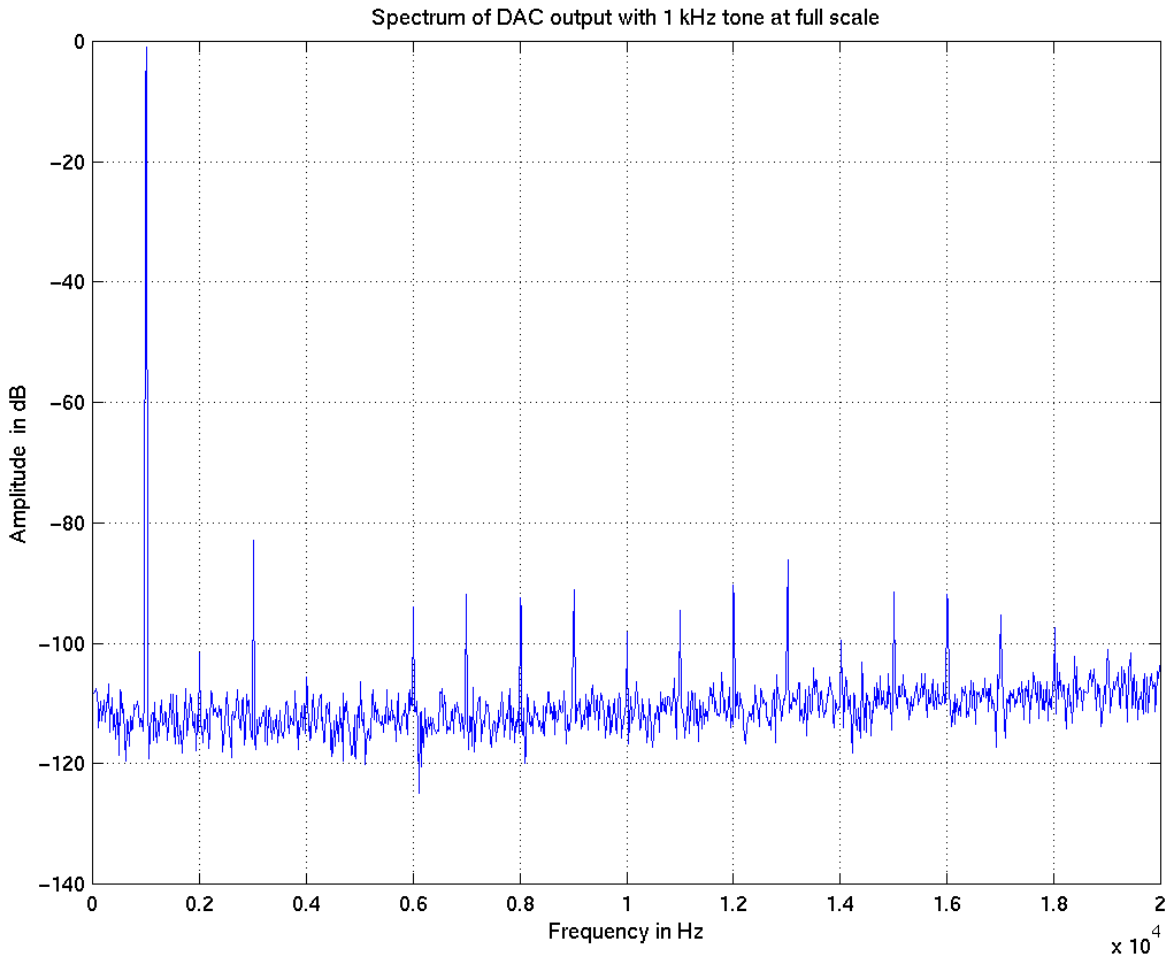


Figure 8.28: Spectrum of DAC Output with 1kHz Tone at Full Scale

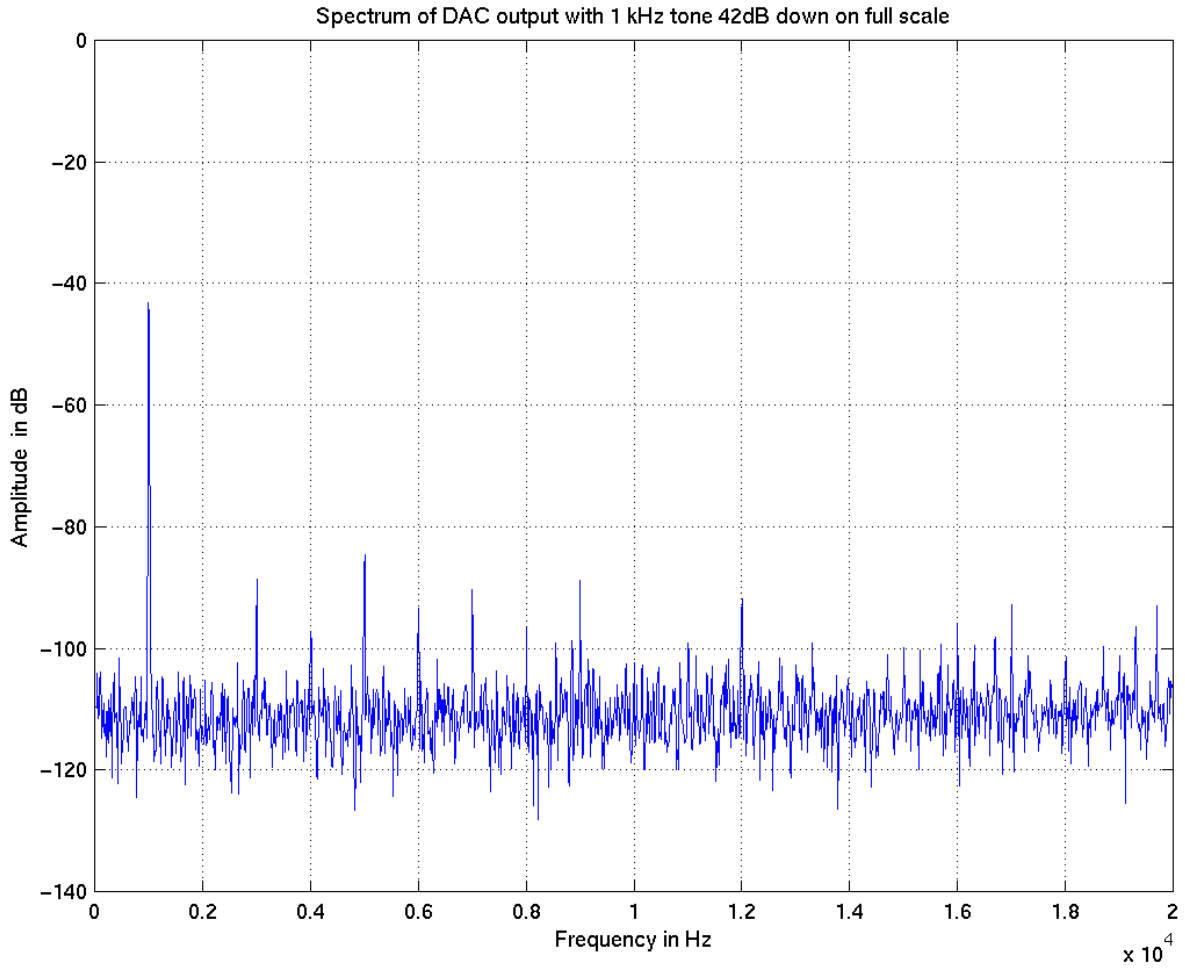


Figure 8.29: Spectrum of DAC Output with 1kHz Tone 42dB down on Full Scale

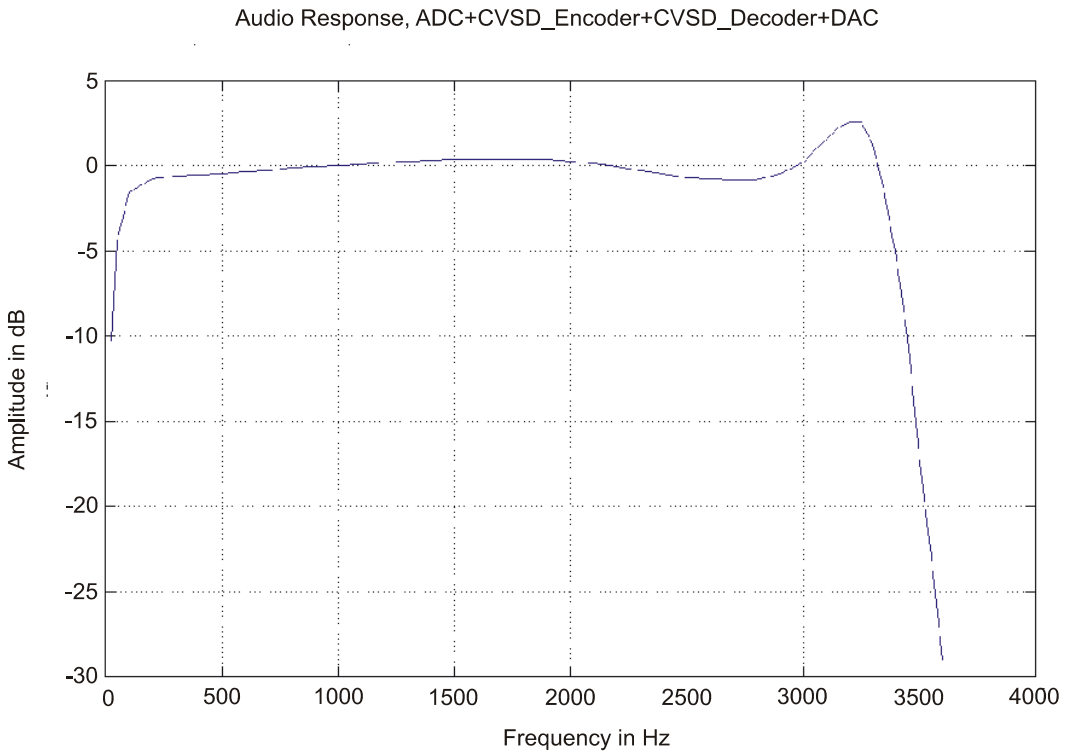


Figure 8.30: Response of CVSD Interpolation/Decimation Filter

8.7.6 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise human voice patterns for transmission over digital communication channels. Through its PCM interface, BlueCore3-Audio Flash has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore3-Audio Flash offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore3-Audio Flash allows the data to be sent to and received from a SCO connection.

Up to three SCO or eSCO connections can be supported by the PCM interface at any one time.

BlueCore3-Audio Flash can operate as the PCM interface Master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave it can operate with an input clock up to 2048kHz. BlueCore3-Audio Flash is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13 or 16-bit linear, 8-bit μ-law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32 (0x1b3).

BlueCore3-Audio Flash interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore3-Audio Flash is also compatible with the Motorola SSI™ interface

8.7.7 PCM Interface Master/Slave

When configured as the Master of the PCM interface, BlueCore3-Audio Flash generates PCM_CLK and PCM_SYNC.

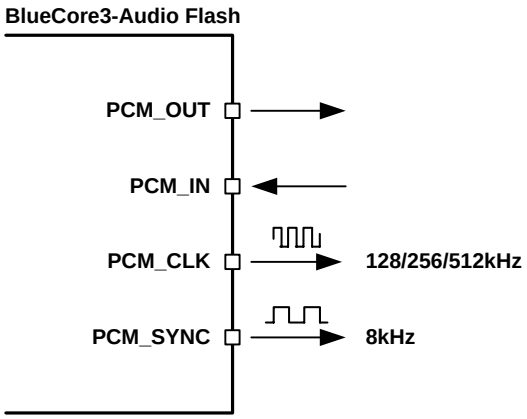


Figure 8.31: BlueCore3-Audio Flash as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore3-Audio Flash accepts PCM_CLK rates up to 2048kHz.

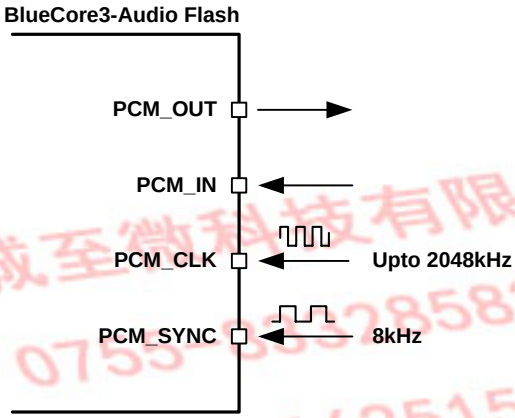


Figure 8.32: BlueCore3-Audio Flash as PCM Interface Slave

8.7.8 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore3-Audio Flash is configured as PCM Master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore3-Audio Flash is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e. 62.5µs long.

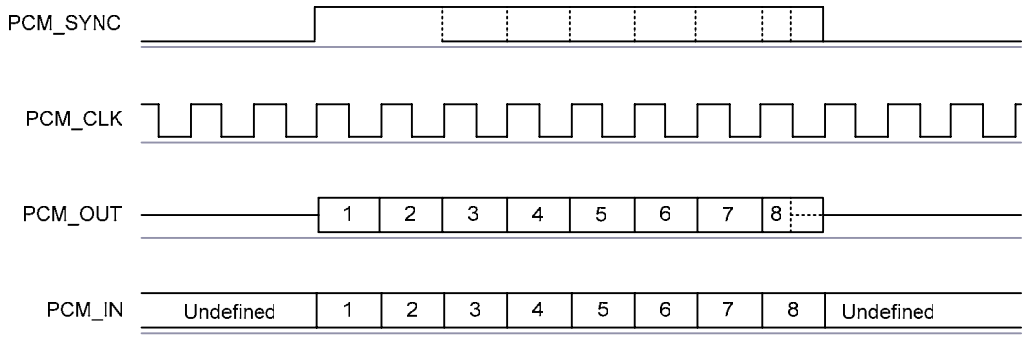


Figure 8.33: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore3-Audio Flash samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.7.9 Short Frame Sync

In Short Frame Sync the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

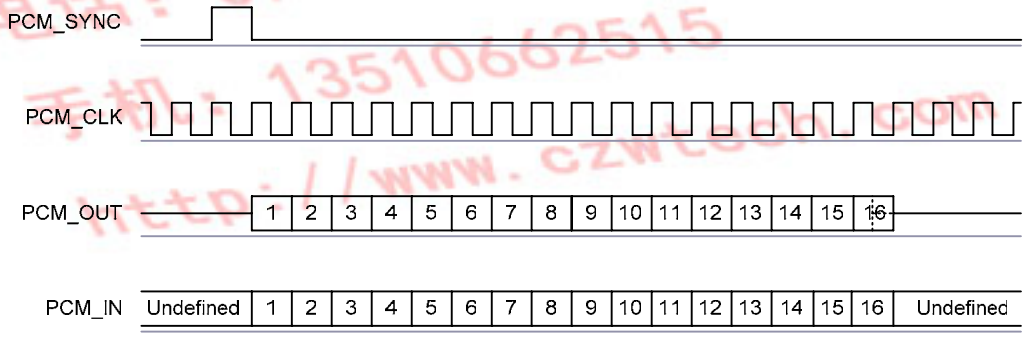


Figure 8.34: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore3-Audio Flash samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

8.7.10 Multi Slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

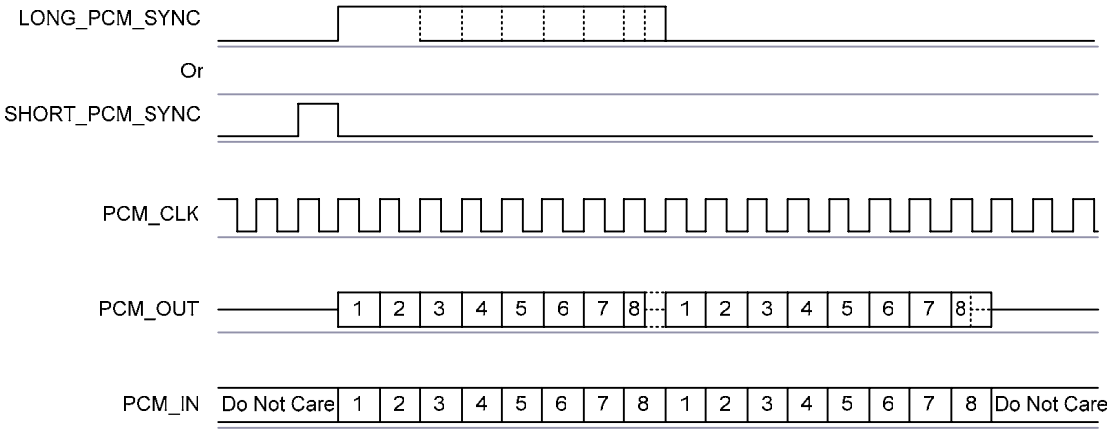


Figure 8.35: Multi Slot Operation with Two Slots and 8-bit Companded Samples

8.7.11 GCI Interface

BlueCore3-Audio Flash is compatible with the General Circuit Interface, a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

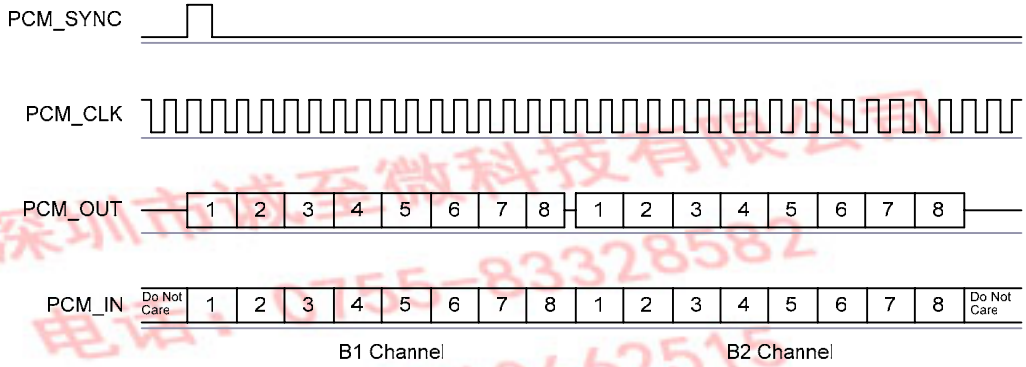


Figure 8.36: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore3-Audio Flash in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

8.7.12 Slots and Sample Formats

BlueCore3-Audio Flash can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8, 13 or 16-bit sample formats.

BlueCore3-Audio Flash supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

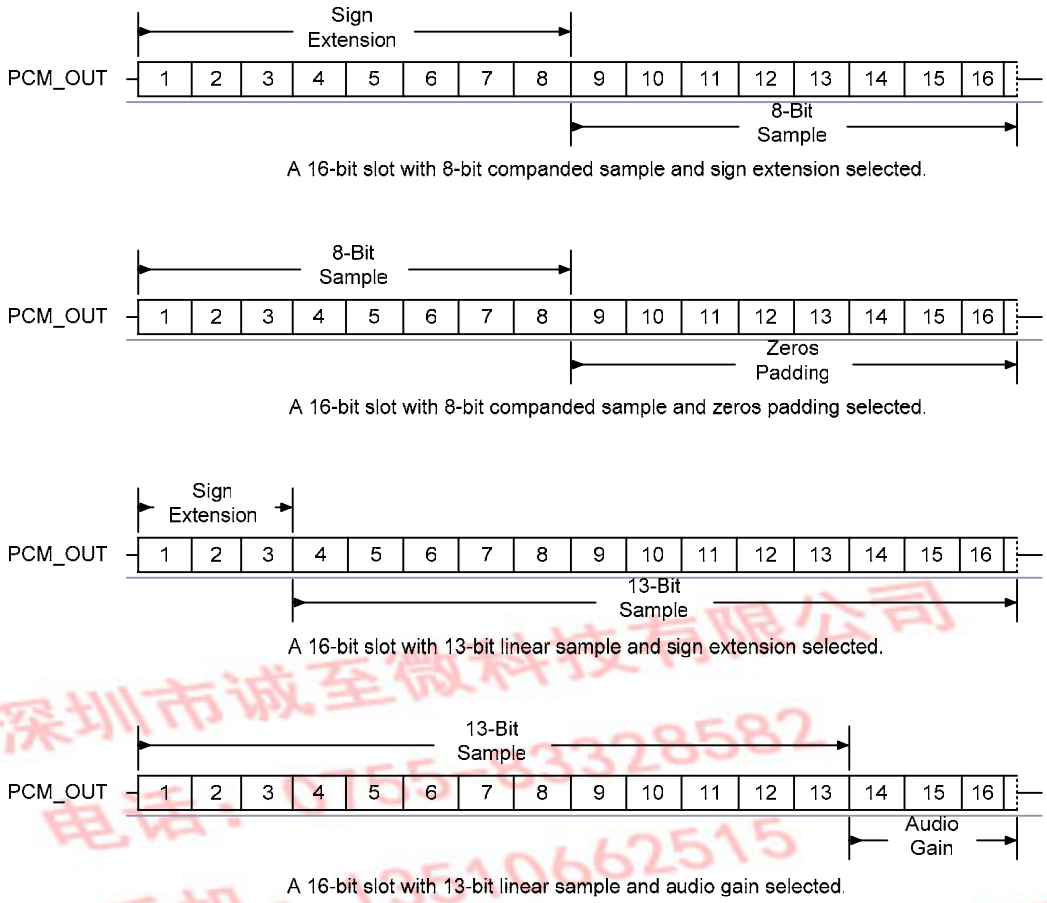


Figure 8.37: 16-Bit Slot Length and Sample Formats

8.7.13 Additional Features

BlueCore3-Audio Flash has a mute facility that forces PCM_OUT to be 0. In Master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

8.7.14 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable, see Table 8.12	-	128 256 512	-	kHz
		48MHz DDS generation. Selection of frequency is programmable, see Table 8.13 and Section 8.7.16	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
t_{mclkh} (1)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (1)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 8.10: PCM Master Timing

Note:

(1) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

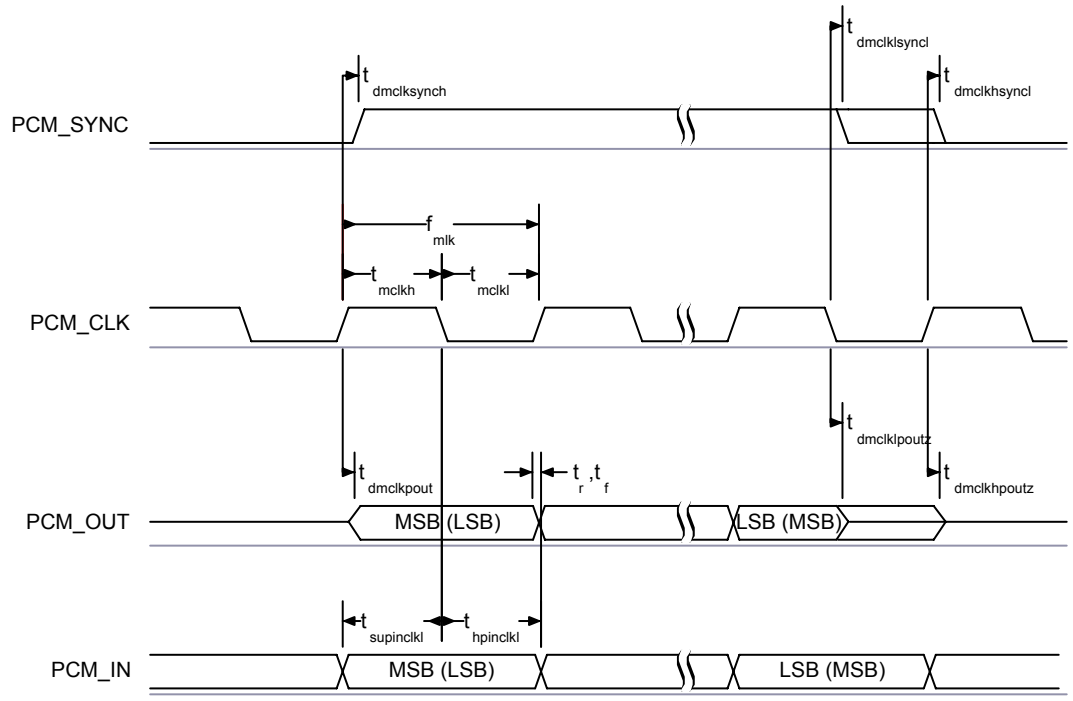


Figure 8.38: PCM Master Timing Long Frame Sync

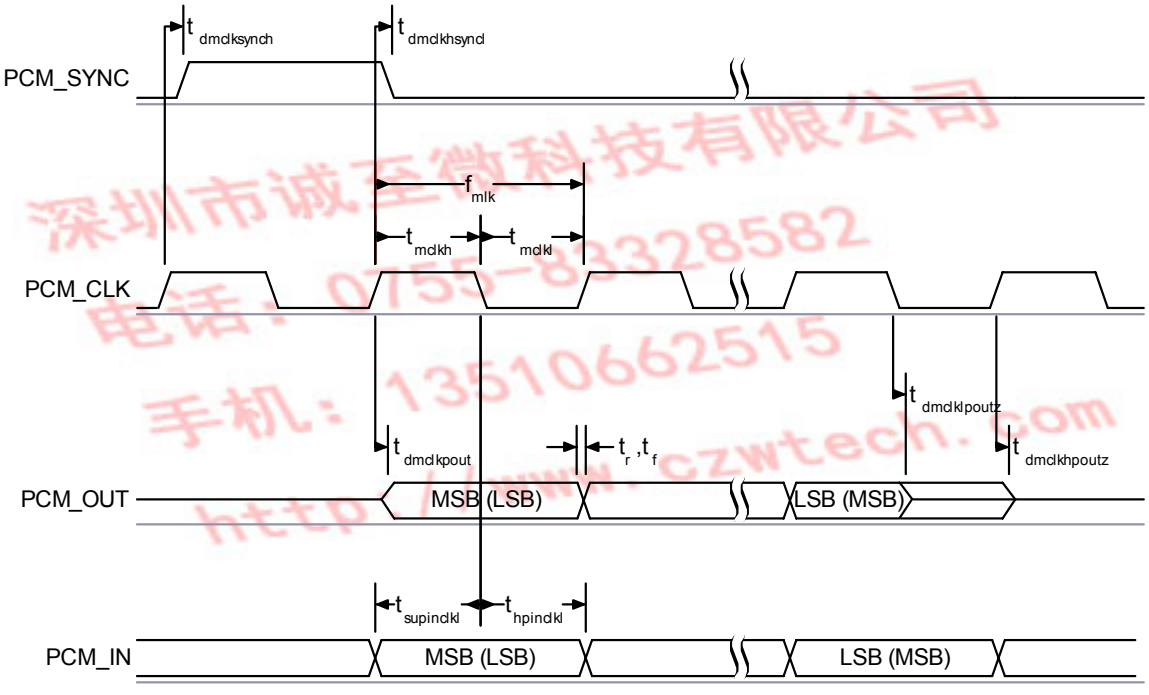


Figure 8.39: PCM Master Timing Short Frame Sync

8.7.15 PCM Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	4096	kHz
t_{sclkl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	30	-		ns

Table 8.11: PCM Slave Timing

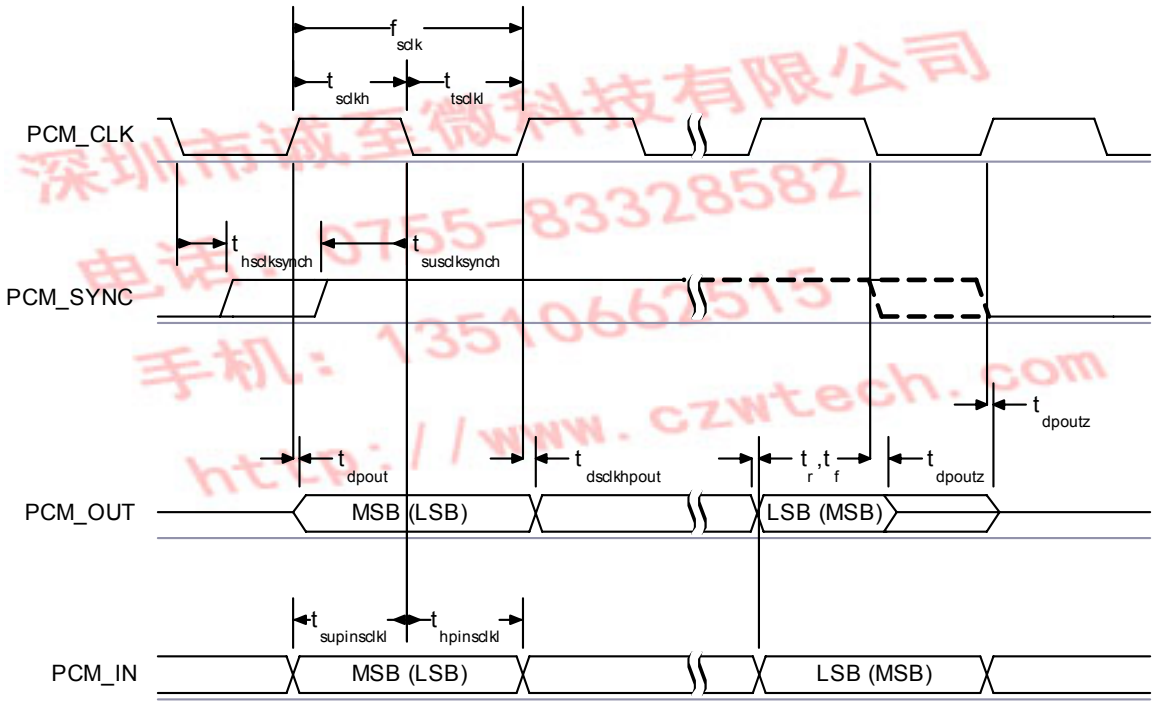


Figure 8.40: PCM Slave Timing Long Frame Sync

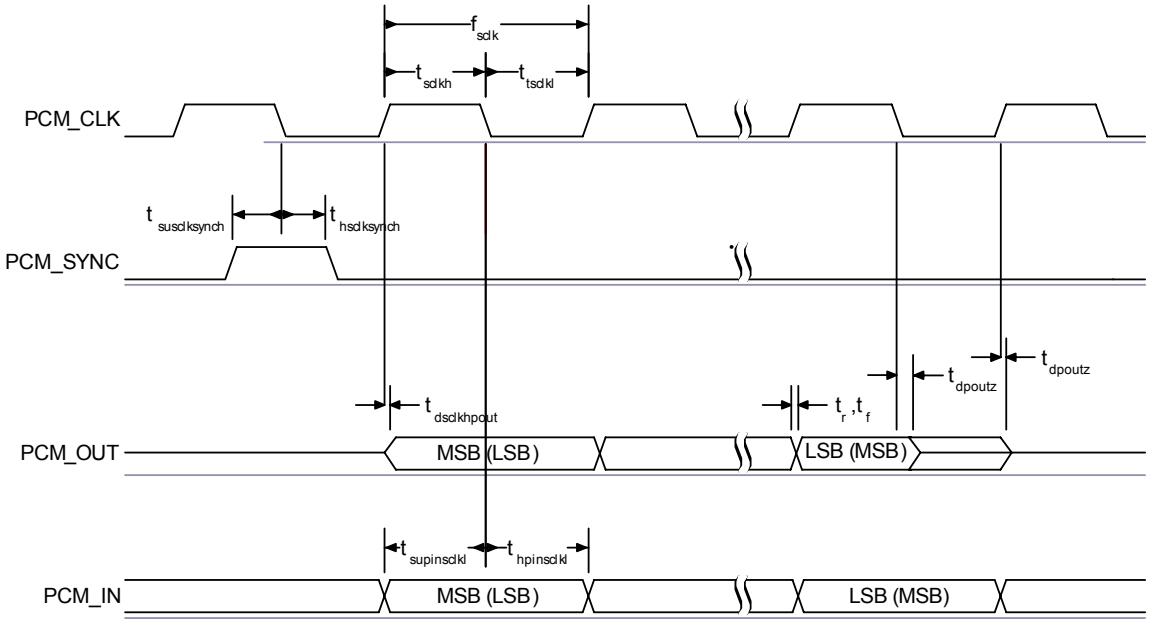


Figure 8.41: PCM Slave Timing Short Frame Sync

8.7.16 PCM_CLK and PCM_SYNC Generation

BlueCore3-Audio Flash has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore3-Audio Flash internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock which allows a greater range of frequencies to be generated with low jitter but consumes more power. This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32.

Note:

The bit SLAVE_MODE_EN should also be set. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

The Equation 8.10 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{CNT\_RATE}{CNT\_LIMIT} \times 24MHz$$

Equation 8.10: PCM_CLK Frequency When Being Generated Using the Internal 48MHz clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using following equation:

$$f = \frac{PCM\_CLK}{SYNC\_LIMIT \times 8}$$

Equation 8.11: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

8.7.17 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The following tables detail these PS Keys. PSKEY_PCM_CONFIG32. The default for this key is 0x00800000 i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristating of PCM_OUT. PSKEY_PCM_LOW_JITTER_CONFIG is described in Table 8.13.

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 selects Master mode with internal generation of PCM_CLK and PCM_SYNC. 1 selects Slave mode requiring externally generated PCM_CLK and PCM_SYNC. This should be set to 1 if 48M_PCM_CLK_GEN_EN (bit 11) is set.
SHORT_SYNC_EN	2	0 selects long frame sync (rising edge indicates start of frame), 1 selects short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 selects padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs, 1 selects sign extension. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit samples the 8 padding bits are zeroes.
LSB_FIRST_EN	5	0 transmits and receives voice samples MSB first, 1 uses LSB first.
TX_TRISTATE_EN	6	0 drives PCM_OUT continuously, 1 tri-states PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 tristates PCM_OUT immediately after the falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is also not active. 1 tristates PCM_OUT after the rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 enables PCM_SYNC output when master, 1 suppresses PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state.
GCI_MODE_EN	9	1 enables GCI mode.
MUTE_EN	10	1 forces PCM_OUT to 0.
48M_PCM_CLK_GEN_EN	11	0 sets PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock, as for BlueCore3-Audio Flash. 1 sets PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock.
LONG_LENGTH_SYNC_EN	12	0 sets PCM_SYNC length to 8 PCM_CLK cycles and 1 sets length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to 0b00000.
MASTER_CLK_RATE	[22:21]	Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration.

Table 8.12: PSKEY_PCM_CONFIG32 Description

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit.
CNT_RATE	[23:16]	Sets PCM_CLK count rate.
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK.

Table 8.13: PSKEY_PCM_LOW_JITTER_CONFIG Description

8.8 I/O Parallel Ports

Fourteen lines of programmable bi-directional input/outputs (I/O) are provided. PIO[11:6] and PIO[3:0] are powered from VDD_PIO. PIO[7:4] are powered from VDD_PADS. AIO [2:0] are powered from VDD_USB.

PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

PIO[0] and PIO[1] are normally dedicated to RXEN and TXEN respectively, but they are available for general use.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO [2] can be configured as a request line for an external clock source. This is useful when the clock to BlueCore3-Audio Flash is provided from a system application specific integrated circuit (ASIC).

BlueCore3-Audio Flash has three general purpose analogue interface pins, AIO[0], AIO[1], and AIO[2]. These are used to access internal circuitry and control signals. One pin is allocated to decoupling for the on-chip band gap reference voltage, the others may be configured to provide additional functionality.

Auxiliary functions available via these pins include an 8-bit ADC and an 8-bit DAC. Typically the ADC is used for battery voltage measurement. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals; 48, 24, 16, 8MHz and the XTAL clock frequency. When used with analogue signals the voltage range is constrained by the analogue supply voltage (1.8V). When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_USB.

8.8.1 PIO Defaults for BTv1.2 HCI Level Bluetooth Stack

CSR cannot guarantee that these terminal functions remain the same. Please refer to the software release note for the implementation of these PIO lines, as they are firmware build specific.

8.9 I²C Interface

PIO[8:6] can be used to form a Master I²C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD), keyboard scanner or EEPROM.

Note:

PIO lines need to be pulled-up through 2.2kΩ resistors.

PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM cannot support UART bypass mode.

For connection to EEPROMs, refer to CSR documentation on I²C EEPROMS for use with BlueCore. This provides information on the type of devices which are currently supported.

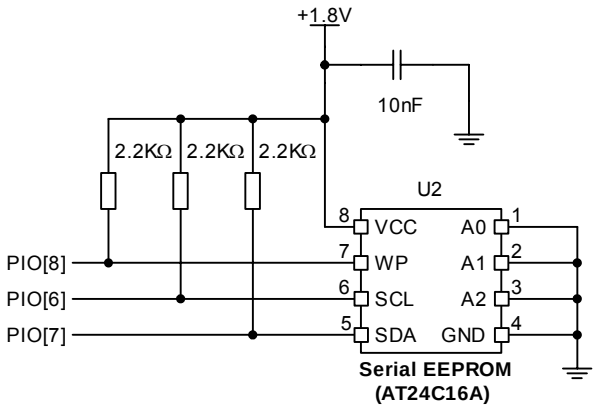


Figure 8.42: Example EEPROM Connection

8.10 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore3-Audio Flash where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the Host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore3-Audio Flash.

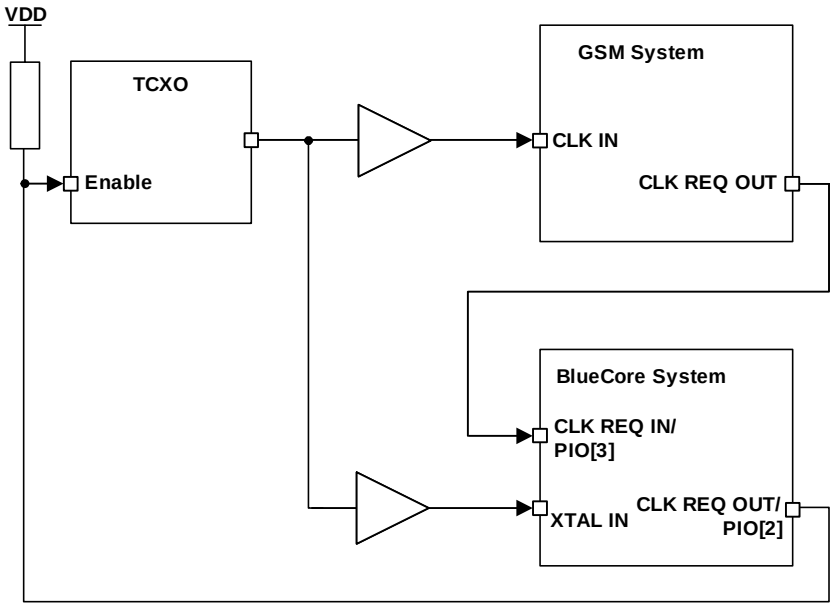


Figure 8.43: Example TXCO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-stated. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

8.11 RESETB

BlueCore3-Audio Flash may be reset from several sources: RESETB pin, power on reset, a UART break character or via a software configured watchdog timer.

The RESET pin is an active high reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms. The RESETB pin is the active low version of RESET and is OR'd on-chip with the active high RESET with either causing the reset function.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tristated. The PIOs have weak pull-downs.

Following a reset, BlueCore3-Audio Flash assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore3-Audio Flash is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore3-Audio Flash free runs, again at a safe frequency.

8.11.1 Pin States on Reset

Table 8.14 shows the pin states of BlueCore3-Audio Flash on reset.

Pin name	State: BlueCore3-Audio Flash
PIO[11:0]	Input with weak pull-down
PCM_OUT	Tri-stated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	Input with weak pull-down
UART_TX	Output tri-stated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tri-stated with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Output tri-stated with weak pull-down
AIO[2:0]	Output, driving low
RESETB	Input with weak pull-up
TEST_EN	Input with strong pull-down
AUX_DAC	High impedance
RX_IN	High impedance
XTAL_IN	High impedance, 250k to XTAL_OUT
XTAL_OUT	High impedance, 250k to XTAL_IN

Table 8.14: Pin States of BlueCore3-Audio Flash on Reset

8.11.2 Status After Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset(1): Baud rate and RAM data not available

Note:

19 Cold Reset constitutes:

- Power cycle
- System reset (firmware fault code)
- Reset signal, see Section 8.11

8.12 Power Supplies

BlueCore3-Audio Flash contains two 1.8V regulators, either of which may be used to power the 1.8V supplies of the device. The device pin VREG_EN is used to enable and disable both of these regulators.

8.12.1 Supply Domains and Sequencing

The 1.8V supplies are VDD_ANA, VDD_VCO, VDD_RADIO, VDD_MEM and VDD_CORE. It is recommended that the 1.8V supplies are all powered at the same time. The order of powering the 1.8V supplies relative to the other I/O supplies (VDD_PIO, VDD_PADS, VDD_USB) is not important, however if the I/O supplies are powered before the 1.8V supplies all digital IO will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_VCO, VDD_RADIO and VDD_MEM should be connected directly to the 1.8V supply; a simple RC filter is recommended for VDD_CORE to reduce transients put back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

8.12.2 External Voltage Source

If the 1.8V rails of BlueCore3-Audio Flash are supplied from an external voltage source, it is recommended that VDD_VCO, VDD_RADIO, and VDD_ANA, should have less than 10mV rms noise levels between 0 to 10MHz. Single tone frequencies are also to be avoided.

The transient response of any regulator used should be 20µs or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption will jump to high levels (see average current consumption section).

8.12.3 Switch-mode Regulator

The on-chip switch-mode 1.8V regulator can be used to power the 1.8V supplies. An external filter circuit of a low-resistance 33µH series inductor followed by a low ESR 5µH shunt capacitor is required between the terminal LX and the 1.8V supply rail. It is recommended that the series resistance of tracks between the BAT_P and BAT_N terminals, the filter components and the external voltage source are minimised to maintain high efficiency power conversion and low supply ripple.

The regulator may be enabled by the VREG_EN pin, by the device firmware, or by the internal battery charger. The regulator is switched into a low power pulse skipping mode when the device is sent into Deep-Sleep mode.

When this regulator and LED outputs are not used, the terminals BAT_P and LX must be grounded or left unconnected. If the LED outputs are required with the regulator disabled, the BAT_P terminal should be connected to a 1.8V supply and the LX terminal left unconnected.

8.12.4 Linear Regulator

The on-chip 1.8V linear regulator may also be used to power the 1.8V dependent supplies or may be used to provide a low noise bias for the electret microphone. It is recommended that a smoothing circuit using a series connected 2.2µF low ESR capacitor and a 2.2Ω resistor to ground is placed on the output of the regulator VREG_OUT.

The regulator may be enabled by the VREG_EN pin or by the device firmware. The regulator is switched into a low power mode when the device is sent into Deep-Sleep mode.

When this regulator is not used the terminals VREG_IN and VREG_OUT must be grounded or left unconnected.

8.12.5 VREG_EN Pin

The regulator enable pin, VREG_EN can be used to enable and disable the BlueCore3-Audio Flash device if one of the on-chip regulators is being used. The pin is active high and has a weak pull down.

When the pin is pulled high the active regulator is enabled, allowing the device to boot-up. The firmware is then able to latch the regulator on and the VREG_EN pin may be released. As the state of the pin is available to the firmware the pin may also be pulsed high to signal that the device should be turned off.

8.13 Battery Charger

The battery charger is a constant current / constant voltage charger circuit and is suitable for Lithium Ion/Polymer batteries only. It must be used in conjunction with the switch-mode regulator as the two circuits share a connection to the battery terminal, BAT_P.

The charger circuit requires a float voltage calibration setting which is stored in Flash memory. To ensure this is set, the circuit enables the switch-mode regulator whenever it enters fast-charge mode. This allows the device to boot-up and read the float voltage from a PSKEY in Flash memory.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, an LED connected to the terminal LED[0] illuminates. When the charger supply is not connected to VDD_CHG the terminal must be left open.

For BC31A223A, charge current is set at 90mA (nominal) to suit a battery with a capacity of 110mAH. For BC31A223B, charge current is set at 40mA (nominal) to suit a battery with a capacitiy of 50mAH. For batteries of other capacities, the charge current can be modified as a customer variant of a standard device. Fast charge current can be set to nominal values between 25mA -110mA. Trickle and flat battery current will be modified proportionately.

Important Note:

See 6.4.3 Integrated Battery Charger Circuit for important notes on Lithium Ion/Polymer battery safety.

8.14 LED Drivers

BlueCore3-Audio Flash includes two 4.2V tolerant pads dedicated to driving LED indicators. Both pads may be controlled by firmware, while LED[0] can also be set by the battery charger.

The pads are low output impedance open-drain outputs, so the LED must be connected in series with a current limiting resistor between the battery terminal or positive supply and the pad.

9 Application Schematic

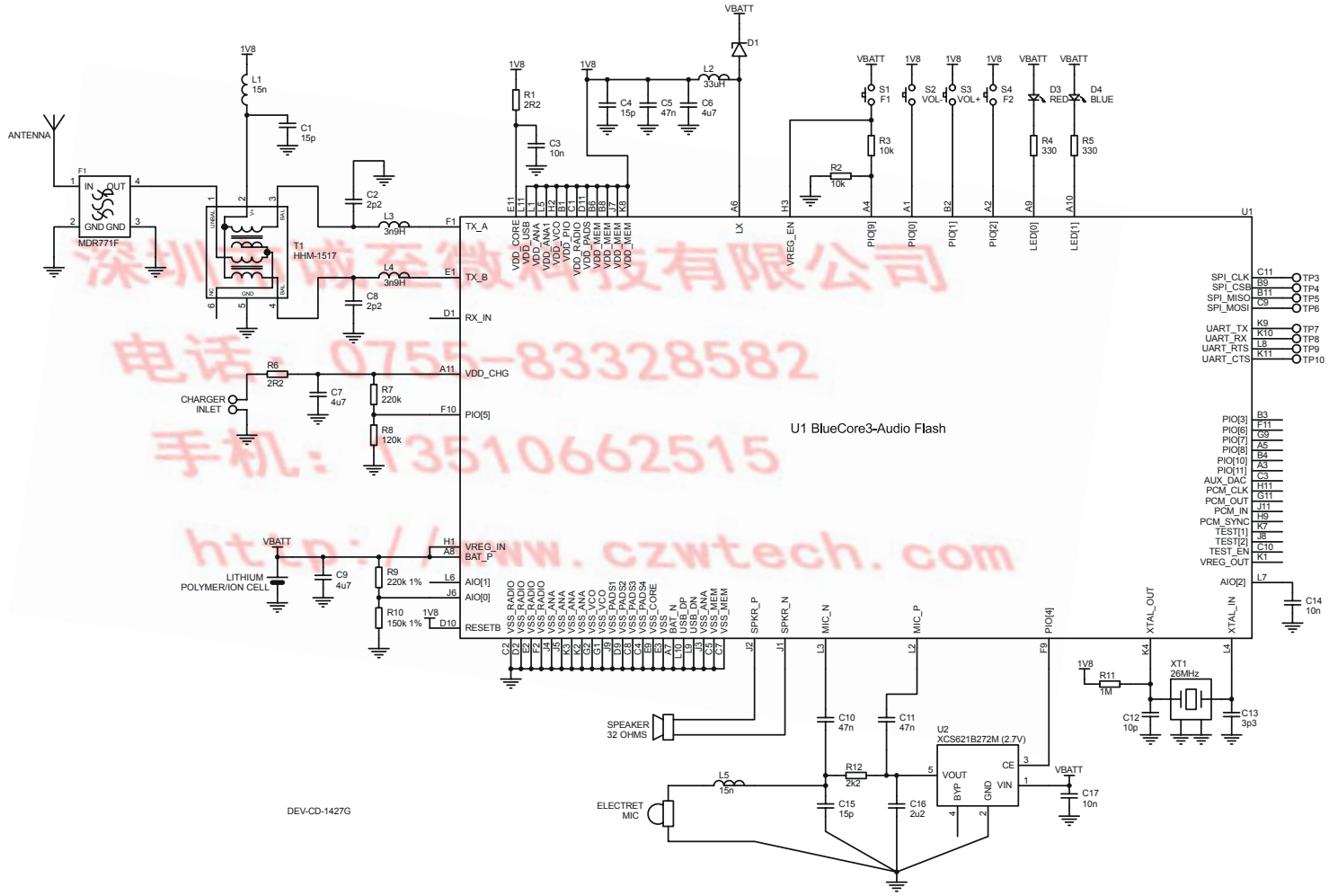
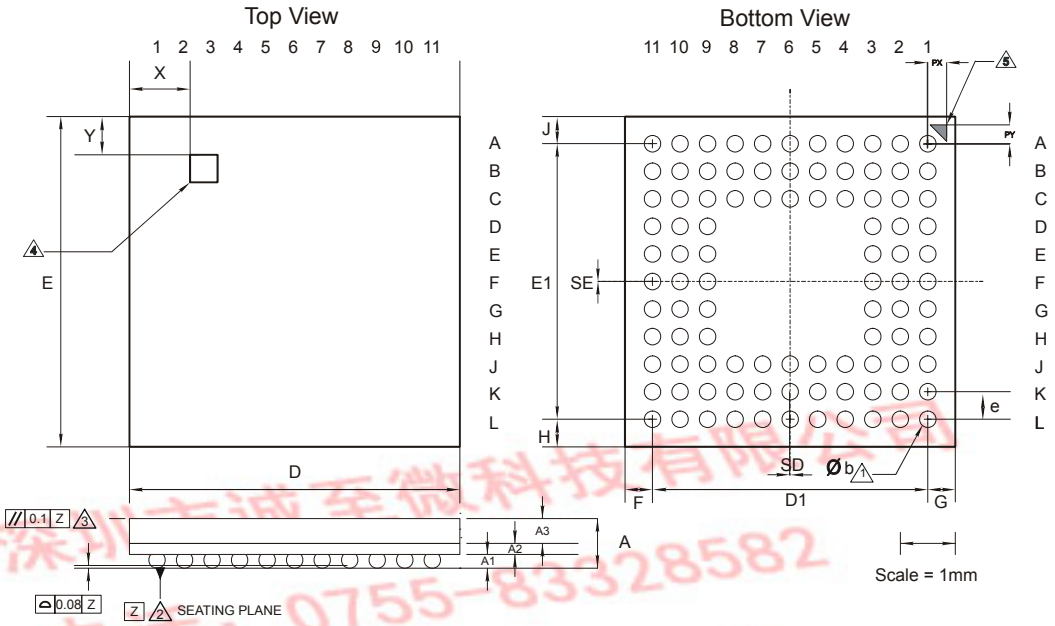


Figure 9.1: Application Circuit for Radio Characteristics Specification with 8 x 8mm TFBGA Package

10 Package Dimensions

10.1 8 x 8mm TFBGA 96-Ball Package



Description	96-Ball Thin Fine-Pitch Ball Grid Array (TFBGA)			
Size	8 x 8 x 1.2mm			
Pitch	0.65mm			
Package Ball Land	Solder mask defined. Solder mask aperture 260µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A			1.2	1 Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.18	0.23	0.28	
A2		0.21		
A3		0.7		2 Datum Z is defined by the spherical crowns of the solder balls
b	0.27	0.32	0.37	
D	7.90	8.00	8.10	3 Parallelism measurement shall exclude any effect of mark on top surface of package
E	7.90	8.00	8.10	
e		0.65		
D1		6.50		4 Top-side polarity mark. The dimensions of the square polarity mark are 0.5 x 0.5mm.
E1		6.50		
F	0.70	0.75	0.80	5 Bottom-side polarity mark. The dimensions of the triangular polarity mark are 0.30 x 0.30 x 0.42mm.
G	0.70	0.75	0.80	
H	0.70	0.75	0.80	
J	0.70	0.75	0.80	
PX		0.40		
PY		0.40		
SD		0		
SE		0		
X		1.10		
Y		0.70		
JEDEC	MO-195			
Unit	mm			

Figure 10.1: BlueCore3-Audio Flash 96-Ball TFBGA Package Dimensions

10.2 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. **Preheat Zone** - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. **Equilibrium Zone** - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
3. **Reflow Zone** - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. **Cooling Zone** - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

10.3 Solder Re-flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

Figure 13.10.2: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile. Lead-free devices will withstand up to 5 reflows to a maximum temperature of 260°C.

11 Ordering Information

11.1 BlueCore3-Audio Flash (Internal Flash)

Interface Version	Package			Battery Current	Order Number
	Type	Size	Shipment Method		
UART and USB	96-Ball TFBGA (Pb free)	8 x 8 x 1.2mm	Tape and reel	90mA	BC31A223A-IVN-E4
UART and USB	96-Ball TFBGA (Pb free)	8 x 8 x 1.2mm	Tape and reel	40mA	BC31A223B-IVN-E4

Note:

Part BC31A223B is pre-production.

Maximum Order Engineering Sample Quantity

2kpcs taped and reeled

Minimum Order Production Quantity

2kpcs taped and reeled

12 Contact Information

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13 Document References

Document	Reference
Specification of the Bluetooth System	v1.2, 05 November 2003
Universal Serial Bus Specification	v2.0, 27 April 2000
Selection of I^2C EEPROMs for Use with BlueCore	bcore-an-008Pb, 30 September 2003
Lithium Ion/Polymer Battery Safety Information Note	bcore-an-057P, 25 November 2004

Terms and Definitions

ACL	Asynchronous Connection-Less. A Bluetooth data packet.
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
A-law	Audio encoding standard
API	Application Programming Interface
ASIC	Application Specific Integrated Circuit
BCSP	BlueCore™ Serial Protocol
BER	Bit Error Rate. Used to measure the quality of a link
BIST	Built-In Self-Test
BlueCore™	Group term for CSR's range of Bluetooth chips
Bluetooth™	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder Decoder
CQDDR	Channel Quality Driven Data Rate
CSB	Chip Select (Active Low)
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DFU	Device Firmware Upgrade
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
FIR	Finite Impulse Response
FSK	Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
HID	Human Interface Device
IQ Modulation	In-Phase and Quadrature Modulation
IF	Intermediate Frequency
IIR	Infinite Impulse Response
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific and Medical
ksps	KiloSamples Per Second
L2CAP	Logical Link Control and Adaptation Protocol (protocol layer)
LC	Link Controller
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LSB	Least-Significant Bit

MCU	MicroController Unit
μ-law	Audio Encoding Standard
MMU	Memory Management Unit
MISO	Master In Serial Out
OHCI	Open Host Controller Interface
PA	Power Amplifier
PCM	Pulse Code Modulation. Refers to digital voice data
Persistent Store	Storage of BlueCore's configuration values in non-volatile memory
PIO	Parallel Input Output
PLL	Phase Lock Loop
ppm	parts per million
PS Key	Persistent Store Key
RAM	Random Access Memory
REB	Read enable (Active Low)
REF	Reference. Represents dimension for reference use only.
RF	Radio Frequency
RFCOMM	Protocol layer providing serial port emulation over L2CAP
RISC	Reduced Instruction Set Computer
rms	root mean squared
RSSI	Receive Signal Strength Indication
RTS	Ready To Send
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented. Voice oriented Bluetooth packet
SD	Secure Digital
SDK	Software Development Kit
SDP	Service Discovery Protocol
SIG	Special Interest Group
SPI	Serial Peripheral Interface
SSI	Signal Strength Indication
TBD	To Be Defined
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus or Upper Side Band (depending on context)
VCO	Voltage Controlled Oscillator
VFBGA	Very Fine Ball Grid Array
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WEB	Write Enable (Active Low)

Document History

Date	Revision	Reason for Change
30 JUN 04	a	Original publication of this document. (CSR reference: BC358239A-ds-001Pa)
11 AUG 04	b	Changes made to name of the device
09 SEP 04	c	Notes added for PIO power supply lines in 8x8 package information
09 DEC 04	d	Important notes concerning Lithium Ion/Polymer battery safety added to sub-sections 6.4.3 Battery Charger and 8.13 Battery Charger. Added information concerning BC31A223B. Changes were made to the front page, to 3 Electrical Characteristics (Input/Output Terminal Characteristics table), to 8.13 Battery Charger and to 11 Ordering Information. Added note to 3 Electrical Characteristics, and additional paragraph to 8.13 Battery Charger to indicate that battery charge current may be modified as a customer variant of a standard BC31A223A or BC31A223B device.
11 FEB 05	e	Added VDD_MEM and VSS_MEM to provide pin compatibility with future devices. Removed pin TEST[3]
19 APR 05	f	Temperature range amended to -40°C to +85°C. Amended max voltage on VDD_CHG to 5.75. Amended Application Schematics to remove VPP. Amended Radio Characteristics data and added RF graphs. Produced as Production Information Data Book, CSR reference BC31A223A-db-001Pf.
17 MAY 05	g	Added VREG_EN Supply Voltage in Electrical Characteristics. Corrected diode numbering on Application Schematic
07 JUN 05	h	Solder profiles added
10 JUN 05	i	Note concerning operation of VREG_IN and VREG_EN updated for Linear Regulator table in 3 Electrical Characteristics. Acronyms and Definitions re-titled Terms and Conditions; Record of Changes re-titled Document History

BlueCore™3-Audio Flash

Product Data Sheet

BC31A223A-ds-001Pi

June 2005