

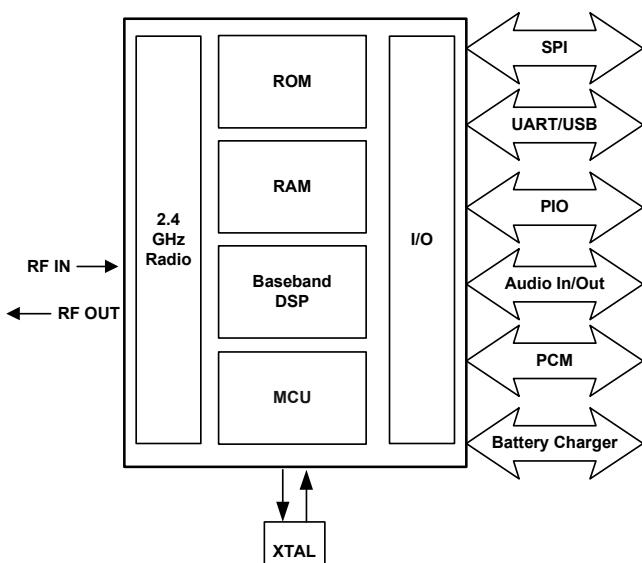
Device Features

- Fully Qualified Bluetooth v2.0+EDR
- Enhanced Data Rate (EDR) compliant with v2.0 of the specification for both 2Mbps and 3Mbps modulation modes
- Full Speed Bluetooth Operation with Piconet and Scatternet Support
- Internal 6Mbit ROM
- Low Power 1.8V operation
- Integrated Switch-mode Regulator
- Integrated Battery Charger with Programmable Current
- 8 x 8mm 96-ball TFBGA Package
- UART Port
- 15-bit Linear Audio CODEC
- 4.2V Tolerant LED Drivers with Intensity Control

General Description

BlueCore™4-Audio ROM is a single chip radio and baseband IC for Bluetooth 2.4GHz systems including enhanced data rates (EDR) to 3Mbps.

BC413159A contains 6Mbit of embedded ROM. When used with the CSR Bluetooth software stack, it provides a fully compliant Bluetooth system to v2.0 + EDR of the specification for data and voice communications.



System Architecture

BlueCore™4-Audio ROM

Single Chip Bluetooth® v2.0 + EDR System

Production Information Data Book For

BC413159A

May 2006

Applications

- Headsets
- Automotive Hands-Free Kits
- General purpose Bluetooth systems requiring an on-chip audio CODEC

BlueCore4-Audio ROM has been designed to reduce the number of external components required which ensures production costs are minimised. The device incorporates auto-calibration and built in self test (BIST) routines to simplify development, type approval and production test. All hardware and device firmware is fully compliant with the Bluetooth v2.0 + EDR specification (all mandatory and optional features).

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1 Status Information

The status of this Data Book is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-Production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-Critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

RoHS Compliance

BlueCore4-Audio ROM devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

2 Key Features

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time. No external trimming is required in production
- Full RF reference designs available
- Bluetooth v2.0 + EDR Specification compliant

Transmitter

- +6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class 1 support using external power amplifier with RF power controlled by an internal 8-bit DAC

Receiver

- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser; requires no external VCO, varactor diode, resonator or loop filter
- Compatible with an external crystal or with an external clock using sinusoidal or logic-level signals
- Accepts frequencies between 8 and 32MHz (in multiples of 250kHz); additionally accepts 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies typically used in GSM and CDMA devices

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip linear regulator; 1.8V output from a 2.2-4.2V input, can also be used to generate microphone bias
- Power-on-reset cell detects low supply voltage

Auxiliary Features (Continued)

- Arbitrary power supply sequencing permitted
- 8-bit ADC and DAC available to applications
- Battery charger with programmable current (25 -100mA) for Lithium Ion /Polymer battery
- LED intensity control for dedicated LED1 and LED0 outputs

Baseband and Software

- Internal 6Mbit ROM
- Internal 48KB RAM to support EDR. Allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ -law and linear voice from host and A-law, μ -law and CVSD voice over air

Physical Interfaces

- Synchronous serial interface up to 4Mbaud for system debugging
- UART interface with programmable baud rate up to 3Mbaud with an optional bypass mode
- Full speed USB v1.1 interface supports OHCI and UHCI host interfaces. Compliant with USB v2.0
- Optional I²C™ compatible interface

Audio CODEC

- 15-bit resolution, 8kHz sampling frequency
- Digital enhancements to add bass cut, side tone and treble boost
- Analogue enhancements to support single-ended speaker drive capability and reference availability

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on-chip in a variety of configurations:

- Standard HCI (UART or USB)
- Fully embedded to RFCOMM
- Customised builds with embedded application code

Package Options

- 96-ball TFBGA, 8 x 8 x 1.2mm, 0.65mm pitch

3 Package Information

3.1 BlueCore4-Audio ROM Pinout Diagram

Orientation from Top of Device

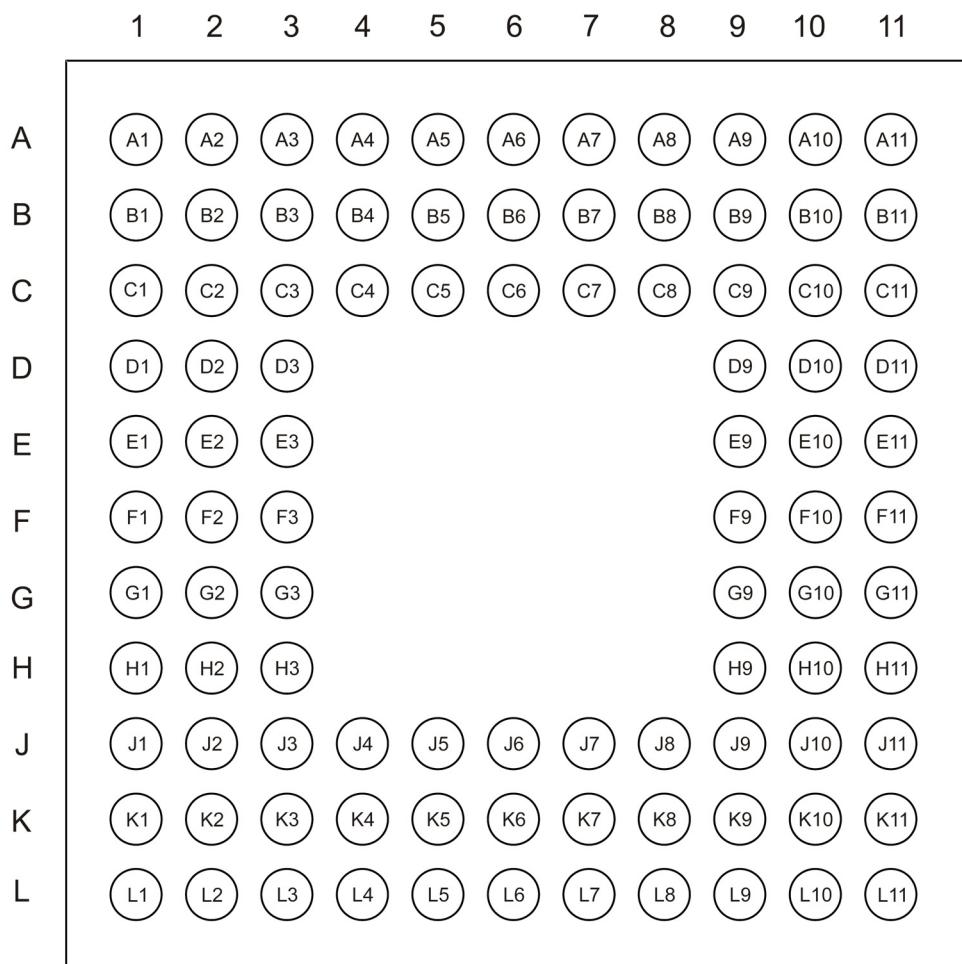


Figure 3.1: BlueCore4-Audio ROM Device Pinout

3.2 Device Terminal Functions

| Radio | Ball | Pad Type | Supply Pad | Description |
|-------------|------|---|------------|--|
| RX_IN | D1 | Analogue | VDD_RADIO | Single ended receiver input |
| PIO[0]/RXEN | A1 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | Control output for external TX/RX switch (if fitted) |
| PIO[1]/TXEN | B2 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | Control output for external PA (If fitted) |
| RF_N | F1 | Analogue | VDD_RADIO | Transmitter output/switched receiver input |
| RF_P | E1 | Analogue | VDD_RADIO | Complement of RF_N |
| AUX_DAC | C3 | Analogue | VDD_PIO | Voltage DAC output |

| Synthesiser and Oscillator | Ball | Pad Type | Supply Pad | Description |
|----------------------------|------|----------|------------|-------------------------------------|
| XTAL_IN | L4 | Analogue | VDD_ANA | For crystal or external clock input |
| XTAL_OUT | K4 | Analogue | VDD_ANA | Drive for crystal |

| USB and UART | Ball | Pad Type | Supply Pad | Description |
|--------------|------|--|------------|---|
| UART_TX | K9 | CMOS output, tri-state, with weak internal pull-up | VDD_USB | UART data output |
| UART_RX | K10 | CMOS input with weak internal pull-down | VDD_USB | UART data input |
| UART_RTS | L8 | CMOS output, tri-state, with weak internal pull-up | VDD_USB | UART request to send active low |
| UART_CTS | K11 | CMOS input with weak internal pull-down | VDD_USB | UART clear to send active low |
| USB_DP | L10 | Bi-directional | VDD_USB | USB data plus with selectable internal 1.5kΩ pull-up resistor |
| USB_DN | L9 | Bi-directional | VDD_USB | USB data minus |

| PCM Interface | Ball | Pad Type | Supply Pad | Description |
|---------------|------|--|------------|-------------------------|
| PCM_OUT | G11 | CMOS output, tri-state, with weak internal pull-down | VDD_PADS | Synchronous data output |
| PCM_IN | J11 | CMOS input, with weak internal pull-down | VDD_PADS | Synchronous data input |
| PCM_SYNC | H9 | Bi-directional with weak internal pull-down | VDD_PADS | Synchronous data sync |
| PCM_CLK | H11 | Bi-directional with weak internal pull-down | VDD_PADS | Synchronous data clock |

| PIO Port | Ball | Pad Type | Supply Pad | Description |
|---------------------------------|------|---|------------|--|
| PIO[2]/CLK_REQ | A2 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | PIO or external clock request |
| PIO[3]/USB_WAKE_UP/HOST_CLK_REQ | B3 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | PIO or output goes high to wake up PC when in USB mode or clock request input from host controller |
| PIO[4]/USB_ON | F9 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | PIO or USB on (input senses when VBUS is high, wakes BlueCore4-Audio ROM) |
| PIO[5]/USB_DETACH | F10 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | PIO line or chip detaches from USB when this input is high |
| PIO[6]/CLK_REQ | F11 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | PIO line or clock request output to enable external clock for external clock line |
| PIO[7]/CLK_OUT | G9 | Bi-directional with programmable strength internal pull-up/down | VDD_PADS | Programmable input/output line or programmable frequency clock output |
| PIO[8] | A5 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | Programmable input/output line |
| PIO[9] | A4 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | Programmable input/output line |
| PIO[10] | B4 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | Programmable input/output line |
| PIO[11] | A3 | Bi-directional with programmable strength internal pull-up/down | VDD_PIO | Programmable input/output line |
| AIO[0] | J6 | Bi-directional | VDD_USB | Programmable input/output line |
| AIO[1] | L6 | Bi-directional | VDD_USB | Programmable input/output line |
| AIO[2] | L7 | Bi-directional | VDD_USB | Programmable input/output line |
| LED[0] | A9 | Open drain output | VDD_BAT | Current sink to drive LED |
| LED[1] | A10 | Open drain output | VDD_BAT | Current sink to drive LED |

| Test and Debug | Ball | Pad Type | Supply Pad | Description |
|----------------|------|----------|------------|--|
| MIC_P | L2 | Analogue | VDD_ANA | Microphone differential, Input P |
| MIC_N | L3 | Analogue | VDD_ANA | Microphone differential, Input N |
| SPKR_P | J2 | Analogue | VDD_ANA | Speaker differential output P or single ended output |
| SPKR_N | J1 | Analogue | VDD_ANA | Speaker differential output N |

| Test and Debug | Ball | Pad Type | Supply Pad | Description |
|----------------|------|--|------------|--|
| RESETB | D10 | CMOS input with weak internal pull-up | VDD_PADS | Reset if low. Input debounced so must be low for >5ms to cause a reset |
| SPI_CSB | B9 | CMOS input with weak internal pull-up | VDD_PADS | Chip select for Synchronous Serial Interface active low |
| SPI_CLK | C11 | CMOS input with weak internal pull-down | VDD_PADS | Serial Peripheral Interface clock |
| SPI_MOSI | C9 | CMOS input with weak internal pull-down | VDD_PADS | Serial Peripheral Interface data input |
| SPI_MISO | B11 | CMOS output, tri-state, with weak internal pull-down | VDD_PADS | Serial Peripheral Interface data output |
| TEST_EN | C10 | CMOS input with strong internal pull-down | VDD_PADS | For test purposes only(leave unconnected) |

| Power Supplies and Control | Ball | Pad Type | Description |
|----------------------------|--------------------|------------------------------|--|
| VREG_EN | H3 | CMOS input | Enable input terminal for both voltage regulators |
| VREG_IN | H1 | Regulator input | Linear regulator input |
| VREG_OUT | K1 | Regulator output | Linear regulator output |
| V_CHG | A11 | Charger input | Input for battery charger |
| BAT_P | A8 | Battery terminal + | Lithium-Ion/Polymer battery positive terminal/Input connection for switch-mode regulator |
| BAT_N | A7 | Battery terminal - | Lithium-Ion/Polymer battery negative terminal/Ground connection for switch-mode regulator |
| LX | A6 | Switch-mode regulator output | Switch-mode power regulator output |
| VDD_USB | L11 | VDD | Positive supply for UART/USB ports |
| VDD_PIO | B1 | VDD | Positive supply for PIO and AUX DAC ^(a) |
| VDD_MEM | B6,B8,J7, K8 | VDD | Positive supply for memory. Connect to VDD_CORE to provide pin compatibility with previous devices |
| VDD_PADS | D11 | VDD | Positive supply for all digital Input/Output ports ^(b) |
| VDD_CORE | E11 | VDD | Positive supply for internal digital circuitry |
| VDD_RADIO | C1 | VDD/Regulator sense | Positive supply for RF circuitry |
| VDD_VCO | H2 | VDD | Positive supply for local oscillator circuitry |
| VDD_ANA | L1,L5 | VDD | Positive supply for analogue circuitry and 1.8V regulated output |
| VSS_MEM | C5,C7 | VSS | Ground connection for memory. Connect to provide pin compatibility with future devices |
| VSS_PADS | C4, C8, D9,J9 | VSS | Ground connection for input/output ports |
| VSS_CORE | E9 | VSS | Ground connection for internal digital circuitry |
| VSS_RADIO | C2,D2,E2, F2 | VSS | Ground connections for RF circuitry |
| VSS_VCO | G1,G2 | VSS | Ground connections for local oscillator |
| VSS_ANA | J3,J4,J5, K2,K3 | VSS | Ground connections for analogue circuitry |
| VSS | E3 | VSS | Ground connection |

(a) Positive supply for PIO[3:0] and PIO[11:6].

(b) Positive supply for SPI/PCM ports and PIO[7:4]

| Unconnected Terminals | Ball | Description |
|-----------------------|---|-------------------|
| N/C | B5, B7, B10, C6, D3, E10, F3, G3, G10, H10, J8, J10, K5, K6, K7 | Leave unconnected |

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4 Electrical Characteristics

4.1 Absolute Maximum Ratings

| Rating | Min | Max |
|--|----------|----------|
| Storage temperature | -40°C | +150°C |
| Supply voltage: VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE | -0.4V | 2.2V |
| Supply voltage: VDD_PADS, VDD_PIO, VDD_MEM and VDD_USB | -0.4V | 3.7V |
| Supply Voltage: VREG_IN | -0.4V | 5.6V |
| Supply Voltage: BAT_P | -0.4V | 4.25V |
| Supply Voltage: V_CHG | -0.4V | 6.5V |
| Other terminal voltages | VSS-0.4V | VDD+0.4V |

4.2 Recommended Operating Conditions

| Operating Condition | Min | Max |
|--|-------|----------|
| Operating temperature range | -40°C | +105°C |
| Guaranteed RF performance range(a) | -40°C | +85°C |
| Supply voltage: VDD_RADIO, VDD_VCO, VDD_ANA and VDD_CORE | 1.7V | 1.9V |
| Supply voltage: VDD_PADS, VDD_PIO, VDD_MEM and VDD_USB | 1.7V | 3.6V |
| Supply voltage: VREG_IN | 2.2V | 5.25V(b) |
| Supply voltage: BAT_P | 2.5V | 4.2V |
| Supply voltage: V_CHG | 4.5V | 6.5V |

(a) Typical figures are given for RF performance between -40°C and +105°C.

(b) The device will operate without damage with VREG_IN as high as 5.6V. However the RF performance is not guaranteed above 5.25V.

4.3 Linear Regulator

| Linear Regulator | Min | Typ | Max | Unit |
|---|------|------|---------|--------|
| Normal Operation | | | | |
| Input voltage | 2.2 | - | 5.25(a) | V |
| Dropout voltage ($I_{load} = 70$ mA) | - | - | 350 | mV |
| Output Voltage ($I_{load} = 70$ mA) | 1.70 | 1.78 | 1.9 | V |
| Temperature Coefficient | -250 | - | +250 | ppm/°C |
| Output Noise ^(b) (c) | - | - | 1 | mV rms |
| Load Regulation ($I_{load} < 100$ mA) | - | - | 50 | mV/A |
| Settling Time ^(b) (d) | - | - | 50 | μs |
| Maximum Output Current | 100 | - | - | mA |
| Minimum Load Current | 5 | - | - | μA |
| Input Voltage | - | - | 4.2 | V |
| Quiescent Current (excluding load, $I_{load} < 1$ mA) | 25 | 35 | 50 | μA |
| Low Power Mode^(e) | | | | |
| Quiescent Current (excluding load, $I_{load} < 100$ μA) | 4 | 7 | 10 | μA |
| Disabled Mode^(f) | | | | |
| Quiescent Current | 1.5 | 2.5 | 3.5 | μA |

- (a) Operation up to 5.6V is permissible without damage and without the output voltage rising sufficiently to damage the rest of BlueCore4-Audio ROM, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 5.25V.
- (b) Regulator output connected to 47nF pure and 4.7μF 2.2Ω ESR capacitors.
- (c) Frequency range is 100Hz to 100kHz.
- (d) 1mA to 70mA pulsed load.
- (e) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode.
- (f) Regulator is disabled when VREG_EN is pulled low. It is also disabled when VREG_IN is either open circuit or driven to the same voltage as VDD_ANA.

4.4 Switch-mode Regulator

| Switch-mode Regulator | Min | Typ | Max | Unit |
|---|------|-------|------|--------|
| Input voltage | 2.5 | - | 4.2 | V |
| Output voltage ($I_{load} = 70$ mA) | 1.70 | 1.78 | 1.9 | V |
| Temperature coefficient | -250 | - | +250 | ppm/°C |
| Normal Operation | | | | |
| Output ripple | - | - | 1 | mV rms |
| Transient settling time ^(a) | - | - | 50 | μs |
| Maximum load current | 100 | - | - | mA |
| Conversion efficiency (I_{load} 70 mA) | - | 90 | - | % |
| Switching frequency ^(b) | - | 1.333 | - | MHz |
| Start-up current limit ^(c) | - | 60 | - | mA |
| Low Power Mode^(d) | | | | |
| Output ripple | - | - | 1 | mV rms |
| Transient settling time ^(e) | - | - | 700 | mV rms |
| Maximum load current | 20 | - | - | mA |
| Minimum load current | 0 | - | - | μA |
| Conversion efficiency (I_{load} 1mA) | - | 80 | - | % |
| Switching frequency ^(f) | 50 | - | 150 | kHz |
| Disabled Mode | | | | |
| Quiescent Current | - | - | 1 | μA |

- (a) 1mA to 70mA pulsed load.
- (b) Locked to crystal frequency
- (c) Current is limited on start-up to prevent excessive stored energy in the filter inductor. The regulator will operate with reduced efficiency until the current limiter is disabled during the firmware boot-up sequence.
- (d) Low power mode is entered and exited automatically when the chip enters/leaves Deep Sleep mode
- (e) 100μA to 1mA pulsed load
- (f) Defines minimum period between pulses. Pulses are skipped at low current loads.

4.5 Battery Charger

| Battery Charger | Min | Typ | Max | Unit |
|---|------|------|------|------|
| Input voltage | 4.5 | - | 6.5 | V |
| Charging Mode (BAT_P rising to 4.2V) | | | | |
| Supply current (a) | - | 2 | - | mA |
| Flat battery charge current(b) | - | 4 | - | mA |
| Battery trickle charge current(c) (d) | | | | |
| Maximum setting (I-CTRL=15): | - | 10 | - | mA |
| Minimum setting (I-CTRL=0): | - | 2.5 | - | mA |
| Maximum battery fast charge current (I-CTRL =15)(e) (d) | | | | |
| (V_CHG - BAT_P > 0.3V): | - | 100 | - | mA |
| (V_CHG - BAT_P > 0.7V): | - | 50 | - | mA |
| Minimum battery fast charge current (I-CTRL=0)(e) (d) | | | | |
| (V_CHG - BAT_P > 0.3V): | - | 25 | - | mA |
| (V_CHG - BAT_P > 0.7V): | - | 15 | - | mA |
| Trickle charge voltage threshold | - | 2.9 | - | V |
| Float voltage (with correct trim value set)(f) | 4.17 | 4.2 | 4.23 | V |
| Float voltage trim step size(f) | | 50 | - | mV |
| Battery charge termination current(g) | - | 10 | - | % |
| Standby Mode (BAT_P falling from 4.2V) | | | | |
| Supply current(a) | - | 80 | - | µA |
| Battery current | - | -40 | - | µA |
| Battery recharge hysteresis(h) | 100 | - | 200 | mV |
| Shutdown Mode (V_CHG too low) | | | | |
| V_CHG under-voltage threshold | | | | |
| (V_CHG rising): | - | 3.9 | - | V |
| (V_CHG falling): | - | 3.7 | - | V |
| V_CHG - BAT_P lockout threshold | | | | |
| (V_CHG rising): | - | 0.22 | - | V |
| (V_CHG falling): | - | 0.17 | - | V |
| Supply current | - | - | 100 | µA |
| Battery current | -1 | - | 0 | µA |

- (a) Current into V_CHG - does not include current delivered to battery ($I(V_{CHG}) - I(BAT_P)$)
- (b) BAT_P < 1.8V approx.
- (c) $1.8V < BAT_P < \text{Float voltage}$
- (d) Charge current can be set in 16 equally spaced steps, under the control of a register setting I-CTRL
- (e) Trickle charge threshold $< BAT_P < \text{Float voltage}$
- (f) Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence
- (g) Specified as a percentage of the Fast charge current
- (h) Hysteresis of $(V_{FLOAT} - BAT_P)$ for charging to restart

4.6 Digital Terminals

| Digital Terminals | | Min | Typ | Max | Unit |
|--|-------------------|---------|------|---------|------|
| Input Voltage Levels | | | | | |
| V _{IL} input logic level low | 2.7V ≤ VDD ≤ 3.6V | -0.4 | - | +0.8 | V |
| | 1.7V ≤ VDD ≤ 1.9V | -0.4 | - | +0.4 | V |
| V _{IH} input logic level high | | 0.7VDD | - | VDD+0.4 | V |
| Output Voltage Levels | | | | | |
| V _{OL} output logic level low, (I _o = 4.0mA), 2.7V ≤ VDD ≤ 3.6V | | - | - | 0.2 | V |
| V _{OL} output logic level low, (I _o = 4.0mA), 1.7V ≤ VDD ≤ 1.9V | | - | - | 0.4 | V |
| V _{OH} output logic level high, (I _o = -4.0mA), 2.7V ≤ VDD ≤ 3.6V | | VDD-0.2 | - | - | V |
| V _{OH} output logic level high, (I _o = -4.0mA), 1.7V ≤ VDD ≤ 1.9V | | VDD-0.4 | - | - | V |
| Input and Tri-state Current with: | | | | | |
| Strong pull-up | | -100 | -40 | -10 | µA |
| Strong pull-down | | +10 | +40 | +100 | µA |
| Weak pull-up | | -5.0 | -1.0 | -0.2 | µA |
| Weak pull-down | | +0.2 | +1.0 | +5.0 | µA |
| I/O pad leakage current | | -1 | 0 | +1 | µA |
| C _I Input Capacitance | | 1.0 | - | 5.0 | pF |

4.7 USB Terminals

| USB Terminals | Min | Typ | Max | Unit |
|--|------------|-----|------------|------|
| VDD_USB for correct USB operation | 3.1 | | 3.6 | V |
| Input Threshold | | | | |
| V _{IL} input logic level low | - | - | 0.3VDD_USB | V |
| V _{IH} input logic level high | 0.7VDD_USB | - | - | V |
| Input Leakage Current | | | | |
| VSS_PADS < VIN < VDD_USB ^(a) | -1 | 1 | 5 | µA |
| C _I Input capacitance | 2.5 | - | 10.0 | pF |
| Output Voltage Levels to Correctly Terminated USB Cable | | | | |
| V _{OL} output logic level low | 0.0 | - | 0.2 | V |
| V _{OH} output logic level high | 2.8 | - | VDD_USB | V |

(a) Internal USB pull-up disabled

4.8 Power on Reset

| Power-on Reset | Min | Typ | Max | Unit |
|----------------------------|------|------|------|------|
| VDD_CORE falling threshold | 1.40 | 1.50 | 1.60 | V |
| VDD_CORE rising threshold | 1.50 | 1.60 | 1.70 | V |
| Hysteresis | 0.05 | 0.10 | 0.15 | V |

4.9 Auxilliary ADC

| Auxiliary ADC | Min | Typ | Max | Unit |
|---|------------|---------|---------|-----------|
| Resolution | - | - | 8 | Bits |
| Input voltage range (LSB size = VDD_ANA/255) | 0 | - | VDD_ANA | V |
| Accuracy (Guaranteed monotonic) | INL DNL | -1 0 | - - | 1 1 |
| Offset | -1 | - | 1 | LSB |
| Gain Error | -0.8 | - | 0.8 | % |
| Input Bandwidth | - | 100 | - | kHz |
| Conversion time | - | 2.5 | - | μs |
| Sample rate ^(a) | - | - | 700 | Samples/s |

(a) ADC is accessed through the VM function. The sample rate given is achieved as part of this function.

4.10 Auxilliary DAC

| Auxiliary DAC | Min | Typ | Max | Unit |
|---|-------------|--------------------------|---------|---------------|
| Resolution | - | - | 8 | Bits |
| Average output step size ^(a) | 12.5 | 14.5 | 17.0 | mV |
| Output Voltage | | monotonic ^(a) | | |
| Voltage range ($I_O=0\text{mA}$) | VSS_PADS | - | VDD_PIO | V |
| Current range | -10.0 | - | 0.1 | mA |
| Minimum output voltage ($I_O=100\mu\text{A}$) | 0.0 | - | 0.2 | V |
| Maximum output voltage ($I_O=10\text{mA}$) | VDD_PIO-0.3 | - | VDD_PIO | V |
| High Impedance leakage current | -1 | - | 1 | μA |
| Offset | -220 | - | 120 | mV |
| Integral non-linearity ^(a) | -2 | - | 2 | LSB |
| Settling time (50pF load) | - | - | 10 | μs |

(a) Specified for an output voltage between 0.2V and VDD_PIO -0.2V. Output is high impedance when chip is in Deep Sleep mode.

4.11 Clocks

| Crystal Oscillator | Min | Typ | Max | Unit |
|------------------------------------|-----|------|---------|------------------|
| Crystal frequency ^(a) | 8.0 | - | 32.0 | MHz |
| Digital trim range ^(b) | 5.0 | 6.2 | 8.0 | pF |
| Trim step size ^(b) | - | 0.1 | - | pF |
| Transconductance | 2.0 | - | - | mS |
| Negative resistance ^(c) | 870 | 1500 | 2400 | Ω |
| External Clock | | | | |
| Input frequency ^(d) | 7.5 | - | 40.0 | MHz |
| Clock input level ^(e) | 0.2 | - | VDD_ANA | V pk-pk |
| Allowable Jitter | - | - | 15 | ps rms |
| XTAL_IN input impedance | - | - | - | $\text{k}\Omega$ |
| XTAL_IN input capacitance | - | 7 | - | pF |

(a) Integer multiple of 250kHz

(b) The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

(c) XTAL frequency = 16MHz; XTAL C0 = 0.75pF; XTAL load capacitance = 8.5pF.

(d) Clock input can be any frequency between 8MHz and 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 7.68, 14.44, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

(e) Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

4.12 Audio CODEC

| Audio CODEC, 15Bit Resolution | Min | Typ | Max | Unit |
|---|------------------|------|--------------|------------|
| Microphone Amplifier | | | | |
| Input full scale at maximum gain | - | 3 | - | mV rms |
| Input full scale at minimum gain | - | 350 | - | mV rms |
| Gain resolution ^(a) | 2.8 | 3 | 3.2 | dB |
| Distortion at 1kHz | - | - | -78 | dB |
| Input referenced rms noise ^(b) | - | 5 | - | µV rms |
| Bandwidth | - | 20 | - | kHz |
| Mic mode input impedance | - | 20 | - | kΩ |
| Input mode input impedance | - | 130 | - | Ω |
| Analogue to Digital Converter | | | | |
| Input sample rate ^(c) | - | 1 | - | MSamples/s |
| Output sample rate ^(d) | - | 8 | - | KSamples/s |
| Distortion and noise at 1kHz (relative to full scale) | - | -78 | -75 | dB |
| Digital to Analogue Converter | | | | |
| Gain resolution | 2.8 | 3 | 3.2 | dB |
| Min gain ^(e) | - | -18 | - | dB |
| Max gain ^(e) | - | 3 | - | dB |
| Loudspeaker Driver | | | | |
| Output voltage full scale swing (differential) | - | 2.0 | - | V Pk-Pk |
| Output current drive (at full scale swing) ^(f) | 10 | 20 | 40 | mA |
| Output full scale current (at reduced swing) ^(g) | - | 75 | - | mA |
| Output -3dB bandwidth | - | 18.5 | - | kHz |
| Distortion and noise (relative to full scale) (32Ω load) differential | - | -75 | - | dB |
| Allowed load: resistive | 8 ^(h) | - | Open Circuit | Ω |
| Allowed load: capacitive | - | - | 500 | pF |

- (a) 42dB range of gain control (under software control)
- (b) Noise in bandwidth from 100Hz to 4kHz gain setting >17dB
- (c) Single bit, second order T - Δ ADC clocked at 1MHz
- (d) This is the decimated and filtered output at 15-bit resolution
- (e) 21dB gain range (under software control)
- (f) Output for 0.1%THD, signal level of 2V Pk-Pk differential
- (g) Output for 1%THD, signal level of 1V Pk-Pk differential
- (h) Output swing reduced to 1.2V Pk-Pk differential with 1%THD or 0.1V Pk-Pk differential with 0.1%THD

4.13 Power Consumption

4.13.1 Linear Regulator - Typical Average Current

| Operation Mode | Connection Type | UART Rate (kbps) | Average (3V3 Supply) | Unit |
|--|-----------------|------------------|----------------------|------|
| Page scan | - | 115.2 | 0.49 | mA |
| Inquiry and page scan | - | 115.2 | 0.83 | mA |
| ACL No traffic | Master | 115.2 | 4.1 | mA |
| ACL With file transfer | Master | 115.2 | 11.8 | mA |
| ACL No traffic | Slave | 115.2 | 16.8 | mA |
| ACL With file transfer | Slave | 115.2 | 20.5 | mA |
| ACL 40ms sniff | Master | 38.4 | 2.40 | mA |
| ACL 1.28s sniff | Master | 38.4 | 0.37 | mA |
| SCO HV1 | Master | 38.4 | 40.8 | mA |
| SCO HV3 | Master | 38.4 | 20.4 | mA |
| SCO HV3 30ms sniff | Master | 38.4 | 19.9 | mA |
| ACL 40ms sniff | Slave | 38.4 | 2.2 | mA |
| ACL 1.28s sniff | Slave | 38.4 | 0.42 | mA |
| Parked 1.28s beacon | Slave | 38.4 | 0.20 | mA |
| SCO HV1 | Slave | 38.4 | 40.9 | mA |
| SCO HV3 | Slave | 38.4 | 25.2 | mA |
| SCO HV3 30ms sniff | Slave | 38.4 | 19.0 | mA |
| Standby Host connection ^(a) | - | 38.4 | 76 | µA |
| Reset (RESETB low) ^(a) | - | - | 58 | µA |

(a) Low power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode.

4.13.2 Switch-mode Regulator - Typical Average Current

| Operation Mode | Connection Type | UART Rate (kbps) | Average (2V7 Supply) | Average (4V2 Supply) | Unit |
|-------------------------|-----------------|------------------|----------------------|----------------------|------|
| Page scan | - | 115.2 | 0.35 | 0.22 | mA |
| Inquiry and page scan | - | 115.2 | 0.60 | 0.39 | mA |
| ACL No traffic | Master | 115.2 | 3.3 | 2.4 | mA |
| ACL With file transfer | Master | 115.2 | 7.6 | 5.0 | mA |
| ACL No traffic | Slave | 115.2 | 13.2 | 8.7 | mA |
| ACL With file transfer | Slave | 115.2 | 15.3 | 10.0 | mA |
| ACL 40ms sniff | Master | 38.4 | 1.6 | 1.2 | mA |
| ACL 1.28s sniff | Master | 38.4 | 0.26 | 0.20 | mA |
| SCO HV1 | Master | 38.4 | 31.0 | 19.5 | mA |
| SCO HV3 | Master | 38.4 | 15.6 | 10.1 | mA |
| SCO HV3 30ms sniff | Master | 38.4 | 15.3 | 9.9 | mA |
| ACL 40ms sniff | Slave | 38.4 | 1.4 | 1.1 | mA |
| ACL 1.28s sniff | Slave | 38.4 | 0.32 | 0.24 | mA |
| Parked 1.28s beacon | Slave | 38.4 | 0.14 | 0.10 | mA |
| SCO HV1 | Slave | 38.4 | 31.1 | 19.6 | mA |
| SCO HV3 | Slave | 38.4 | 19.3 | 12.5 | mA |
| SCO HV3 30ms sniff | Slave | 38.4 | 14.9 | 9.8 | mA |
| Standby Host connection | - | 38.4 | 40 | 36 | µA |

4.13.3 Typical Measurement Conditions

| | |
|----------------------------|---------------|
| Firmware | HCI 19.2 |
| VREG_IN, VDD_PIO, VDD_PADS | 3.15V |
| Clock source | 26MHz crystal |
| Output power | 0dBm |

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5 Radio Characteristics - Basic Data Rate

Important Note:

BlueCore4-Audio ROM meets the Bluetooth v2.0+EDR specification when used in a suitable application circuit between -40°C and +105°C. TX output is guaranteed unconditionally stable over guaranteed temperature range (between -40°C and +85°C).

5.1 Temperature +20°C

5.1.1 Transmitter

| Radio Characteristics | VDD = 1.8V | | Temperature = +20°C | | |
|---|------------|------|---------------------|-------------------------------|----------------|
| | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) ^(b) | 1.5 | 5.5 | - | -6 to +4 ^(c) | dBm |
| RF power variation over temperature range with compensation enabled(\pm) ^(d) | - | 1.2 | 2 | - | dB |
| RF power variation over temperature range with compensation disabled(\pm) | - | 2.7 | 5 | - | dB |
| RF power control range | 25 | 35 | - | ≥ 16 | dB |
| RF power range control resolution ^(e) | - | 0.5 | 1.5 | - | dB |
| 20dB bandwidth for modulated carrier | - | 780 | 1000 | ≤ 1000 | kHz |
| Adjacent channel transmit power $F = F_0 \pm 2\text{MHz}$ ^(f) ^(g) | - | -41 | -20 | ≤ -20 | dBm |
| Adjacent channel transmit power $F = F_0 \pm 3\text{MHz}$ | - | -45 | -40 | ≤ -40 | dBm |
| Adjacent channel transmit power $F = F_0 \pm > 3\text{MHz}$ | - | -50 | -40 | ≤ -40 | dBm |
| $\Delta f_{1\text{avg}}$ Maximum Modulation | 140 | 164 | 175 | $140 < f_{1\text{avg}} < 175$ | kHz |
| $\Delta f_{2\text{max}}$ Minimum Modulation | 115 | 152 | - | ≥ 115 | kHz |
| $\Delta f_{1\text{avg}}/\Delta f_{2\text{avg}}$ | 0.8 | 0.98 | - | ≥ 0.80 | - |
| Initial carrier frequency tolerance | -30 | 5 | 30 | ± 75 | kHz |
| Drift Rate | - | 7 | 20 | ≤ 20 | kHz/50 μ s |
| Drift (single slot packet) | - | 8 | 25 | ≤ 25 | kHz |
| Drift (five slot packet) | - | 10 | 40 | ≤ 40 | kHz |
| 2 nd Harmonic Content | - | -50 | -30 | ≤ -30 | dBm |
| 3 rd Harmonic Content | - | -45 | -30 | ≤ -30 | dBm |

- (a) The BlueCore4-Audio ROM firmware maintains the transmit power within Bluetooth v2.0+EDR specification limits
- (b) Measurement using PSKEY_LC_MAX_TX_POWER setting corresponding to a PSKEY_LC_POWER_TABLE power table entry = 63
- (c) Class 2 RF transmit power range, Bluetooth specification v2.0+EDR
- (d) These parameters are dependent on matching circuit used, and its behaviour over temperature, therefore these parameters are not under CSR's direct control
- (e) Resolution guaranteed over the range -5dB to -25dB relative to maximum power for Tx Level > 20
- (f) Measured at $F_0 = 2441\text{MHz}$
- (g) BlueCore4-Audio ROM guaranteed to meet ACP performance in Bluetooth v2.0+EDR specification, three exceptions allowed.

| Radio Characteristics | | VDD = 1.8V | Temperature = +20°C | | | | |
|---|------------------|-----------------|---------------------|-----|---------------------|---------------|----------|
| | | Frequency (GHz) | Min | Typ | Max | Cellular Band | Unit |
| Emitted power in cellular bands measured at unbalanced port of the balun. Output power = TBDdBm | 0.869 - 0.894(a) | - | TBD | - | GSM 850 | | dBm / Hz |
| | 0.869 - 0.894(b) | - | TBD | - | CDMA 850 | | |
| | 0.925 - 0.960(a) | - | TBD | - | GSM 900 | | |
| | 1.570 - 1.580(c) | - | TBD | - | GPS | | |
| | 1.805 - 1.880(a) | - | TBD | - | GSM 1800 / DCS 1800 | | |
| | 1.930 - 1.990(d) | - | TBD | - | PCS 1900 | | |
| | 1.930 - 1.990(a) | - | TBD | - | GSM 1900 | | |
| | 1.930 - 1.990(b) | - | TBD | - | CDMA 1900 | | |
| | 2.110 - 2.170(b) | - | TBD | - | W-CDMA 2000 | | |
| | 2.110 - 2.170(e) | - | TBD | - | W-CDMA 2000 | | |

(a) Integrated in 200kHz bandwidth and then normalised to 1Hz bandwidth

(b) Integrated in 1.2MHz bandwidth and then normalised to 1Hz bandwidth

(c) Integrated in 1MHz bandwidth and then normalised to 1Hz bandwidth

(d) Integrated in 30kHz bandwidth and then normalised to 1Hz bandwidth

(e) Integrated in 5MHz bandwidth and then normalised to 1Hz bandwidth

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5.1.2 Receiver

| Radio Characteristics | | VDD = 1.8V | | | Temperature = +20°C | |
|--|-----------------|-------------|----------|------------|-------------------------|--------|
| | Frequency (GHz) | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.1% BER for all packet types | 2.402 | - | -87.0 | -83.0 | ≤ -70 | dBm |
| | 2.441 | - | -88.0 | -84.0 | | |
| | 2.480 | - | -87.5 | -83.5 | | |
| Maximum received signal at 0.1% BER | -20.0 | ≥ -10 | - | ≤ -20 | | dBm |
| | Frequency (MHz) | Min | Typ | Max | Bluetooth Specification | Unit |
| Continuous power required to block Bluetooth reception (for input power of -67dBm with 0.1% BER) measured at the unbalanced port of the balun. | 30-2000 | -10 | ≥ 0 | - | ≤ -10 | dBm |
| | 2000-2400 | -27 | -15 | - | ≤ -27 | |
| | 2500-3000 | -27 | -15 | - | ≤ -27 | |
| C/I co-channel | | | 7 | 11 | ≤ 11 | dB |
| Adjacent channel selectivity C/I $F = F_0 + 1\text{MHz}$ (a) (b) | | - | 4 | 0 | ≤ 0 | dB |
| Adjacent channel selectivity C/I $F = F_0 - 1\text{MHz}$ | | - | -3 | 0 | ≤ 0 | dB |
| Adjacent channel selectivity C/I $F = F_0 + 2\text{MHz}$ | | - | -45 | -30 | ≤ -30 | dB |
| Adjacent channel selectivity C/I $F = F_0 - 2\text{MHz}$ | | - | -23 | -20 | ≤ -20 | dB |
| Adjacent channel selectivity C/I $F = F_0 + 3\text{MHz}$ | | - | -48 | -40 | ≤ -40 | dB |
| Adjacent channel selectivity C/I $F = F_0 - 5\text{MHz}$ | | - | -48 | -40 | ≤ -40 | dB |
| Adjacent channel selectivity C/I $F = F_{\text{Image}}$ | | - | -22 | -9 | ≤ -9 | dB |
| Maximum level of intermodulation interferers ^(c) | -39 | -30 | - | ≥ -39 | | dBm |
| Spurious output level ^(d) | - | ≤ -130 | - | - | | dBm/Hz |

- (a) Up to five exceptions are allowed in v2.0+EDR of the Bluetooth specification. BlueCore4-Audio ROM is guaranteed to meet the C/I performance as specified by the Bluetooth specification v2.0+EDR.
- (b) Measured at $F = 2441\text{MHz}$
- (c) Measured at $f_1 - f_2 = 5\text{MHz}$. Measurement is performed in accordance with Bluetooth RF test RCV/CA/05/c., i.e., wanted signal at -64dBm .
- (d) Measured at unbalanced port of the balun. Integrated in 100kHz bandwidth and normalised to 1Hz. Actual figure is typically below -130dBm/Hz except for peaks of -65dbm at 1600MHz , -60dBm inband at 2.4GHz and -65dBm at 3.2GHz .

5.2 Temperature -40°C

5.2.1 Transmitter

| Radio Characteristics | VDD = 1.8V | | | Temperature = -40°C | |
|---|------------|------|------|------------------------------------|----------|
| | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | 2.8 | 6.8 | - | -6 to +4 ^(b) | dBm |
| RF power control range | 25 | 35 | - | ≥16 | dB |
| RF power range control resolution | - | 0.5 | - | - | dB |
| 20dB bandwidth for modulated carrier | - | 780 | 1000 | ≤1000 | kHz |
| Adjacent channel transmit power $F = F_0 \pm 2\text{MHz}$ ^{(c) (d)} | - | -40 | -20 | ≤-20 | dBm |
| Adjacent channel transmit power $F = F_0 \pm 3\text{MHz}$ | - | -45 | -40 | ≤-40 | dBm |
| $\Delta f_{1\text{avg}}$ Maximum Modulation | 140 | 164 | 175 | 140< $\Delta f_{1\text{avg}}$ <175 | kHz |
| $\Delta f_{2\text{max}}$ Minimum Modulation | 115 | 150 | - | ≥115 | kHz |
| $\Delta f_{2\text{avg}}/\Delta f_{1\text{avg}}$ | 0.80 | 0.97 | - | ≥0.80 | - |
| Initial carrier frequency tolerance | -30 | 10 | 30 | ±75 | kHz |
| Drift Rate | - | 7 | 20 | ≤20 | kHz/50μs |
| Drift (single slot packet) | - | 7 | 25 | ≤25 | kHz |
| Drift (five slot packet) | - | 10 | 40 | ≤40 | kHz |

(a) BlueCore4-Audio ROM firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits

(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification

(c) Measured at $F_0 = 2441\text{MHz}$

(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification

5.2.2 Receiver

| Radio Characteristics | VDD = 1.8V | | | Temperature = -40°C | | |
|---|-----------------|--------|-------|---------------------|-------------------------|------|
| | Frequency (GHz) | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.1% BER for all packet types | 2.402 | - | -88.2 | -84.2 | ≤-70 | dBm |
| | 2.441 | - | -89.0 | -85.0 | | |
| | 2.480 | - | -89.0 | -85.0 | | |
| Maximum received signal at 0.1% BER | -20.0 | ≥-10.0 | - | ≥-20 | | dBm |

5.3 Temperature -25°C

5.3.1 Transmitter

| Radio Characteristics | VDD = 1.8V | | | Temperature = -25°C | |
|---|------------|------|------|------------------------------------|----------|
| | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | 2.4 | 6.4 | - | -6 to +4 ^(b) | dBm |
| RF power control range | 25 | 35 | - | ≥16 | dB |
| RF power range control resolution | - | 0.5 | - | - | dB |
| 20dB bandwidth for modulated carrier | - | 780 | 1000 | ≤1000 | kHz |
| Adjacent channel transmit power $F = F_0 \pm 2\text{MHz}$ ^{(c) (d)} | - | -40 | -20 | ≤-20 | dBm |
| Adjacent channel transmit power $F = F_0 \pm 3\text{MHz}$ | - | -44 | -40 | ≤-40 | dBm |
| $\Delta f_{1\text{avg}}$ Maximum Modulation | 140 | 164 | 175 | 140< $\Delta f_{1\text{avg}}$ <175 | kHz |
| $\Delta f_{2\text{max}}$ Minimum Modulation | 115 | 152 | - | ≥115 | kHz |
| $\Delta f_{2\text{avg}}/\Delta f_{1\text{avg}}$ | 0.80 | 0.98 | - | ≥0.80 | - |
| Initial carrier frequency tolerance | -35 | 5 | 35 | ±75 | kHz |
| Drift Rate | - | 7 | 20 | ≤20 | kHz/50μs |
| Drift (single slot packet) | - | 7 | 25 | ≤25 | kHz |
| Drift (five slot packet) | - | 10 | 40 | ≤40 | kHz |

(a) BlueCore4-Audio ROM firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits

(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification

(c) Measured at $F_0 = 2441\text{MHz}$

(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification.

5.3.2 Receiver

| Radio Characteristics | VDD = 1.8V | | | Temperature = -25°C | | |
|---|-----------------|--------|-------|---------------------|-------------------------|------|
| | Frequency (GHz) | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.1% BER for all packet types | 2.402 | - | -88.0 | -84.0 | ≤-70 | dBm |
| | 2.441 | - | -89.0 | -85.0 | | |
| | 2.480 | - | -89.0 | -85.0 | | |
| Maximum received signal at 0.1% BER | -20.0 | ≥-10.0 | - | ≥-20 | | dBm |

5.4 Temperature +85°C

5.4.1 Transmitter

| Radio Characteristics | VDD = 1.8V | | | Temperature = +85°C | |
|---|------------|------|------|------------------------------------|----------|
| | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | -1.0 | 3 | - | -6 to +4 ^(b) | dBm |
| RF power control range | 25 | 35 | - | ≥16 | dB |
| RF power range control resolution | - | 0.5 | - | - | dB |
| 20dB bandwidth for modulated carrier | - | 850 | 1000 | ≤1000 | kHz |
| Adjacent channel transmit power $F = F_0 \pm 2\text{MHz}$ ^{(c) (d)} | - | -41 | -20 | ≤-20 | dBm |
| Adjacent channel transmit power $F = F_0 \pm 3\text{MHz}$ | - | -44 | -40 | ≤-40 | dBm |
| $\Delta f_{1\text{avg}}$ Maximum Modulation | 140 | 164 | 175 | 140< $\Delta f_{1\text{avg}}$ <175 | kHz |
| $\Delta f_{2\text{max}}$ Minimum Modulation | 115 | 149 | - | ≥115 | kHz |
| $\Delta f_{2\text{avg}}/\Delta f_{1\text{avg}}$ | 0.80 | 0.97 | - | ≥0.80 | - |
| Initial carrier frequency tolerance | -35 | 10 | 35 | ±75 | kHz |
| Drift Rate | - | 7 | 20 | ≤20 | kHz/50μs |
| Drift (single slot packet) | - | 10 | 25 | ≤25 | kHz |
| Drift (five slot packet) | - | 10 | 40 | ≤40 | kHz |

(a) BlueCore4-Audio ROM firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits.

(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification

(c) Measured at $F_0 = 2441\text{MHz}$

(d) Three exceptions are allowed in Bluetooth v2.0+EDR specification

5.4.2 Receiver

| Radio Characteristics | VDD = 1.8V | | | Temperature = +85°C | | |
|---|-----------------|--------|-------|---------------------|-------------------------|------|
| | Frequency (GHz) | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.1% BER for all packet types | 2.402 | - | -84.0 | -80.0 | ≤-70 | dBm |
| | 2.441 | - | -85.0 | -81.0 | | |
| | 2.480 | - | -84.0 | -80.0 | | |
| Maximum received signal at 0.1% BER | -20.0 | ≥-10.0 | - | ≥-20 | | dBm |

5.5 Temperature +105°C

5.5.1 Transmitter

| Radio Characteristics | VDD = 1.8V | | | Temperature = +105°C | |
|---|------------|------|------|----------------------------|----------|
| | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | -2.5 | 1.5 | - | -6 to +4 ^(b) | dBm |
| RF power control range | 25 | 35 | - | ≥16 | dB |
| RF power range control resolution | - | 0.5 | - | - | dB |
| 20dB bandwidth for modulated carrier | - | 850 | 1000 | ≤1000 | kHz |
| Adjacent channel transmit power $F = F_0 \pm 2\text{MHz}$ ^{(c) (d)} | - | -42 | -20 | ≤-20 | dBm |
| Adjacent channel transmit power $F = F_0 \pm 3\text{MHz}$ | - | -42 | -40 | ≤-40 | dBm |
| Δf _{avg} Maximum Modulation | 140 | 164 | 175 | 140<Δf _{avg} <175 | kHz |
| Δf _{2max} Minimum Modulation | 115 | 148 | - | ≥115 | kHz |
| Δf _{2avg} /Δf _{1avg} | 0.80 | 0.97 | - | ≥0.80 | - |
| Initial carrier frequency tolerance | -35.0 | 8 | 35.0 | ±75 | kHz |
| Drift Rate | - | 7 | 20 | ≤20 | kHz/50μs |
| Drift (single slot packet) | - | 10 | 25 | ≤25 | kHz |
| Drift (five slot packet) | - | 10 | 40 | ≤40 | kHz |

(a) BlueCore4-Audio ROM firmware maintains the transmit power to be within the Bluetooth v2.0+EDR specification limits.

(b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification

(c) Measured at $F_0 = 2441\text{MHz}$

(d) Three exceptions are allowed in the Bluetooth v2.0+EDR specification

5.5.2 Receiver

| Radio Characteristics | VDD = 1.8V | | | Temperature = +105°C | | |
|---|-----------------|--------|-------|----------------------|-------------------------|------|
| | Frequency (GHz) | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.1% BER for all packet types | 2.402 | - | -83.0 | -79.0 | ≤-70 | dBm |
| | 2.441 | - | -84.0 | -80.0 | | |
| | 2.480 | - | -83.0 | -79.0 | | |
| Maximum received signal at 0.1% BER | -20.0 | ≥-10.0 | - | ≥-20 | | dBm |

6 Radio Characteristics - Enhanced Data Rate

Important Note:

Results shown are referenced to the unbalanced port of the balun.

6.1 Temperature +20°C

6.1.1 Transmitter

| Radio Characteristics | VDD = 1.8V | Temperature = +20°C | | | | |
|---|-------------------------------|---------------------|-----|----------|----------------------------|------|
| | | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | -1.0 | 3.0 | - | - | -6 to +4 ^(b) | dBm |
| Relative transmit power ^(c) | -4 | -1.3 | - | - | -4 to +1 | dB |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_0 | -10 | 1.9 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_i | -75 | 2.1 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) $ w_0 + w_i $ | -75 | 3.4 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_0 | -10 | 1.5 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_i | -75 | 2.9 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) $ w_0 + w_i $ | -75 | 4.0 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7 | 20 | ≤20 | % |
| | 99% DEVM | - | 12 | 30 | ≤30 | % |
| | Peak DEVM | - | 17 | 35 | ≤35 | % |
| 8DPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7 | 13 | ≤13 | % |
| | 99% DEVM | - | 12 | 20 | ≤20 | % |
| | Peak DEVM | - | 17 | 25 | ≤25 | % |
| In-band spurious emissions ^(e) | $F > F_0 + 3\text{MHz}$ | - | -45 | -40 | ≤-40 | dBm |
| | $F < F_0 - 3\text{MHz}$ | - | -45 | -40 | ≤-40 | dBm |
| | $F = F_0 - 3\text{MHz}$ | - | -41 | -40 | ≤-40 | dBm |
| | $F = F_0 - 2\text{MHz}$ | - | -28 | -20 | ≤-20 | dBm |
| | $F = F_0 - 1\text{MHz}$ | - | -30 | -26 | ≤-26 | dB |
| | $F = F_0 + 1\text{MHz}$ | - | -30 | -26 | ≤-26 | dB |
| | $F = F_0 + 2\text{MHz}$ | - | -26 | -20 | ≤-20 | dBm |
| | $F = F_0 + 3\text{MHz}^{(e)}$ | - | -28 | - | ≤-40 | dBm |
| EDR Differential Phase Encoding | 99 | No Errors | - | ≥99 | - | % |

(a) BlueCore4-Audio ROM firmware maintains transmit power within Bluetooth v2.0 + EDR specification limits

(b) Class 2 RF transmit power range, Bluetooth h v2.0 + EDR specification

(c) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification

(d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.

(e) Bluetooth specification values are for 8DPSK. Three exceptions are allowed in Bluetooth v2.0 + EDR specification.

6.1.2 Receiver

| Radio Characteristics | VDD = 1.8V | Temperature = +20°C | | | | |
|---|---------------|---------------------|------------|-------|-------------------------|------|
| | Modulation | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.01% BER ^(a) | $\pi/4$ DQPSK | - | -85.5 | -81.5 | \leq 70 | dBm |
| | 8DPSK | - | -81.5 | -77.5 | \leq 70 | dBm |
| Maximum received signal at 0.1% BER ^(a) | $\pi/4$ DQPSK | -20 | \geq -10 | - | \geq -20 | dBm |
| | 8DPSK | -20 | \geq -10 | - | \geq -20 | dBm |
| C/I co-channel at 0.1% BER ^(a) | $\pi/4$ DQPSK | - | 8 | 13 | \leq +13 | dB |
| | 8DPSK | - | 18 | 21 | \leq +21 | dB |
| Adjacent channel selectivity C/I $F=F_0+1\text{MHz}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -10 | 0 | \leq 0 | dB |
| | 8DPSK | - | -5 | 5 | \leq +5 | dB |
| Adjacent channel selectivity C/I $F=F_0-1\text{MHz}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -10 | 0 | \leq 0 | dB |
| | 8DPSK | - | -6 | 5 | \leq +5 | dB |
| Adjacent channel selectivity C/I $F=F_0+2\text{MHz}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -40 | -30 | \leq -30 | dB |
| | 8DPSK | - | -41 | -25 | \leq -25 | dB |
| Adjacent channel selectivity C/I $F=F_0-2\text{MHz}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -23 | -20 | \leq -20 | dB |
| | 8DPSK | - | -22 | -13 | \leq -13 | dB |
| Adjacent channel selectivity C/I $F=F_0+3\text{MHz}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -45 | -40 | \leq -40 | dB |
| | 8DPSK | - | -45 | -33 | \leq -33 | dB |
| Adjacent channel selectivity C/I $F=F_0-5\text{MHz}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -45 | -40 | \leq -40 | dB |
| | 8DPSK | - | -45 | -33 | \leq -33 | dB |
| Adjacent channel selectivity C/I $F=F_{\text{Image}}$ ^{(a) (b) (c)} | $\pi/4$ DQPSK | - | -20 | -7 | \leq -7 | dB |
| | 8DPSK | - | -12 | 0 | \leq 0 | dB |

- (a) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification
- (b) Up to five exceptions are allowed in the Bluetooth v2.0 + EDR specification. BlueCore4-Audio ROM is guaranteed to meet the C/I performance as specified by the Bluetooth v2.0 + EDR
- (c) Measured at $F_0 = 2405\text{MHz}$, 2441MHz, 2477MHz

6.2 Temperature -40°C

6.2.1 Transmitter

| Radio Characteristics | VDD = 1.8V | Temperature = -40°C | | | | |
|---|---------------------------|---------------------|------|-----|----------------------------|------|
| | | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | 1.0 | 5.0 | - | - | -6 to +4 ^(b) | dBm |
| Relative transmit power ^(c) | -4.0 | -1.6 | 1 | - | -4 to +1 | dB |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_0 | -10 | 2.0 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_i | -75 | 12 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) $ w_0+w_i $ | -75 | 13 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_0 | -10 | 2 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_i | -75 | 12 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) $ w_0+w_i $ | -75 | 13 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7 | 20 | ≤20 | % |
| | 99% DEVM | - | 12 | 30 | ≤30 | % |
| | Peak DEVM | - | 15 | 35 | ≤35 | % |
| 8DPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7 | 13 | ≤13 | % |
| | 99% DEVM | - | 12 | 20 | ≤20 | % |
| | Peak DEVM | - | 18 | 25 | ≤25 | % |
| In-band spurious emissions ^(e) | $F>F_0+3\text{MHz}$ | - | <-45 | -40 | ≤-40 | dBm |
| | $F<F_0-3\text{MHz}$ | - | <-45 | -40 | ≤-40 | dBm |
| | $F=F_0-3\text{MHz}^{(e)}$ | - | -39 | -40 | ≤-40 | dBm |
| | $F=F_0-2\text{MHz}$ | - | -25 | -20 | ≤-20 | dBm |
| | $F=F_0-1\text{MHz}$ | - | -30 | -26 | ≤-26 | dB |
| | $F=F_0+1\text{MHz}$ | - | -30 | -26 | ≤-26 | dB |
| | $F=F_0+2\text{MHz}$ | - | -24 | -20 | ≤-20 | dBm |
| | $F=F_0+3\text{MHz}^{(e)}$ | - | -26 | - | ≤-40 | dBm |
| EDR Differential Phase Encoding | 99 | No Errors | - | - | ≥99 | % |

- (a) BlueCore4-Audio ROM firmware maintains transmit power within Bluetooth v2.0+EDR specification limits
- (b) Class 2 RF transmit power range, Bluetooth v2.0+EDR specification
- (c) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification
- (d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
- (e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.2.2 Receiver

| Radio Characteristics | VDD = 1.8V | Temperature = -40°C | | | | |
|--|---------------|---------------------|------------|-------|-------------------------|------|
| | Modulation | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.01% BER ^(a) | $\pi/4$ DQPSK | - | -91.0 | -87.0 | \leq 70 | dBm |
| | 8DPSK | - | -84.0 | -80.0 | \leq 70 | dBm |
| Maximum received signal at 0.1% BER ^(a) | $\pi/4$ DQPSK | -20 | \geq -10 | - | \leq -20 | dBm |
| | 8DPSK | -20 | \geq -10 | - | \leq -20 | dBm |

(a) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification

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6.3 Temperature -25°C

6.3.1 Transmitter

| Radio Characteristics | VDD = 1.8V | Temperature = -25°C | | | | |
|---|---------------------------|---------------------|------|-----|----------------------------|------|
| | | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | 0 | 4.0 | - | - | -6 to +4 ^(b) | dBm |
| Relative transmit power ^(c) | -4 | -1.6 | 1 | - | -4 to +1 | dB |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_0 | -10 | 1.8 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_i | -75 | 1.2 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) $ w_0+w_i $ | -75 | 1.5 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_0 | -10 | 2.1 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_i | -75 | 1.0 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) $ w_0+w_i $ | -75 | 1.5 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7.0 | 20 | ≤20 | % |
| | 99% DEVM | - | 12 | 30 | ≤30 | % |
| | Peak DEVM | - | 16.0 | 35 | ≤35 | % |
| 8DPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7.0 | 13 | ≤13 | % |
| | 99% DEVM | - | 12 | 20 | ≤20 | % |
| | Peak DEVM | - | 16.0 | 25 | ≤25 | % |
| In-band spurious emissions ^(e) | $F>F_0+3\text{MHz}$ | - | <-45 | -40 | ≤-40 | dBm |
| | $F<F_0-3\text{MHz}$ | - | <-45 | -40 | ≤-40 | dBm |
| | $F=F_0-3\text{MHz}$ | - | -40 | -40 | ≤-40 | dBm |
| | $F=F_0-2\text{MHz}$ | - | -28 | -20 | ≤-20 | dBm |
| | $F=F_0-1\text{MHz}$ | - | -31 | -26 | ≤-26 | dB |
| | $F=F_0+1\text{MHz}$ | - | -31 | -26 | ≤-26 | dB |
| | $F=F_0+2\text{MHz}$ | - | -25 | -20 | ≤-20 | dBm |
| | $F=F_0+3\text{MHz}^{(e)}$ | - | -27 | - | ≤-40 | dBm |
| EDR Differential Phase Encoding | 99 | No Errors | - | - | ≥99 | % |

- (a) BlueCore4-Audio ROM firmware maintains transmit power within Bluetooth v2.0 + EDR specification limits
- (b) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification
- (c) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification
- (d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
- (e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.3.2 Receiver

| Radio Characteristics | VDD = 1.8V | Temperature = -25°C | | | | |
|--|---------------|---------------------|------------|-------|-------------------------|------|
| | Modulation | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.01% BER ^(a) | $\pi/4$ DQPSK | - | -91.0 | -87.0 | \leq 70 | dBm |
| | 8DPSK | - | -83.0 | -79.0 | \leq 70 | dBm |
| Maximum received signal at 0.1% BER ^(a) | $\pi/4$ DQPSK | -20 | \geq -10 | - | \leq 20 | dBm |
| | 8DPSK | -20 | \geq -10 | - | \leq 20 | dBm |

(a) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification

6.4 Temperature +85°C

6.4.1 Transmitter

| Radio Characteristics | VDD = 1.8V | Temperature = +85°C | | | | |
|---|---------------------------|---------------------|------|-----|----------------------------|------|
| | | Min | Typ | Max | Bluetooth Specification | Unit |
| Maximum RF transmit power ^(a) | -2.0 | 2.0 | - | - | -6 to +4 ^(b) | dBm |
| Relative transmit power ^(c) | -4 | -1.2 | 1 | - | -4 to +1 | dB |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_0 | -10 | 1.5 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) w_i | -75 | 1.0 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK max carrier frequency stability ^(c) $ w_0+w_i $ | -75 | 1.8 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_0 | -10 | 1.5 | 10 | - | $\leq\pm10$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) w_i | -75 | 1.0 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| 8DPSK max carrier frequency stability ^(c) $ w_0+w_i $ | -75 | 1.6 | 75 | - | $\leq\pm75$ for all blocks | kHz |
| $\pi/4$ DQPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7 | 20 | ≤20 | % |
| | 99% DEVM | - | 13 | 30 | ≤30 | % |
| | Peak DEVM | - | 18 | 35 | ≤35 | % |
| 8DPSK Modulation Accuracy ^{(c) (d)} | RMS DEVM | - | 7 | 13 | ≤13 | % |
| | 99% DEVM | - | 13 | 20 | ≤20 | % |
| | Peak DEVM | - | 18 | 25 | ≤25 | % |
| In-band spurious emissions ^(e) | $F>F_0+3\text{MHz}$ | - | <-45 | -40 | ≤-40 | dBm |
| | $F<F_0-3\text{MHz}$ | - | <-45 | -40 | ≤-40 | dBm |
| | $F=F_0-3\text{MHz}$ | - | -42 | -40 | ≤-40 | dBm |
| | $F=F_0-2\text{MHz}$ | - | -26 | -20 | ≤-20 | dBm |
| | $F=F_0-1\text{MHz}$ | - | -29 | -26 | ≤-26 | dB |
| | $F=F_0+1\text{MHz}$ | - | -31 | -26 | ≤-26 | dB |
| | $F=F_0+2\text{MHz}$ | - | -26 | -20 | ≤-20 | dBm |
| | $F=F_0+3\text{MHz}^{(e)}$ | - | -29 | - | ≤-40 | dBm |
| EDR Differential Phase Encoding | 99 | No Errors | - | - | ≥99 | % |

- (a) BlueCore4-Audio ROM firmware maintains transmit power within Bluetooth v2.0 + EDR specification limits
- (b) Class 2 RF transmit power range, Bluetooth v2.0 + EDR specification
- (c) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification
- (d) Modulation accuracy utilises differential error vector magnitude (DEVM) with tracking of the frequency drift.
- (e) The Bluetooth specification values are for 8DPSK. Up to three exceptions are allowed in the Bluetooth v2.0 + EDR specification.

6.4.2 Receiver

| Radio Characteristics | VDD = 1.8V | Temperature = +85°C | | | | |
|--|---------------|---------------------|------------|-------|-------------------------|------|
| | Modulation | Min | Typ | Max | Bluetooth Specification | Unit |
| Sensitivity at 0.01% BER ^(a) | $\pi/4$ DQPSK | - | -86.0 | -82.0 | \leq 70 | dBm |
| | 8DPSK | - | -79.0 | -75.0 | \leq 70 | dBm |
| Maximum received signal at 0.1% BER ^(a) | $\pi/4$ DQPSK | -20 | \geq -10 | - | \leq -20 | dBm |
| | 8DPSK | -20 | \geq -10 | - | \leq -20 | dBm |

(a) Measurements methods are in accordance with the Bluetooth v2.0 + EDR specification

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7 Device Diagram

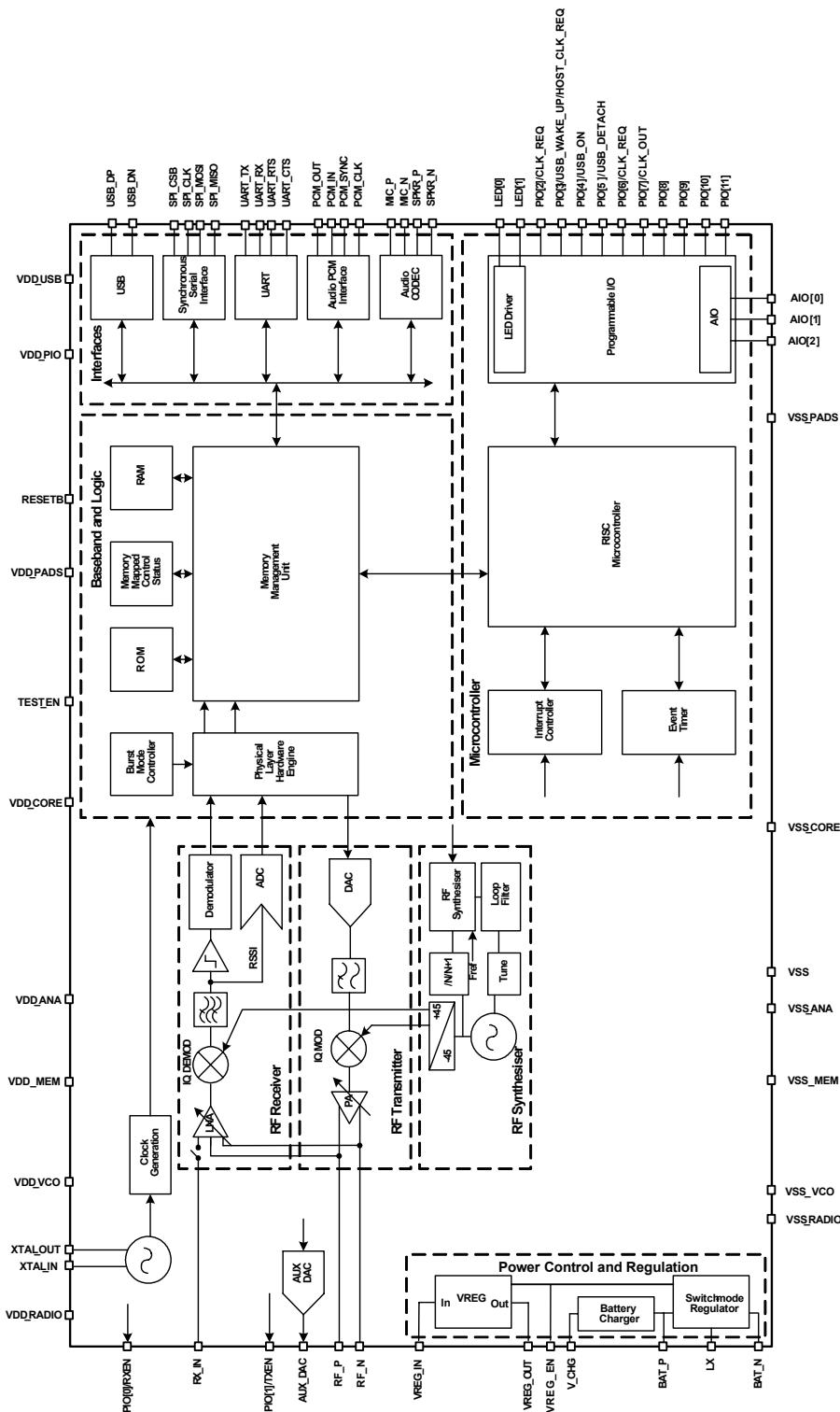


Figure 7.1: BlueCore4-Audio ROM Device Diagram

8 Description of Functional Blocks

8.1 RF Receiver

The receiver features a near-zero Intermediate Frequency (IF) architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the radio to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitised. The use of a digital Frequency Shift Keying (FSK) discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-Audio ROM to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, an ADC is used to digitise the IF received signal.

8.1.1 Low Noise Amplifier

The LNA can be configured to operate in single-ended or differential mode. Single-ended mode is used for Class 1 Bluetooth operation; differential mode is used for Class 2 operation.

8.1.2 Analogue to Digital Converter

The Analogue to Digital Converter (ADC) is used to implement fast Automatic Gain Control (AGC). The ADC samples the Received Signal Strength Indicator (RSSI) voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

8.2 RF Transmitter

8.2.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

8.2.2 Power Amplifier

The internal Power Amplifier (PA) has a maximum output power of +6dBm. This allows BlueCore4-Audio ROM to be used in Class 2 and Class 3 radios without an external RF PA. Support for transmit power control allows a simple implementation for Class 1 with an external RF PA.

8.3 RF Synthesiser

The radio synthesiser is fully integrated onto the die with no requirement for an external Voltage Controlled Oscillator (VCO) screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.0 + EDR specification.

8.4 Switch-Mode Regulator

BlueCore4-Audio ROM contains a high efficiency step-down switch mode 1.8V regulator, which can be used to power the complete chip from a single Lithium Ion/Polymer battery (or other external voltage source). The circuit has only two external passive filter components and has an internal PID feedback for very low supply ripple.

8.5 Linear Regulator

As an alternative, BlueCore4-Audio ROM also contains a 1.8V linear regulator which can be used to power the complete chip. This is less efficient than the switch-mode regulator, but requires less space for external components and can run at lower input voltages. If the switch mode regulator is used to power the chip, the linear regulator can be used to provide an internal low noise bias circuit for a microphone.

8.6 Battery Charger

BlueCore4-Audio ROM contains a fully integrated battery charger circuit, suitable for charging a Lithium Ion/Polymer battery. The circuit requires no external components.

Important Note:

See section 10.11.7 for Important Notes on Lithium Ion/Polymer battery safety.

8.7 Clock Input and Generation

The reference clock for the system is generated from a TCXO or crystal input between 8MHz and 40MHz. All internal reference clocks are generated using a phase locked loop, which is locked to the external reference frequency.

8.8 Baseband and Logic

8.8.1 Memory Management Unit

The Memory Management Unit (MMU) provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available Random Access Memory (RAM) and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

8.8.2 Burst Mode Controller

During radio transmission the Burst Mode Controller (BMC) constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During radio reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

8.8.3 Physical Layer Hardware Engine DSP

Dedicated logic is used to perform the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

The following voice data translations and operations are performed by firmware:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/Continuously Variable Slope Delta (CVSD) (over the air)
- Voice interpolation for lost packets
- Rate mismatches

The hardware supports all optional and mandatory features of Bluetooth v2.0 + EDR including AFH and eSCO.

8.8.4 System RAM

48Kbytes of on-chip RAM is provided to support the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general purpose memory required by the Bluetooth stack.

8.8.5 ROM

6Mbits of internal ROM is available on the . The ROM memory is provided for system firmware and the DSP co-processor code implementation.

8.8.6 External FLASH

External FLASH pads are available for stacked/external FLASH package variants

8.8.7 USB

This is a full speed Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-Audio ROM acts as a USB peripheral, responding to requests from a master host controller such as a PC.

8.8.8 Synchronous Serial Interface

8.8.9 UART

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

8.9 Microcontroller

The microcontroller (MCU), interrupt controller and event timer run the Bluetooth software stack and control the radio and host interfaces. A 16-bit reduced instruction set computer (RISC) microcontroller is used for low power consumption and efficient use of memory.

8.9.1 Programmable I/O

BlueCore4-Audio ROM has a total of 15 (12 digital and 3 analogue) programmable I/O terminals. These are controlled by firmware running on the device.

8.9.2 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded voice data over Bluetooth. It also contains support for PCM master CODECs that require an external system clock. The interface shares the same pins as the digital audio interface.

8.9.3 Audio CODEC

BlueCore4-Audio ROM has a 15-bit Audio CODEC that has a 8kHz sampling frequency. This has been designed for use in voice applications such as headsets and hands-free kits. The CODEC has integrated input/output amplifiers capable of driving a microphone and speaker with minimum external components.

8.9.4 LED Driver

Two LED output pads are provided to control LED indicators. The pads are open drain pull-downs, controlled by firmware running on the device. LED[0] is also hard wired to indicate battery charging.

9 CSR Bluetooth Software Stacks

BlueCore4-Audio ROM is supplied with Bluetooth v2.0 + EDR compliant stack firmware, which runs on the internal RISC microcontroller.

The BlueCore4-Audio ROM software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC microcontroller and an external host processor (if any). The upper layers of the Bluetooth stack (above HCI) can be run either on-chip or on the host processor.

9.1 BlueCore HCI Stack

Figure 9.1: BlueCore HCI Stack

In the implementation shown in the internal processor runs the Bluetooth stack up to the Host Controller Interface (HCI). The Host processor must provide all upper layers including the application.

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9.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

Bluetooth v2.0 + EDR mandatory functionality:

- Adaptive frequency hopping (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

Optional Bluetooth v2.0 + EDR functionality supported:

- Adaptive Frequency Hopping (AFH) as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- Extended SCO (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.0 + EDR specification.

- Bluetooth components:
 - Baseband (including LC)
 - LM
 - HCI
- Standard USB v1.1 and UART HCI Transport Layers
- All standard radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps⁽¹⁾
- Operation with up to seven active slaves⁽¹⁾
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7⁽²⁾
- Maximum number of simultaneous active SCO connections: 3⁽²⁾
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

The firmware's supported Bluetooth features are detailed in the standard Protocol Implementation Conformance Statement (PICS) documents, available from www.csr.com.

⁽¹⁾ This is the maximum allowed by Bluetooth v2.0 + EDR specification.
⁽²⁾ BlueCore4-Audio ROM supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.0 + EDR specification.

9.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BlueCore Serial Protocol (BCSP), a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BlueCore Command (BCCMD), provides:
 - Access to the chip's general-purpose PIO port
 - The negotiated effective encryption key length on established Bluetooth links
 - Access to the firmware's random number generator
 - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
 - Dynamic UART configuration
 - Radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of the chip's external pins. This is normally used to build a battery monitor, using either VM or host code
- A block of BCCMD commands provides access to the chip's Persistent Store configuration database (PS). The database sets the device's Bluetooth address, Class of Device, radio (transmit class) configuration, SCO routing, LM, USB and DFU constants, etc.
- A UART break condition can be used in three ways:
 1. Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
 2. Presenting a break condition at boot time can hold the chip in a low power state, preventing normal initialisation while the condition exists
 3. With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a Deep Sleep state.)
- The DFU standard has been extended with public/private key authentication, allowing manufacturers to control the firmware that can be loaded onto their Bluetooth modules
- A modified version of the DFU protocol allows firmware upgrade via the chip's UART
- A block of radio test or BIST commands allows direct control of the chip's radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Virtual Machine (VM). The firmware provides the VM environment in which to run application-specific code. Although the VM is mainly used with BlueLab and RFCOMM builds (alternative firmware builds providing L2CAP, SDP and RFCOMM), the VM can be used with this build to perform simple tasks such as flashing LEDs via the chip's PIO port.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the chip's single PCM port (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

9.2 BlueCore RFCOMM Stack

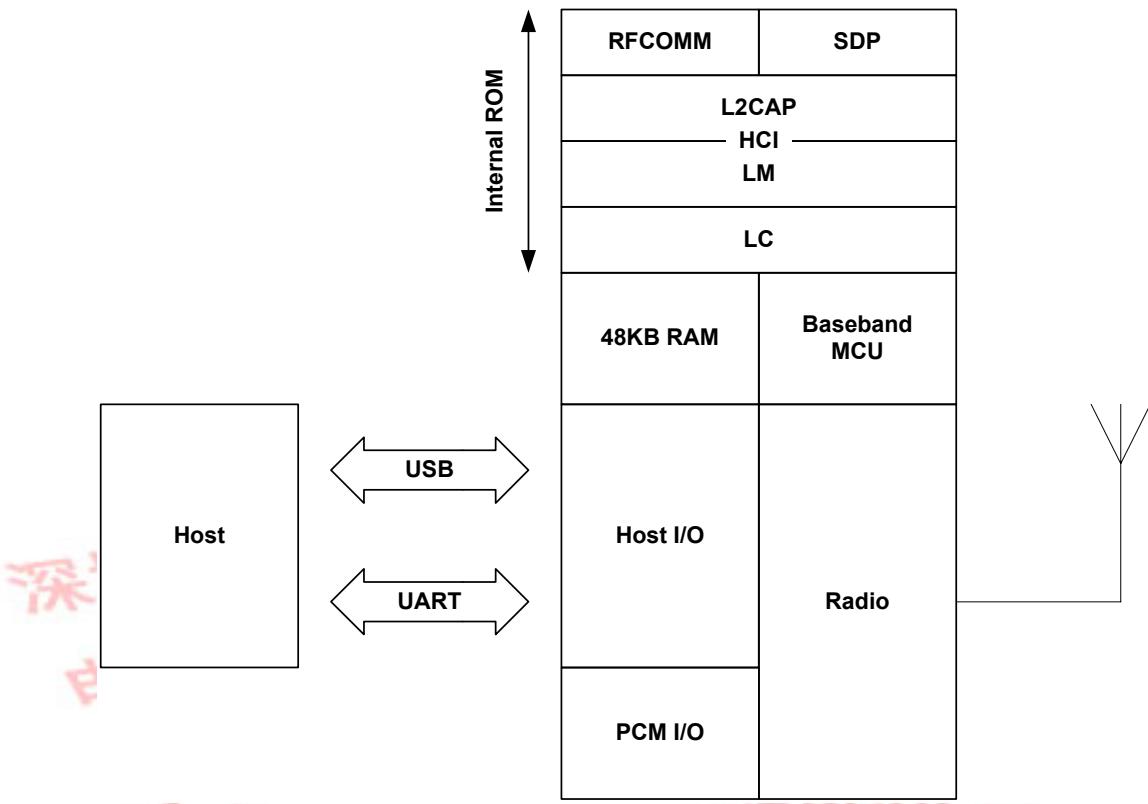


Figure 9.2: BlueCore RFCOMM Stack

In the version of the firmware, shown in Figure 9.2 the upper layers of the Bluetooth stack up to RFCOMM are run on-chip. This reduces host-side software and hardware requirements at the expense of some of the power and flexibility of the HCI only stack.

9.2.1 Key Features of the RFCOMM Stack

Interfaces to Host:

- RFCOMM, an RS-232 serial cable emulation protocol
- SDP, a service database look-up protocol

Connectivity:

- Maximum number of active slaves: three
- Maximum number of simultaneous active ACL connections: three
- Maximum number of simultaneous active SCO connections: three
- Data Rate: up to 350kbps⁽¹⁾

Security:

- Full support for all Bluetooth security features up to and including strong (128-bit) encryption.

Power Saving:

- Full support for all Bluetooth power saving modes (Park, Sniff and Hold).

Data Integrity:

- CQDDR increases the effective data rate in noisy environments.
- RSSI used to minimise interference to other radio devices using the ISM band.

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⁽¹⁾ The data rate is with respect to BlueCore4-Audio ROM with basic data rate packets.

9.3 BlueCore Virtual Machine Stack

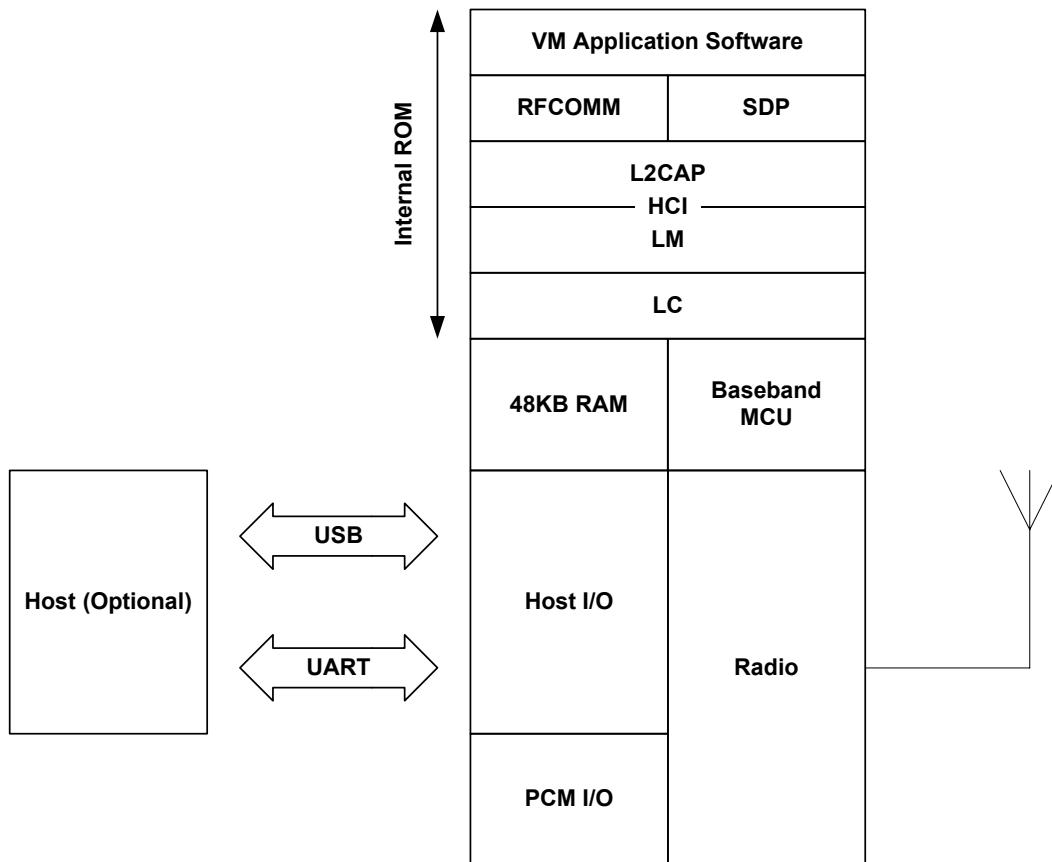


Figure 9.3: Virtual Machine

In Figure 9.3, this version of the stack firmware shown requires no host processor (but it can use a host processor for debugging, etc.). All software layers, including application software, run on the internal RISC processor in a protected user software execution environment known as a Virtual Machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab SDK supplied with the BlueLab Multimedia and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab SDK the user is able to develop applications such as a cordless handsfree kit or other profiles without the requirement of a host controller. BlueLab is supplied with example code including a full implementation of the handsfree profile.

Note:

Sample applications to control PIO lines can also be written with BlueLab SDK and the VM for the HCI stack.

9.4 Host-side Software

BlueCore4-Audio ROM can be ordered with companion host-side software:

- a full Windows 98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with the IC hardware described in this document.
- BCHS, a full host-side stack designed for modern ARM based mobile handsets together with the IC hardware described in this document.

9.5 BlueCore HID Stack

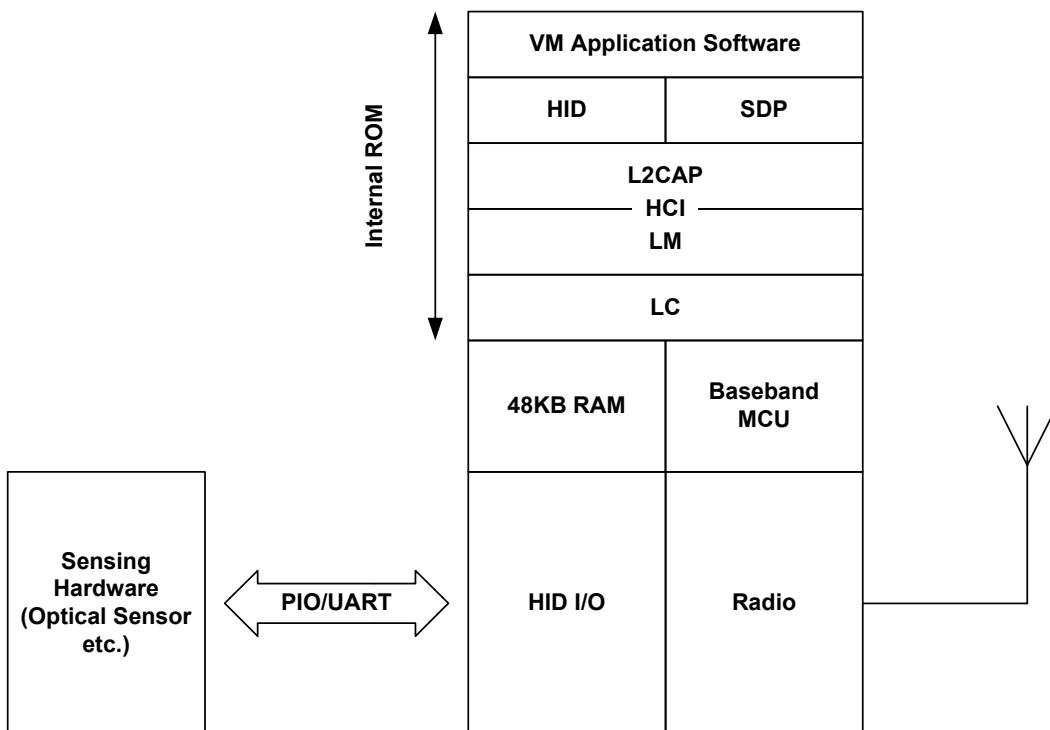


Figure 9.4: HID Stack

This version of the stack firmware requires no host processor. All software layers, including application software, run on the internal RISC microcontroller in a protected user software execution environment known as a virtual machine (VM).

The user may write custom application code to run on the BlueCore VM using BlueLab Professional SDK supplied with the BlueLab Professional and Casira development kits, available separately from CSR. This code will then execute alongside the main BlueCore firmware. The user is able to make calls to the BlueCore firmware for various operations.

The execution environment is structured so the user application does not adversely affect the main software routines, thus ensuring that the Bluetooth stack software component does not need re-qualification when the application is changed.

Using the VM and the BlueLab Professional SDK the user is able to develop Bluetooth HID devices such as an optical mouse or keyboard. The user is able to customise features such as power management and connect/reconnect behaviour.

The HID I/O component in the HID stack controls low latency data acquisition from external sensor hardware. With this component running in native code, it does not incur the overhead of the VM code interpreter. Supported external sensors include five mouse buttons, the Agilent ADNS-2030 optical sensor, quadrature scroll wheel, direct coupling to a keyboard matrix and a UART interface to custom hardware.

A reference schematic for implementing a three button, optical mouse with scroll wheel is available from CSR.

9.6 BCHS Software

BlueCore Embedded Host Software is designed to enable CSR customers to implement Bluetooth functionality into embedded products quickly, cheaply and with low risk.

BCHS is developed to work with CSR's family of BlueCore ICs. BCHS is intended for embedded products that have a host processor for running BCHS and the Bluetooth application, e.g., a mobile phone or a PDA. BCHS together with the BlueCore IC with embedded Bluetooth core stack (L2CAP, RFCOMM and SDP) is a complete Bluetooth system solution from RF to profiles.

BCHS includes most of the Bluetooth intelligence and gives the user a simple API. This makes it possible to develop a Bluetooth product without in-depth Bluetooth knowledge.

The BlueCore Embedded Host Software contains three elements:

- Example Drivers (BCSP and proxies)
- Bluetooth Profile Managers
- Example Applications

The profiles are qualified which makes the qualification of the final product very easy. BCHS is delivered with source code (ANSI C). BCHS also comes with example applications in ANSI C, which makes the process of writing the application easier.

9.7 Additional Software for Other Embedded Applications

When the upper layers of the Bluetooth protocol stack are run as firmware on BlueCore4-Audio ROM, a UART software driver is supplied that presents the L2CAP, RFCOMM and Service Discovery Protocol (SDP) APIs to higher Bluetooth stack layers running on the host. The code is provided as C source or object code.

9.8 CSR Development Systems

CSR's BlueLab Multimedia and Casira development kits are available to allow the evaluation of the BlueCore4-Audio ROM hardware and software, and as toolkits for developing on-chip and host software.

10 Device Terminal Descriptions

10.1 RF Ports

The BlueCore4-Audio ROM RX_IN terminal can be configured as either a single-ended or differential input. The operational mode is determined by setting the PS Key PSKEY_TXRX_PIO_CONTROL (0x20).

10.1.1 RF_P and RF_N

RF_P and RF_N form a complementary balanced pair. On transmit, their outputs are combined using a balun into the single-ended output required for the antenna. Similarly, on receive, their input signals are combined internally. Both terminals present similar complex impedances that require matching networks between them and the balun. Starting from the substrate (chip) side, the outputs can each be modelled as an ideal current source in parallel with a lossy resistance and a capacitor. The bond wire can be represented as series inductance.

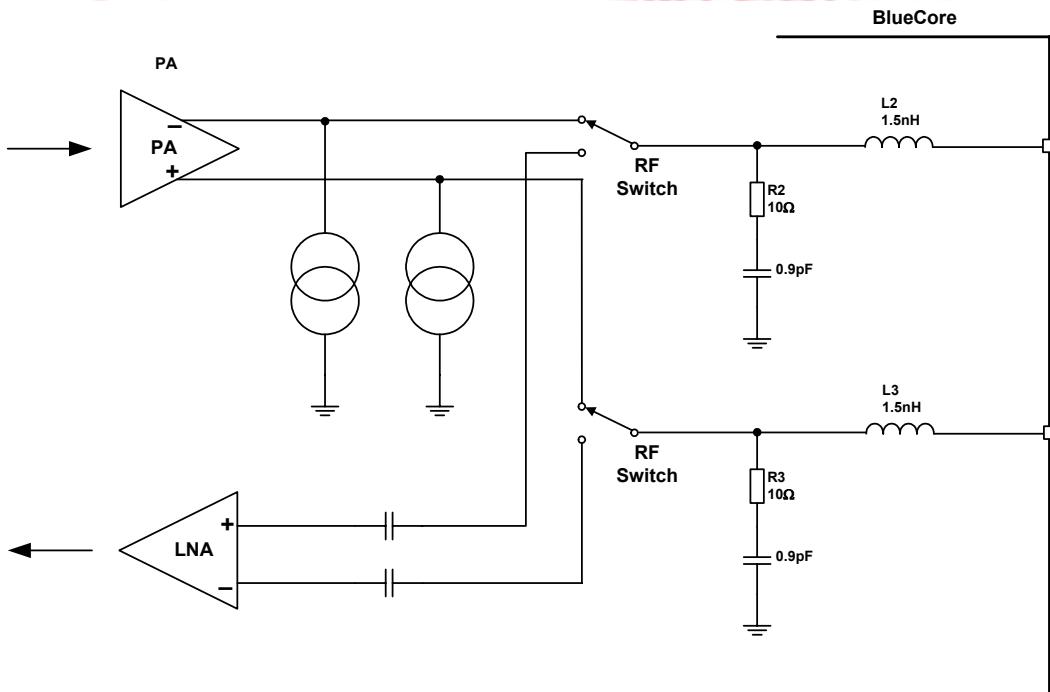


Figure 10.1: Circuit RF_P and RF_N

10.1.2 Single-Ended Input (RX_IN)

This is the single-ended RF input from the antenna. The input presents a complex impedance that requires a matching network between the terminal and the antenna. Starting from the substrate (chip) side, the input can be modelled as a lossy capacitor with the bond wire to the ball grid represented as a series inductance.

The terminal is DC blocked. The DC level must not exceed (VSS_RADIO -0.3V to VDD_RADIO + 0.3V).

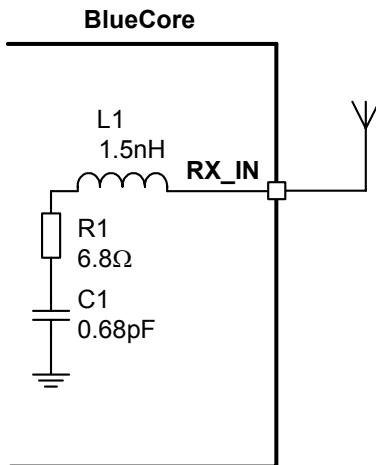


Figure 10.2: Circuit RX_IN

10.1.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) is used to control the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. The output voltage is given by:

$$V_{DAC} = \text{MIN}\left(3.3v \times \frac{\text{CNTRL_WORD}}{255}, (VDD_PIO - 0.3v)\right)$$

Equation 10.1: Output Voltage with Load Current $\leq 10\text{mA}$

for a load current $\leq 10\text{mA}$ (sourced from the device).

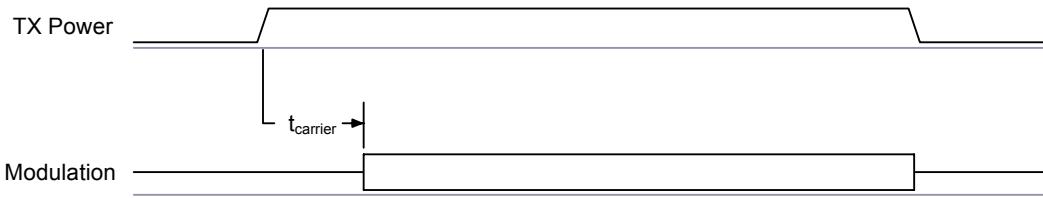
or

$$V_{DAC} = \text{MIN}\left(3.3v \times \frac{\text{CNTRL_WORD}}{255}, VDD_PIO\right)$$

Equation 10.2: Output Voltage with No Load Current

for no load current.

BlueCore4-Audio ROM enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.



Equation 10.3: Internal Power Ramping

The Persistent Store Key (PS Key) PSKEY_TX_GAINRAMP (0x1d), is used to control the delay (in units of μ s) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which gives the transmit circuitry time to fully settle to the correct frequency.

Bits[15:8] define a delay, $t_{carrier}$, (in units of μ s) between the end of the transmit power ramp and the start of modulation. In this period the carrier is transmitted, which aids interoperability with some other vendor equipment which is not strictly Bluetooth compliant.

10.1.4 Control of External RF Components

A PS Key TXRX_PIO_CONTROL (0x209) is used to control external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as Table 10.1 indicates.

| TXRX_PIO_CONTROL Value | AUX_DAC Use |
|------------------------|---|
| 0 | PIO[0], PIO[1], AUX_DAC not used to control RF. Power ramping is internal. |
| 1 | PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal. |
| 2 | PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external. |
| 3 | PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external. |
| 4 | PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal. |

Table 10.1: TXRX_PIO_CONTROL Values

10.2 External Reference Clock Input (XTAL_IN)

The BlueCore4-Audio ROM local oscillator and internal digital clocks are derived from the reference clock at the BlueCore4-Audio ROM XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT. The crystal mode is described in section 10.3.

10.2.1 External Mode

BlueCore4-Audio ROM can be configured to accept an external reference clock from another device (such as TCXO) at XTAL_IN by connecting XTAL_OUT to ground. The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion.

The external clock signal should meet the specifications in Table 10.2:

| | Min | Typ | Max |
|--------------------------------|-------------|-------|---------------------------------------|
| Frequency ^(a) | 7.5MHz | 16MHz | 40MHz |
| Duty cycle | 20:80 | 50:50 | 80:20 |
| Edge Jitter (At Zero Crossing) | - | - | 15ps rms |
| Signal Level | 400mV pk-pk | - | VDD_ANA ^(b) ^(c) |

Table 10.2: External Clock Specifications

(a) The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

(b) VDD_ANA is 1.8V nominal

(c) If the external clock is driven through a DC blocking capacitor, then maximum allowable amplitude is reduced from VDD_ANA to 800mV pk-pk.

10.2.2 XTAL_IN Impedance in External Mode

The impedance of the XTAL_IN will not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason it is recommended that a buffered clock input be used.

10.2.3 Clock Timing Accuracy

As Figure 10.3 indicates, the 250ppm timing accuracy on the external clock is required 7ms after the assertion of the system clock request line. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.0 + EDR specification. Radio activity may occur after 11ms, therefore, at this point the timing accuracy of the external clock source must be within 20ppm.

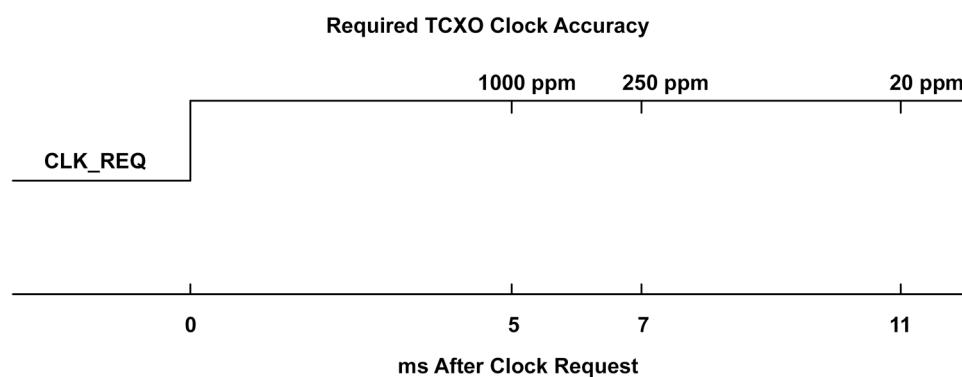


Figure 10.3: TCXO Clock Accuracy

10.2.4 Clock Start-Up Delay

BlueCore4-Audio ROM hardware incorporates an automatic delay after the assertion of the system clock request signal before running firmware. By default, the delay is 5 low-power oscillator (LPO) cycles. At a nominal LPO frequency of 1 kHz, this equates to 5 ms. This is suitable for most applications using an external clock source.

However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-Audio ROM provides a function that alters the system clock request signal to the period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is in units of LPO cycles from 1 to 31. Setting the key to zero gives a delay of 5 cycles, the default value.

The nominal frequency of the internal LPO is 1 kHz, however, the value varies somewhat between chips, so care should be taken to pick a suitable value. If an external slow clock at 32 kHz is supplied, this is divided by 32 before use.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-Audio ROM as low as possible. BlueCore4-Audio ROM consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

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10.2.5 Input Frequencies and PS Key Settings

BlueCore4-Audio ROM should be configured to operate with the chosen reference frequency. This is accomplished by setting the PS Key PSKEY_ANA_FREQ (0x1fe) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-Audio ROM is 26MHz.

The following CDMA/3G TCXO frequencies are also catered for: 7.68, 14.4, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

| Reference Crystal Frequency (MHz) | PSKEY_ANA_FREQ (0x1fe) (Units of 1kHz) |
|-----------------------------------|---|
| 7.68 | 7680 |
| 14.40 | 14400 |
| 15.36 | 15360 |
| 16.20 | 16200 |
| 16.80 | 16800 |
| 19.20 | 19200 |
| 19.44 | 19440 |
| 19.68 | 19680 |
| 19.80 | 19800 |
| 38.40 | 38400 |
| n x 250kHz | - |
| +26.00 Default | 26000 |

Table 10.3: PS Key Values for CDMA/3G Phone TCXO Frequencies

10.3 Crystal Oscillator (XTAL_IN, XTAL_OUT)

This section describes the crystal mode. See section 10.2 for the description of the external reference clock mode.

10.3.1 XTAL Mode

BlueCore4-Audio ROM contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator.

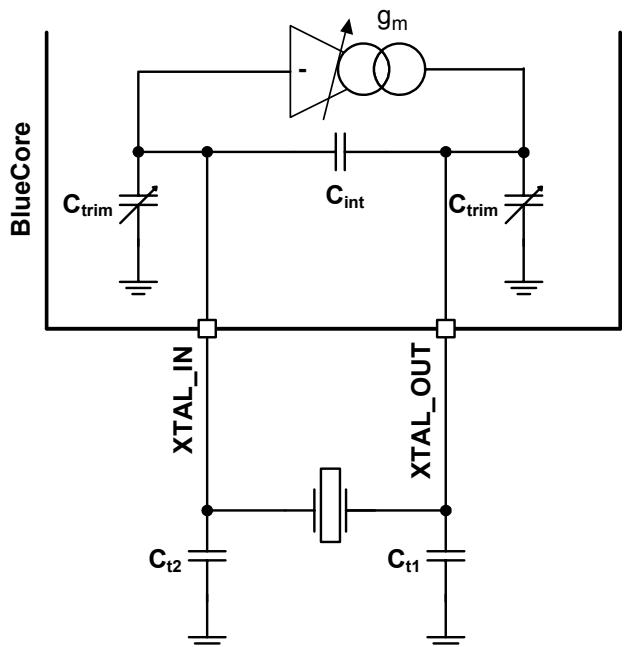


Figure 10.4: Crystal Driver Circuit

Figure 10.5 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

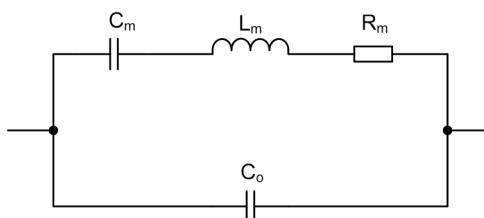


Figure 10.5: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-Audio ROM contains variable internal capacitors to provide a fine trim.

| | Min | Typ | Max |
|-------------------|------|-----------|-------|
| Frequency | 8MHz | 26MHz | 32MHz |
| Initial Tolerance | - | ±25ppm | - |
| Pullability | - | ±20ppm/pF | - |

Table 10.4: Crystal Specification

The BlueCore4-Audio ROM driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

10.3.2 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-Audio ROM provides some of this load with the capacitors C_{trim} and C_{int} . The remainder should be from the external capacitors labelled C_{t1} and C_{t2} . C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence, slew rate at XTAL_IN (to which all on-chip clocks are referred). Crystal load capacitance, C_l is calculated with Equation 10.4:

$$C_l = C_{int} + \frac{C_{trim}}{2} + \frac{C_{t1} \cdot C_{t2}}{C_{t1} + C_{t2}}$$

Equation 10.4: Load Capacitance

Where:

$C_{trim} = 3.4\text{pF}$ nominal (mid-range setting)

$C_{int} = 1.5\text{pF}$

Note:

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

10.3.3 Frequency Trim

BlueCore4-Audio ROM enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with on-chip trim capacitors, C_{trim} . The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (0x1f6). Its value is calculated thus:

$$C_{trim} = 110fF \times PSKEY_ANA_FTRIM$$

Equation 10.5: Trim Capacitance

There are two C_{trim} capacitors, which are both connected to ground. When viewed from the crystal terminals, they appear in series so each least significant bit (LSB) increment of frequency trim presents a load across the crystal of 55fF.

The frequency trim is described by Equation 10.6.

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 55 \times 10^{-3} (\text{ppm/LSB})$$

Equation 10.6: Frequency Trim

Where F_x is the crystal frequency and pullability is a crystal parameter with units of ppm/pF. Total trim range is 63 times the value above.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 10.7.

$$\frac{\partial(F_x)}{\partial(C)} = F_x \cdot \frac{C_m}{2(C_l + C_0)^2}$$

Equation 10.7: Pullability

Where:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 10.5.

Note:

It is a Bluetooth requirement that the frequency is always within ± 20 ppm. The trim range should be sufficient to pull the crystal within ± 5 ppm of the exact frequency. This leaves a margin of ± 15 ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ± 15 ppm is required.

10.3.4 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-Audio ROM uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 10.8:

$$g_m > \frac{3(2\pi F_x)^2 R_m ((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}{(C_{t1} + C_{trim})(C_{t2} + C_{trim})}$$

Equation 10.8: Transconductance Required for Oscillation

BlueCore4-Audio ROM guarantees a transconductance value of at least 2mA/V at maximum drive level.

Notes:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance, by setting the PS Key PSKEY_XTAL_LVL (0x241).

10.3.5 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-Audio ROM crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance may be calculated for it with the following formula in Equation 10.9:

$$R_{neg} > \frac{(C_{t1} + C_{trim})(C_{t2} + C_{trim})}{g_m (2\pi F_x)^2 ((C_0 + C_{int})(C_{t1} + C_{t2} + 2C_{trim}) + (C_{t1} + C_{trim})(C_{t2} + C_{trim}))^2}$$

Equation 10.9: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-Audio ROM driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

10.3.6 Crystal PS Key Settings

See tables in section 10.2.5.

10.3.7 Crystal Oscillator Characteristics

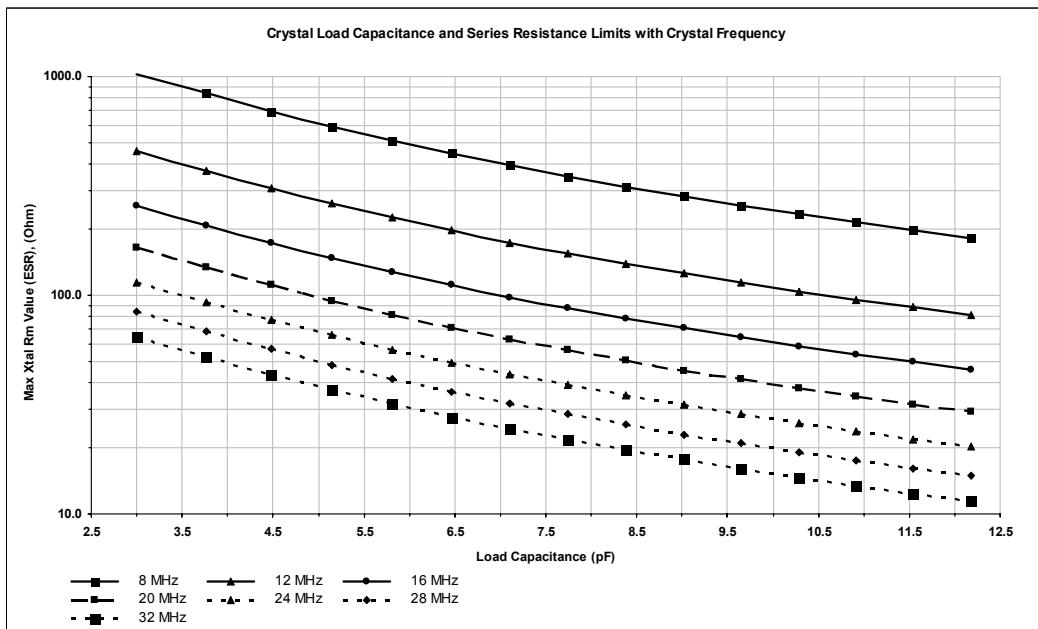


Figure 10.6: Crystal Load Capacitance and Series Resistance Limits with Crystal Frequency

Note:

Graph shows results for BlueCore4-Audio ROM crystal driver at maximum drive level.

Conditions:

$C_{trim} = 3.4\text{pF}$ centre value

Crystal $C_o = 2\text{pF}$

Transconductance setting = 2mA/V

Loop gain = 3

$C_{t1}/C_{t2} = 3$

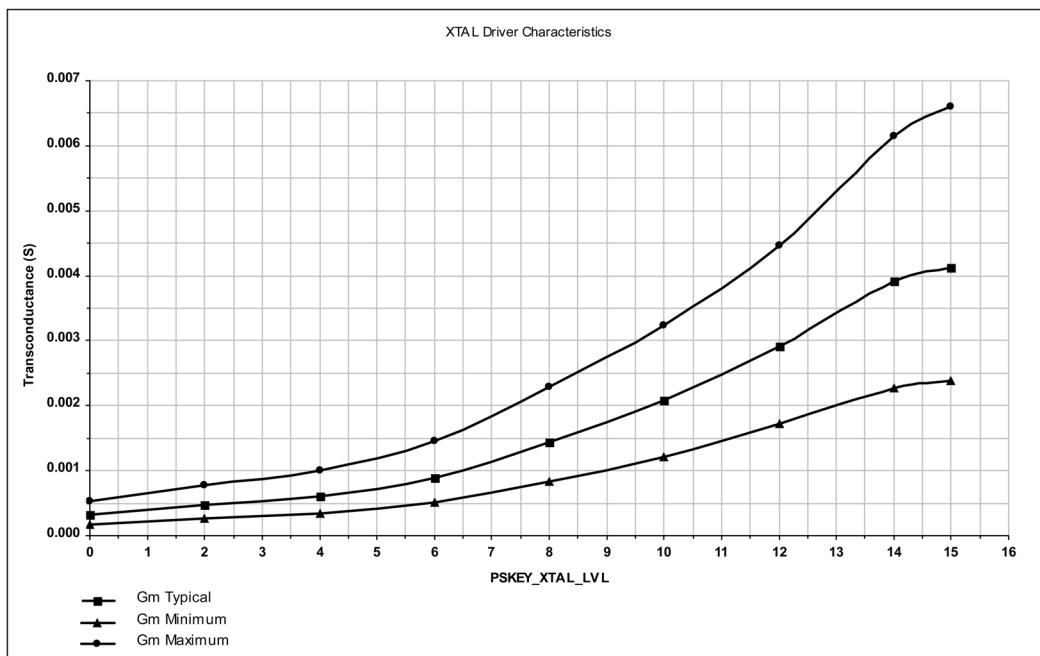


Figure 10.7: Crystal Driver Transconductance vs. Driver Level Register Setting

Note:

Drive level is set by PS Key PSKEY_XTAL_LVL (0x241).

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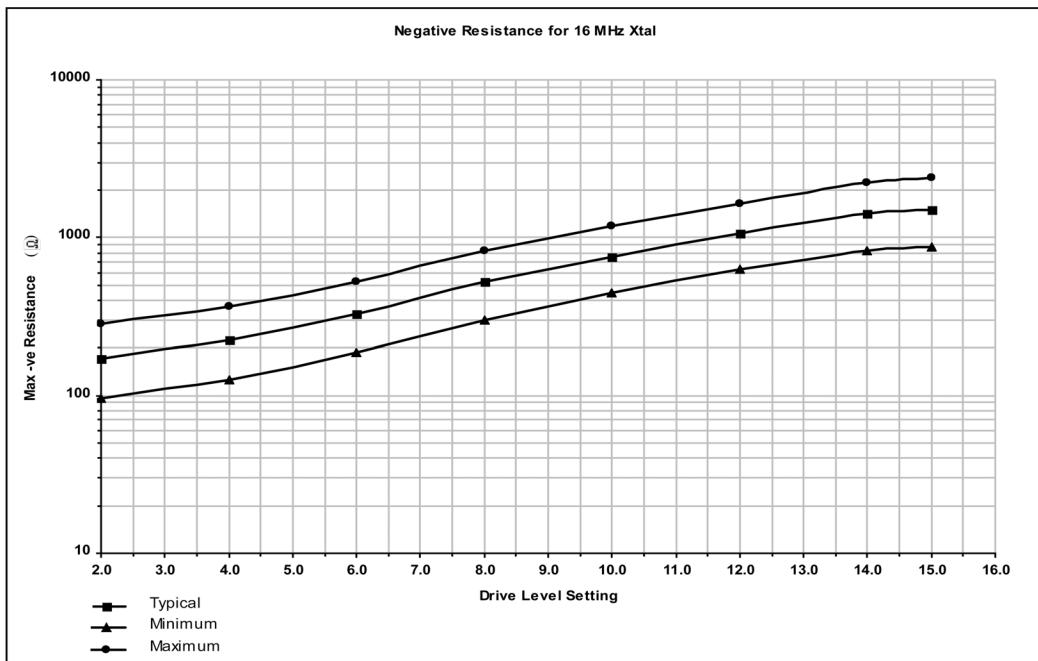


Figure 10.8: Crystal Driver Negative Resistance as a Function of Drive Level Setting

Crystal parameters:

Crystal frequency 16MHz (refer to your software build release note for supported frequencies).

Crystal $C_0 = 0.75\text{pF}$

Circuit parameters:

$C_{\text{trim}} = 8\text{pF}$, maximum value

$C_{t1}, C_{t2} = 5\text{pF}$ (3.9pF plus 1.1 pF stray)

(Crystal total load capacitance 8.5pF)

Note:

This is for a specific crystal and load capacitance.

10.4 UART Interface

This is a standard Universal Asynchronous Receiver Transmitter (UART) interface for communicating with other serial devices.

BlueCore4-Audio ROM UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.⁽¹⁾

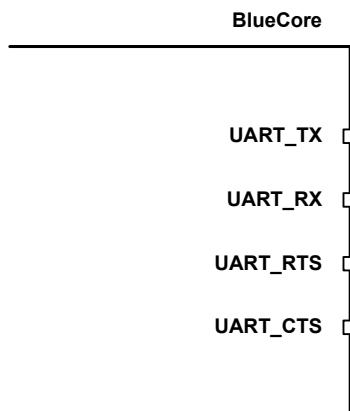


Figure 10.9: Universal Asynchronous Receiver

Four signals are used to implement the UART function, as shown in Figure 10.9. When BlueCore4-Audio ROM is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD_USB.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore4-Audio ROM software.

Note:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

| Parameter | Possible Values | |
|---------------------|-------------------|-------------------------------|
| Baud Rate | Minimum | 1200 baud ($\leq 2\%$ Error) |
| | | 9600 baud ($\leq 1\%$ Error) |
| | Maximum | 3M baud ($\leq 1\%$ Error) |
| Flow Control | RTS/CTS or None | |
| Parity | None, Odd or Even | |
| Number of Stop Bits | 1 or 2 | |
| Bits per Channel | 8 | |

Table 10.5: Possible UART Settings

The UART interface is capable of resetting BlueCore4-Audio ROM upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 10.10. If t_{BRK} is longer than the value, defined by the PS Key PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, BlueCore4-Audio ROM can emit a break character that may be used to wake the host.

(1) Uses RS232 protocol, but voltage levels are 0V to VDD_USB (requires external RS232 transceiver chip).

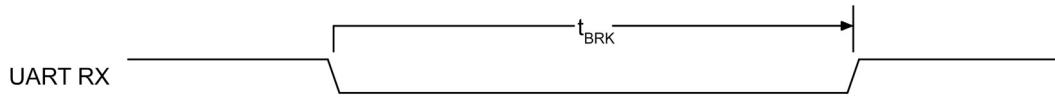


Figure 10.10: Break Signal

Note:

The DFU boot loader must be loaded into the Flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 10.6 shows a list of commonly used baud rates and their associated values for the PS Key PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 10.10.

$$\text{BaudRate} = \frac{\text{PSKEY_UART_BAUD_RATE}}{0.004096}$$

Equation 10.10: Baud Rate

| Baud Rate | Persistent Store Value | | Error |
|-----------|------------------------|-------|--------|
| | Hex | Dec | |
| 1200 | 0x0005 | 5 | 1.73% |
| 2400 | 0x000a | 10 | 1.73% |
| 4800 | 0x0014 | 20 | 1.73% |
| 9600 | 0x0027 | 39 | -0.82% |
| 19200 | 0x004f | 79 | 0.45% |
| 38400 | 0x009d | 157 | -0.18% |
| 57600 | 0x00ec | 236 | 0.03% |
| 76800 | 0x013b | 315 | 0.14% |
| 115200 | 0x01d8 | 472 | 0.03% |
| 230400 | 0x03b0 | 944 | 0.03% |
| 460800 | 0x075f | 1887 | -0.02% |
| 921600 | 0x0ebf | 3775 | 0.00% |
| 1382400 | 0x161e | 5662 | -0.01% |
| 1843200 | 0x1d7e | 7550 | 0.00% |
| 2764800 | 0x2c3d | 11325 | 0.00% |

Table 10.6: Standard Baud Rates

10.4.1 UART Bypass

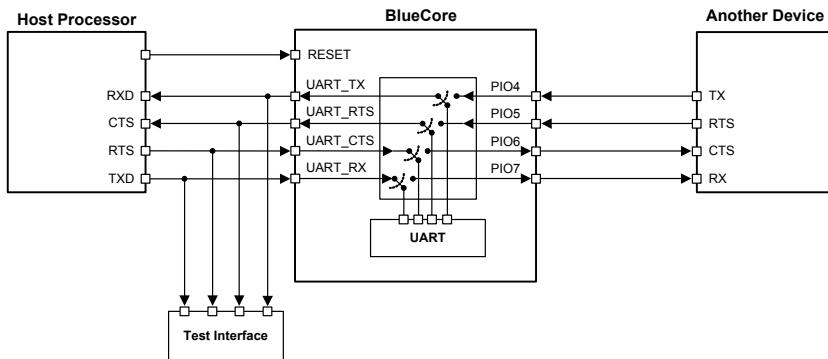


Figure 10.11: UART Bypass Architecture

10.4.2 UART Configuration While RESET is Active

The UART interface for BlueCore4-Audio ROM while the chip is being held in reset is tri-state. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tri-state when BlueCore4-Audio ROM reset is de-asserted and the firmware begins to run.

10.4.3 UART Bypass Mode

Alternatively, for devices that do not tri-state the UART bus, the UART bypass mode on BlueCore4-Audio ROM can be used. The default state of BlueCore4-Audio ROM after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore4-Audio ROM UART, thereby allowing communication to BlueCore4-Audio ROM via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.⁽¹⁾

In order to apply the UART bypass mode, a BCCMD command will be issued to BlueCore4-Audio ROM. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 10.11 indicates. Once the bypass mode has been invoked, BlueCore4-Audio ROM will enter the Deep Sleep state indefinitely.

In order to re-establish communication with BlueCore4-Audio ROM, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

10.4.4 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

⁽¹⁾ The range of the signalling level for the standard UART described in section 10.4 and the UART bypass may differ between CSR BlueCore devices, as the power supply configurations are chip dependent. For BlueCore4-Audio ROM, the standard UART is supplied by VDD_USB, so has signalling levels of 0V and VDD_USB. Whereas in the UART bypass mode, the signals appear on PIO[4:7] which are supplied by VDD_PADS, therefore the signalling levels are 0V and VDD_PADS.

10.5 USB Interface

This is a full speed (12Mbit/s) Universal Serial Bus (USB) interface for communicating with other compatible digital devices. BlueCore4-Audio ROM acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a master/slave oriented system (in common with other USB peripherals), BlueCore4-Audio ROM only supports USB Slave operation.

10.5.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the BlueCore4-Audio ROM, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

10.5.2 USB Pull-Up Resistor

BlueCore4-Audio ROM features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when BlueCore4-Audio ROM is ready to enumerate. It signals to the PC that it is a full speed (12Mbit/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a $15\text{k}\Omega \pm 5\%$ pull-down resistor (in the hub/host) when $\text{VDD_PADS}=3.1\text{V}$. This presents a Thevenin resistance to the host of at least 900Ω . Alternatively, an external $1.5\text{k}\Omega$ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PS Key PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

10.5.3 USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD_USB supply terminals must be an absolute minimum of 3.1V. CSR recommends 3.3V for optimal USB signal quality.

10.5.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to BlueCore4-Audio ROM via a resistor network (R_{vb1} and R_{vb2}), so BlueCore4-Audio ROM can detect when VBUS is powered up. BlueCore4-Audio ROM will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pull-up purposes. A $1.5K\Omega$ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in BlueCore is only suitable for bus-powered USB devices, e.g., dongles.

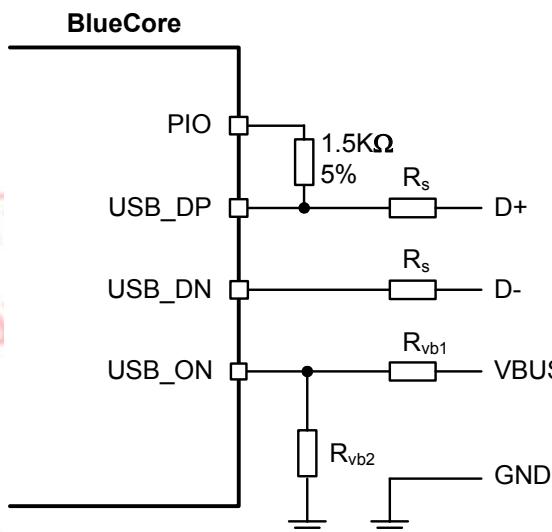


Figure 10.12: USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Note:

USB_ON is shared with BlueCore4-Audio ROM PIO terminals.

| Identifier | Value | Function |
|------------|--------------------|---------------------------------|
| R_s | 27Ω nominal | Impedance matching to USB cable |
| R_{vb1} | $22k\Omega$ 5% | VBUS ON sense divider |
| R_{vb2} | $47k\Omega$ 5% | VBUS ON sense divider |

Table 10.7: USB Interface Component Values

10.5.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. BlueCore4-Audio ROM negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume.

For Class 2 Bluetooth applications, CSR recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, BlueCore4-Audio ROM requests 100mA during enumeration.

For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting the PS Key PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10 μ F is present between VBUS and GND.

The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on the 1.8V supply to the analogue supply pins of BlueCore4-Audio ROM will result in reduced receive sensitivity and a distorted RF transmit signal.

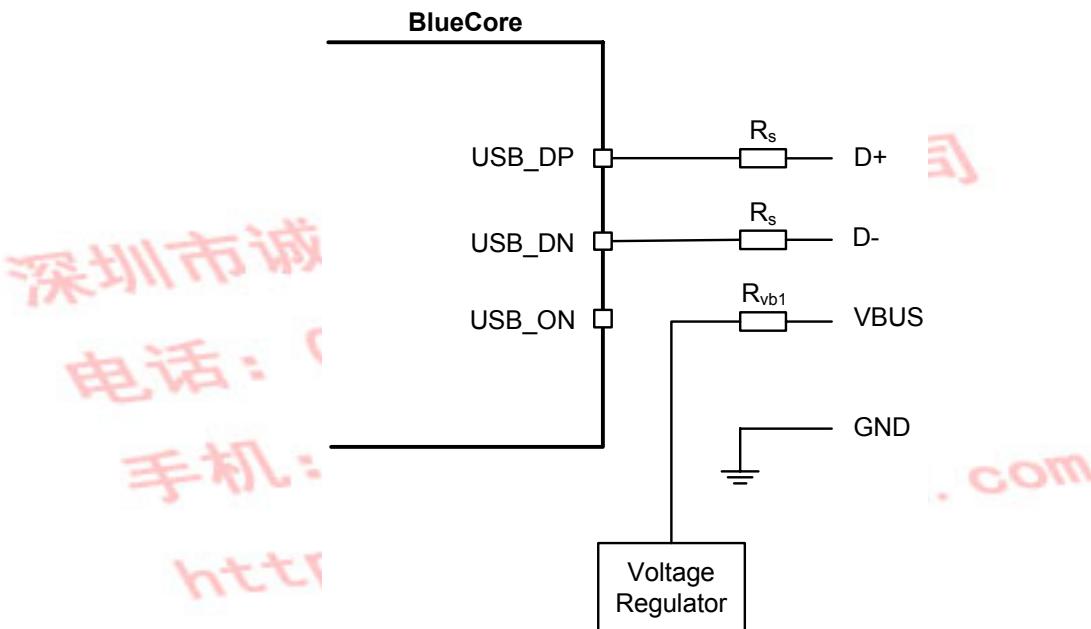


Figure 10.13: USB Connections for Bus-Powered Mode

10.5.6 Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 0.5mA from USB VBUS (self-powered devices may draw more than 0.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

The voltage regulator circuit itself should draw only a small quiescent current (typically less than 100 μ A) to ensure adherence to the suspend current requirement of the USB specification. This is not normally a problem with modern regulators. Ensure that external LEDs and/or amplifiers can be turned off by BlueCore4-Audio ROM. The entire circuit must be able to enter the suspend mode. Refer to separate CSR documentation for more details on USB Suspend.

10.5.7 Detach and Wake_Up Signalling

BlueCore4-Audio ROM can provide out-of-band signalling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding BlueCore4-Audio ROM into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting the PS Keys PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes BlueCore4-Audio ROM to put USB_DN and USB_DP in a high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, BlueCore4-Audio ROM will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB_WAKE_UP message (which runs over the USB cable) and cannot be sent while BlueCore4-Audio ROM is effectively disconnected from the bus.

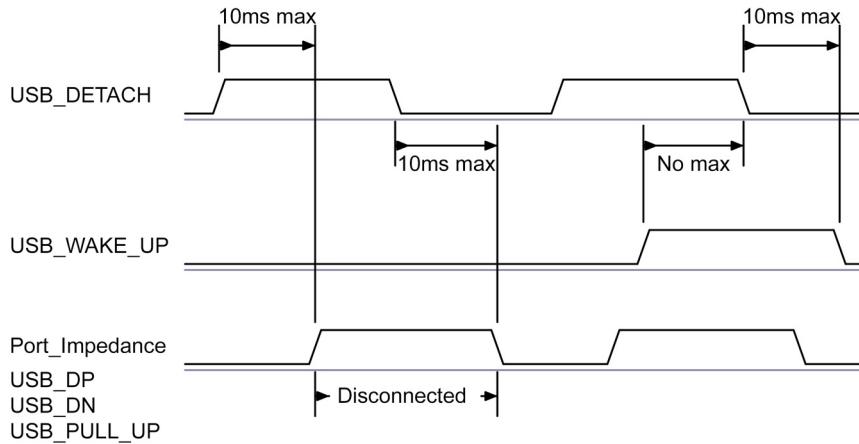


Figure 10.14: USB_DETACH and USB_WAKE_UP Signal

10.5.8 USB Driver

A USB Bluetooth device driver is required to provide a software interface between BlueCore4-Audio ROM and Bluetooth software running on the host computer. Suitable drivers are available from <http://www.csrsupport.com>.

10.5.9 USB 1.1 Compliance

BlueCore4-Audio ROM is qualified to the USB Specification v1.1, details of which are available from www.usb.org. The specification contains valuable information on aspects such as PCB track impedance, supply inrush current and product labelling.

Although BlueCore4-Audio ROM meets the USB specification, CSR cannot guarantee that an application circuit designed around the chip is USB compliant. The choice of application circuit, component choice and PCB layout all affect USB signal quality and electrical characteristics. The information in this document is intended as a guide and should be read in association with the USB specification, with particular attention being given to Chapter 7. Independent USB qualification must be sought before an application is deemed USB compliant and can bear the USB logo. Such qualification can be obtained from a USB plugfest or from an independent USB test house.

Terminals USB_DP and USB_DN adhere to the USB specification v2.0 (Chapter 7) electrical requirements.

10.5.10 USB 2.0 Compatibility

BlueCore4-Audio ROM is compatible with USB v2.0 host controllers; under these circumstances the two ends agree the mutually acceptable rate of 12Mbits/s according to the USB v2.0 specification.

10.6 Serial Peripheral Interface

BlueCore4-Audio ROM uses 16-bit data and 16-bit address serial peripheral interface, where transactions may occur when the internal processor is running or is stopped. This section details the considerations required when interfacing to BlueCore4-Audio ROM via the four dedicated serial peripheral interface terminals. Data may be written or read one word at a time or the auto increment feature may be used to access blocks.

10.6.1 Instruction Cycle

The BlueCore4-Audio ROM is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. The following table shows the instruction cycle for an SPI transaction.

| | | |
|---|--------------------------|---|
| 1 | Reset the SPI interface | Hold SPI_CSB high for two SPI_CLK cycles |
| 2 | Write the command word | Take SPI_CSB low and clock in the 8 bit command |
| 3 | Write the address | Clock in the 16-bit address word |
| 4 | Write or read data words | Clock in or out 16-bit data word(s) |
| 5 | Termination | Take SPI_CSB high |

Table 10.8: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CSB must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-Audio ROM on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-Audio ROM will reply to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CSB high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-Audio ROM offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CSB is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

10.6.2 Writing to the Device

To write to BlueCore4-Audio ROM, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CSB is taken high.

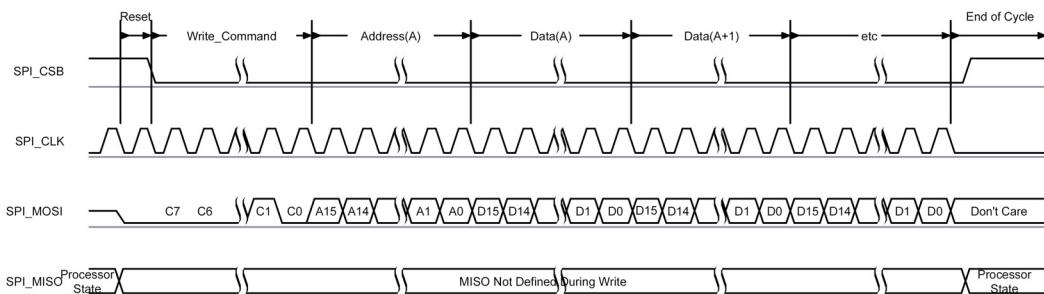


Figure 10.15: SPI Write Operation

10.6.3 Reading from the Device

Reading from BlueCore4-Audio ROM is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-Audio ROM then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CSB is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CSB is taken high.

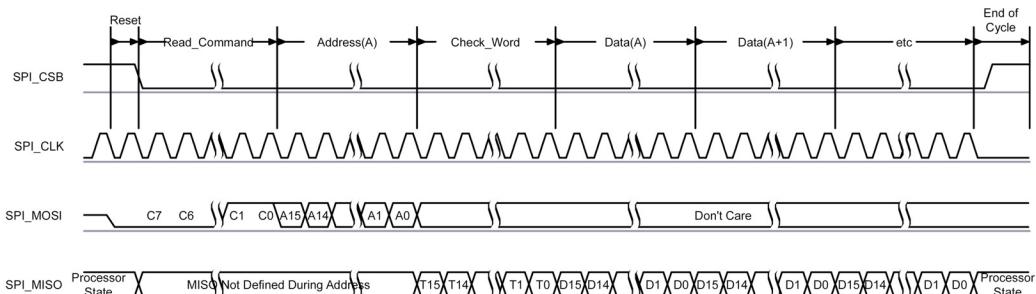


Figure 10.16: SPI Read Operation

10.6.4 Multi-Slave Operation

BlueCore4-Audio ROM should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-Audio ROM is deselected (SPI_CSB = 1), the SPI_MISO line does not float. Instead, BlueCore4-Audio ROM outputs 0 if the processor is running or 1 if it is stopped.

10.7 Mono Audio CODEC

The BlueCore4-Audio ROM audio CODEC is compatible with the direct speaker drive and microphone input using a minimum number of external components. It is primarily intended for voice applications and it is fully operational from a single 1.8V power supply. A fully differential architecture has been implemented for optimal power supply rejection and low noise performance. The digital format is 15-bit/sample linear PCM with a data rate of 8kHz.

The CODEC has an input stage containing a microphone amplifier, variable gain amplifier and a $\Sigma\Delta$ ADC. Its output stage contains a DAC, low-pass filter and output amplifier. The CODEC functional diagram is shown in below.

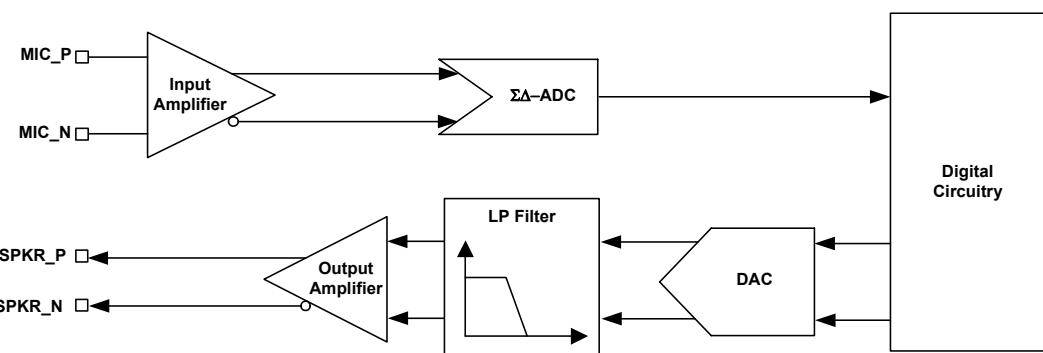


Figure 10.17: BlueCore4-Audio ROM CODEC Diagram

10.7.1 Input Stage

A low noise variable gain amplifier amplifies the signal difference between inputs MIC_N and MIC_P. The input may be from either a microphone or line input. The amplified signal is then digitised by a second order $\Sigma\Delta$ ADC. The high frequency single bit output from the ADC is converted to 15-bit 8kHz linear PCM data.

The gain is programmable via a PS Key and has a 42dB range with 3dB resolution. At maximum gain the full scale input level is 3mV rms. A bias network is required for operation with a microphone whereas the line input may be simply AC coupled. The following sections explain each of these modes. Single-ended signals are supported by BlueCore4-Audio ROM: a single-ended signal may be driven into either MIC_N or MIC_P with the undriven input coupled to ground by a capacitor.

The signal to noise ratio is better than 60dB and distortion is less than -75 dB.

10.7.2 Microphone Input

The BlueCore4-Audio ROM audio CODEC has been designed for use with microphones that have sensitivities between -60 and -40 dBV. The sensitivity of -60 dBV is equivalent to a microphone output of $1\mu\text{A}$ when presented with an input level of 94 dB SPL and loaded with $1\text{k}\Omega$. The microphone should be biased as shown in Figure 10.18.

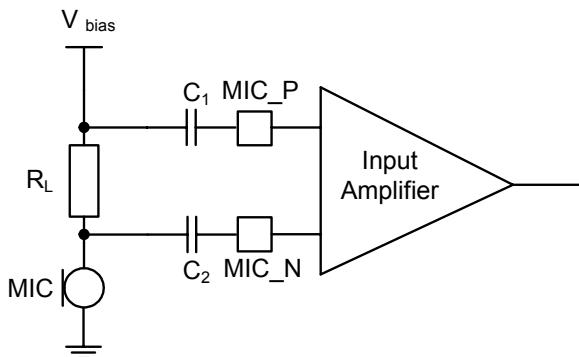


Figure 10.18: BlueCore4-Audio ROM Microphone Biasing

The input impedance at **MIC_N** and **MIC_P** is typically $20\text{k}\Omega$. C_1 and C_2 should be 47nF . R_L sets the microphone load impedance and is normally between 1 and $2\text{k}\Omega$. V_{bias} should be chosen to suit the microphone and have sufficient low noise. It may be obtained by filtering the output of a PIO line.

10.7.3 Line Input

If the input gain is set to less than 21 dB BlueCore4-Audio ROM automatically selects line input mode. In this mode the input impedance at **MIC_N** and **MIC_P** is increased to $130\text{k}\Omega$ typical. At the minimum gain setting the maximum input signal level is 380mV rms. Figure 10.19 and Figure 10.20 show two circuits for line input operation and show connections for either differential or single-ended inputs.

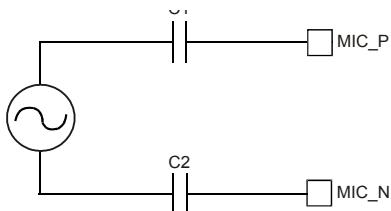


Figure 10.19: Differential Microphone Input

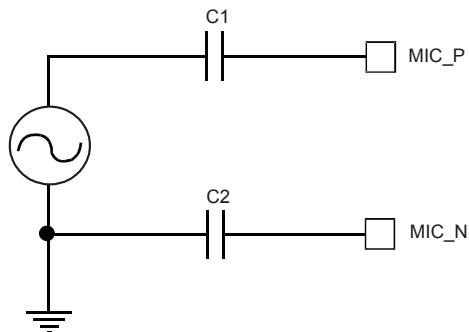


Figure 10.20: Single-ended Microphone Input

Note:

C1 and C2 should be 15nF.

10.7.4 Output Stage

The digital data is converted to an analogue value by a DAC, then it is filtered prior to amplification by the output amplifier and it is available as a differential signal between SPKR_P and SPKR_N. The output amplifier is capable of driving a speaker directly if its impedance is greater than 8Ω . The amplifier is stable with capacitive loads up to 500pF.

The gain is programmable with a range of 21dB and a resolution of 3dB. Maximum output level is typically 700 mV rms for high impedance loads, or 20mA rms for low impedance loads. The signal to noise is better than 70dB and the distortion is less than -75 dB.

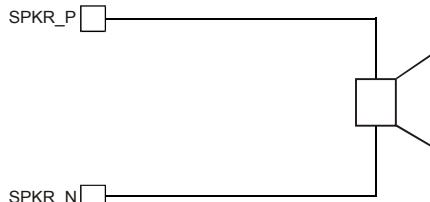


Figure 10.21: Speaker Output

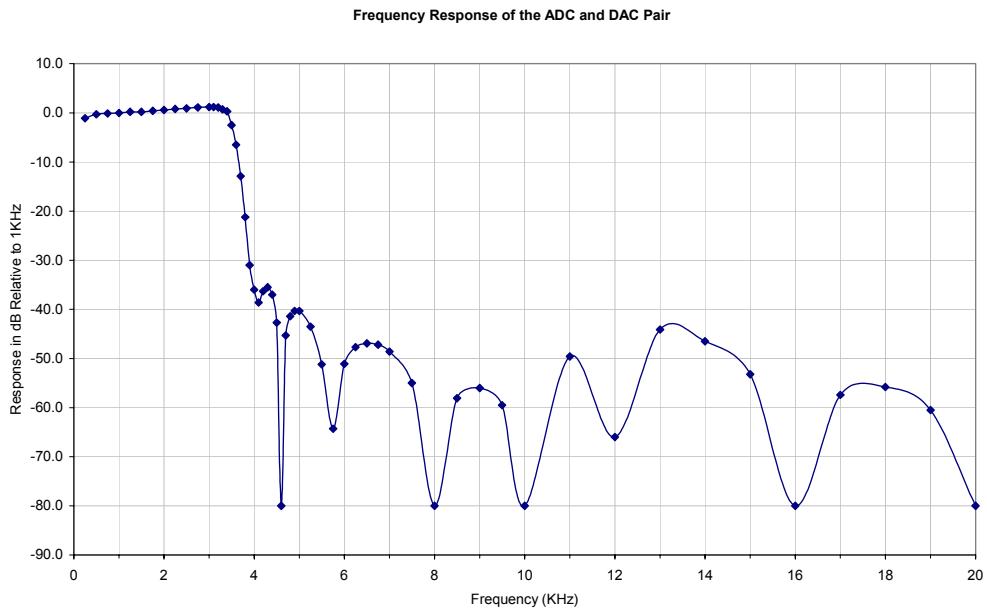


Figure 10.22: Frequency Response of the ADC and DAC Pair

10.7.5 Single-Ended Speaker Termination

Certain applications require that a single-ended speaker termination scheme is used in place of the standard differential output. BlueCore4-Audio ROM allows the unused SPKR_N output to be disabled to reduce static power consumption, or alternatively, to be used to buffer the internal reference voltage that is used by the SPKR_P drive. It is also possible to externally decouple the voltage reference via an AIO.

10.7.6 Bass Cut (Wind Noise Reduction)

Digital enhancements have been made to the BlueCore4-Audio ROM mono CODEC to reduce wind noise. The wind noise filter rejects low frequencies present in the ADC signal. This is achieved by combining an analogue reconstruction filter and a digital filter located at the output of the ADC processing chain (see Figure 10.24).

The digital wind noise filter has been designed to compensate for the frequency response of a single-pole analogue high-pass filter with a 3dB cut-off frequency at 800Hz. The analogue high-pass filter characteristic is provided by the audio input resistance in conjunction with external AC coupling capacitors. A simulation of the frequency response for bass cut (wind noise reduction) digital enhancement is shown in Figure 10.23.

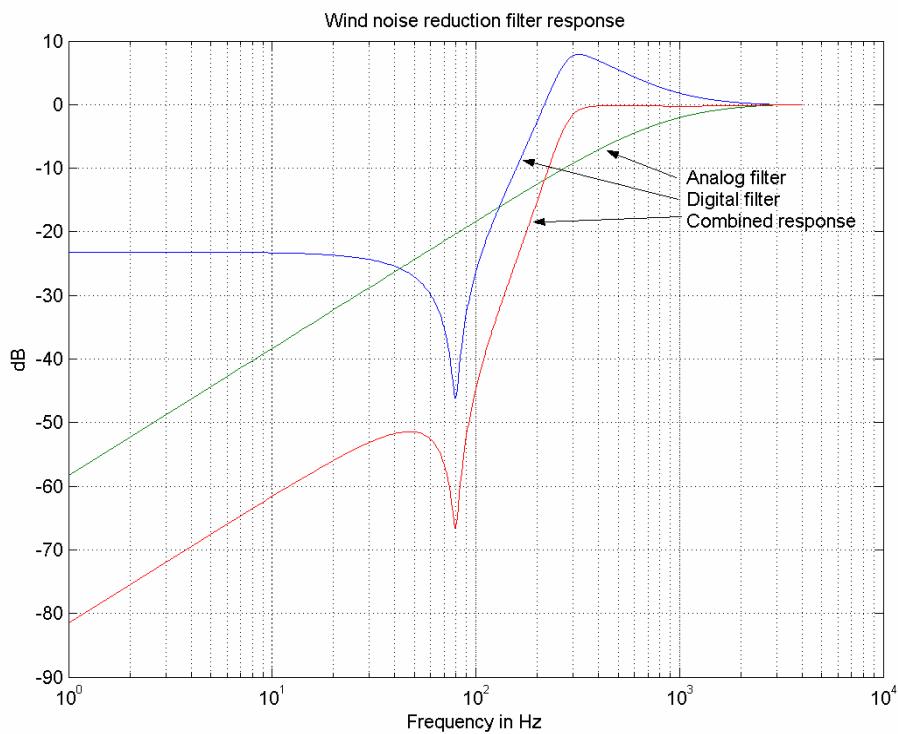


Figure 10.23: Simulated Wind Noise Reduction Filter Response

10.7.7 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BlueCore4-Audio ROM mono CODEC now incorporates the means to do this (see Figure 10.24).

The control bits in the IO_KCODEC_CONFIG register are shown in Figure 10.9

10.7.8 Audio CODEC Outline and Applicable Gains

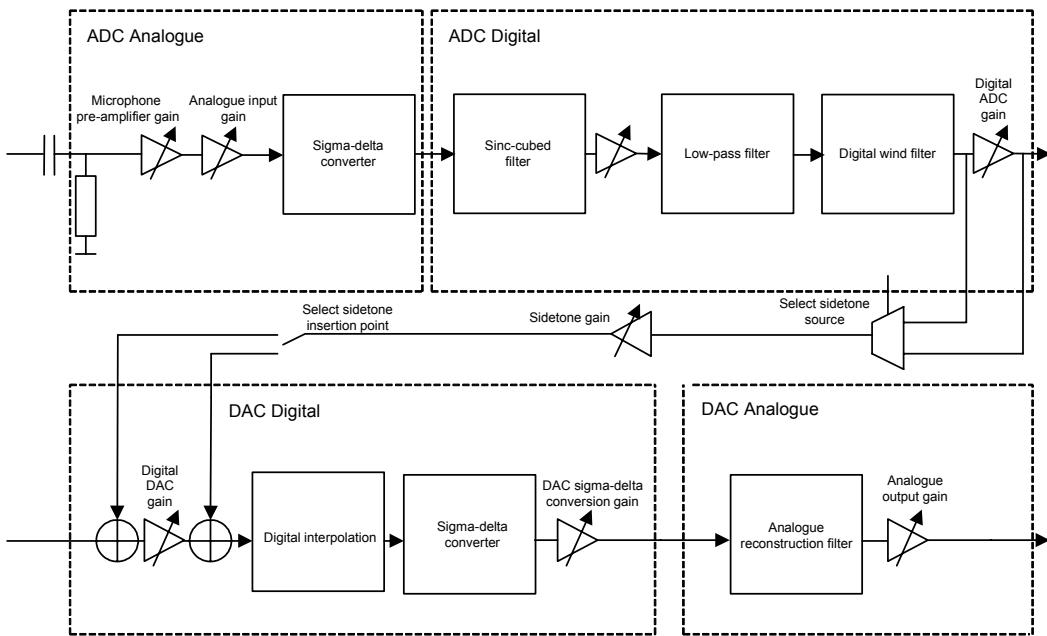


Figure 10.24: Audio CODEC Outline and Applicable Gains

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10.7.9 Firmware Interface

| Bit | Read/Write | Reset Value | Signal Name | Comment |
|-------|------------|-------------|---------------------------|---|
| [12] | W | Sync b0 | CODEC_DITHER_SMALL_EN | |
| [11] | W | Sync b0 | CODEC_ADC_LF_REJECT_HI_EN | Reserved. Set to Zero |
| [10] | W | Sync b0 | CODEC_ADC_LF_REJECT_EN | |
| [9] | W | Sync b0 | CODEC_SCALE_EN | |
| [8] | W | Sync b0 | CODEC_NOTCH_EN | |
| [7] | W | Sync b0 | CODEC_DITHER_EN | |
| [6] | W | Sync b0 | CODEC_SCALE_FINE_EN | |
| [5:4] | W | Sync b00 | CODEC_SIDETONE_ROUTE[1:0] | [1] selects the side tone addition to the DAC output before (when one) or after (when zero) applying the DAC digital gain [0] selects the side tone source to be the ADC output signal before (when zero) or after (when one) the ADC gain |
| [3:1] | W | Sync b000 | CODEC_SIDETONE_GAIN | Side tone gain control |
| [0] | W | Sync b0 | CODEC_SIDETONE_EN | Enable the side tone hardware |

Table 10.9: IO_KCODEC_CONFIG Control Register

Note:

In BlueCore4-Audio ROM all configuration bits are contained in a single register dedicated to the audio CODEC.

| Gain Name | PS Key Control Bits | Recommended Usage | Settings |
|-------------------------------|---------------------|--|---|
| Microphone pre-amplifier gain | CODEC_IN_GAIN[3] | Use to select between line input and microphone input | 0 = 0 dB, 1 = 21 dB |
| Analogue input gain | CODEC_IN_GAIN[2:0] | Use to control the audio input gain | 0 = 0dB, 1 = 3dB, 2 = 6dB, 3 = 9dB, 4 = 12dB, 5 = 15dB, 6 = 18 dB, 7 = 21 dB |
| Sinc-cubed filter gain | CODEC_IN_GAIN[8] | Set to zero | 0 = 0 dB, 1 = -6 dB |
| Digital ADC gain | CODEC_IN_GAIN[7:4] | Use to control the audio input gain, if the analogue ADC gain is exhausted | 0 = 0 dB, 1 = 3.5 dB, 2 = 6 dB, 3 = 9.5 dB, 4 = 12 dB, 5 = 15.5 dB, 6 = 18 dB, 7 = 21.5 dB, 8 = -24 dB, 9 = -20.5 dB, 10 = -18 dB, 11 = -14.5 dB, 12 = -12 dB, 13 = -8.5 dB, 14 = -6 dB, 15 = -2.5 dB |

| Gain Name | PS Key Control Bits | Recommended Usage | Settings |
|---------------------------------|---------------------|---|---|
| Digital DAC gain | CODEC_OUT_GAIN[7:4] | Use to control the audio output gain, if the analogue DAC gain is exhausted | Same as for the digital ADC gain |
| DAC sigma-delta conversion gain | CODEC_OUT_GAIN[9:8] | Set to 3 | 0 = 0dB, 1 = 2 dB, 2 = 3.5 dB, 3 = 4.9 dB |
| Analogue output gain | CODEC_OUT_GAIN[2:0] | Use to control the audio output gain. Do not use setting 7. | Same as for the analogue ADC gain |

Table 10.10: Recommended Settings for Audio CODEC

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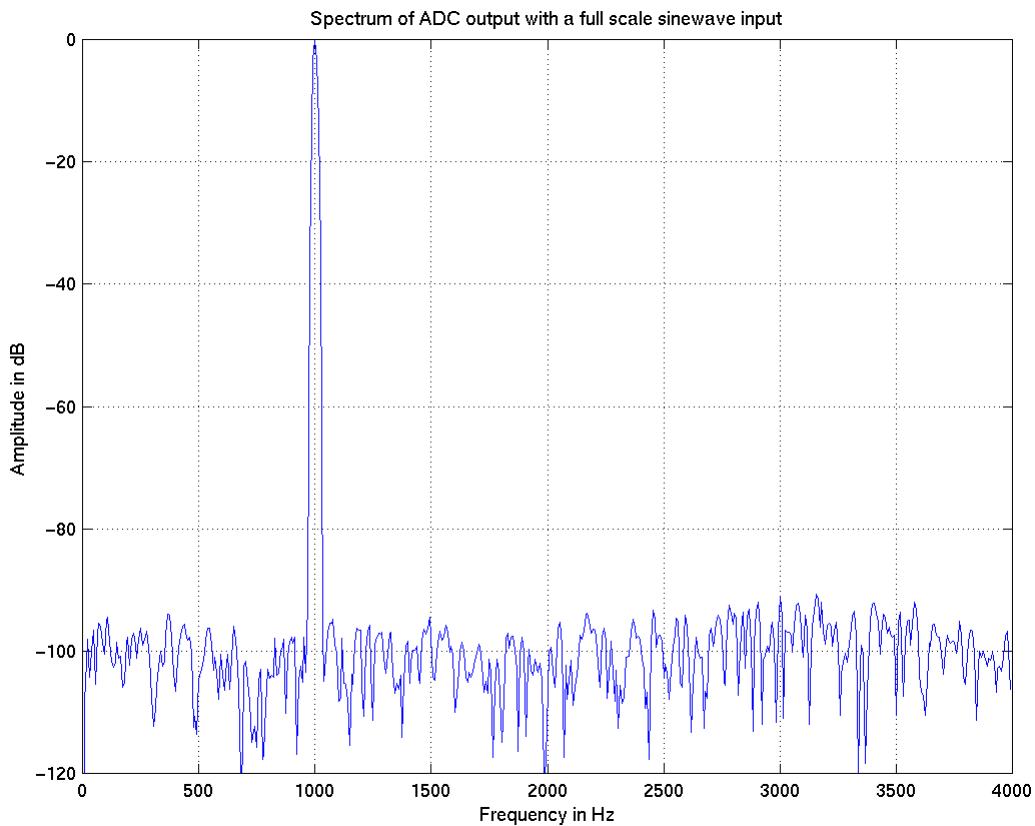


Figure 10.25: Spectrum of Analogue and Digital ADC Output with a Full Scale Sine Wave Input

Note:

(300mV RMS) sine into analogue mic amp. Output from digital ADC (extracted from BlueCore4-Audio ROM voice buffer).

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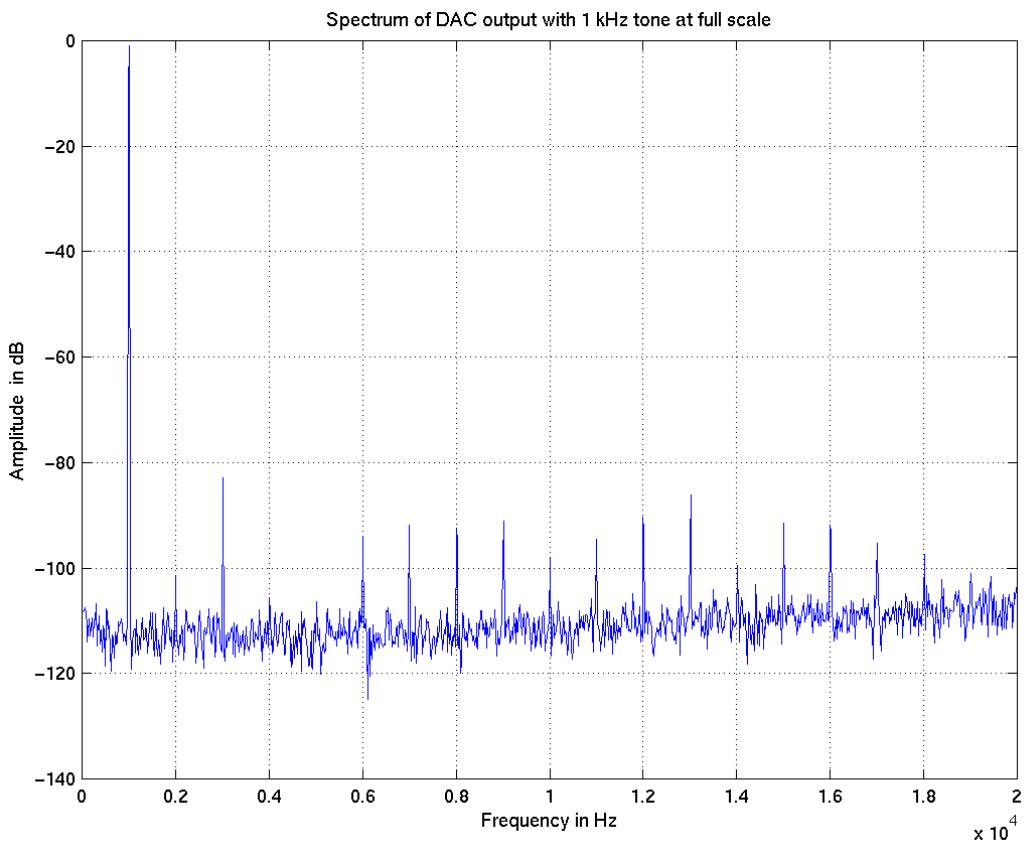


Figure 10.26: Spectrum of DAC Output with 1kHz Full Scale Tone

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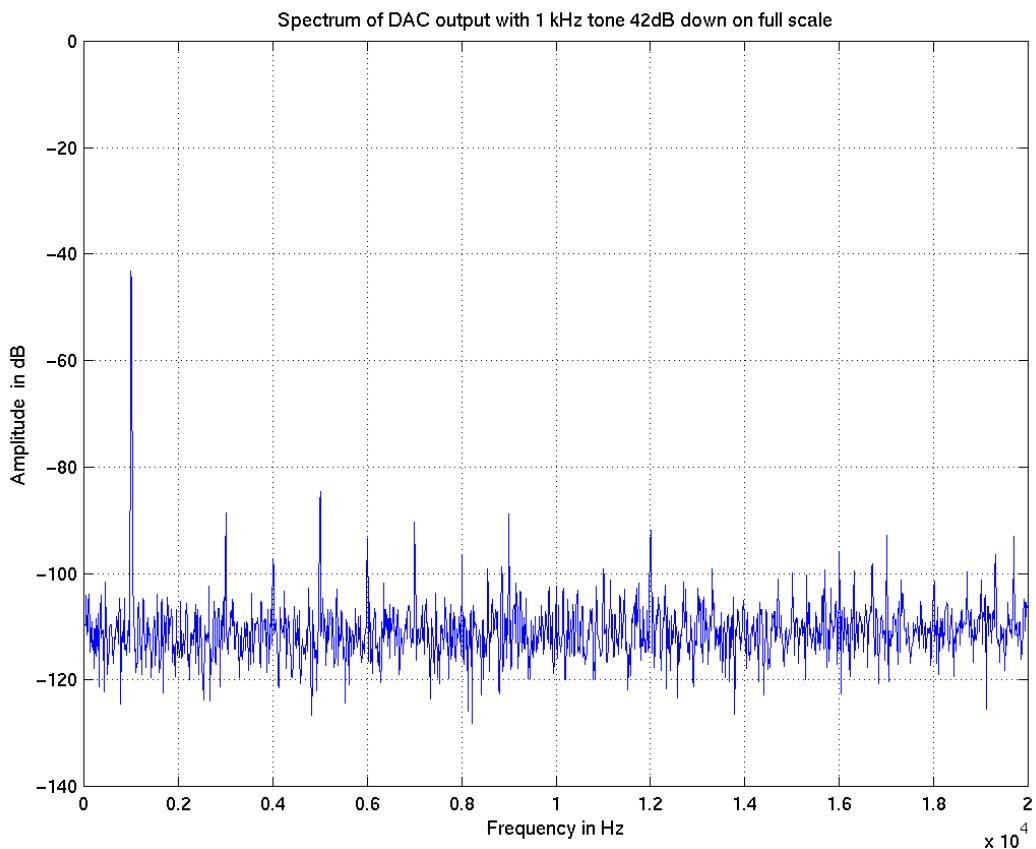


Figure 10.27: Spectrum of DAC Output with 1kHz Tone at -42dB Relative to Full Scale

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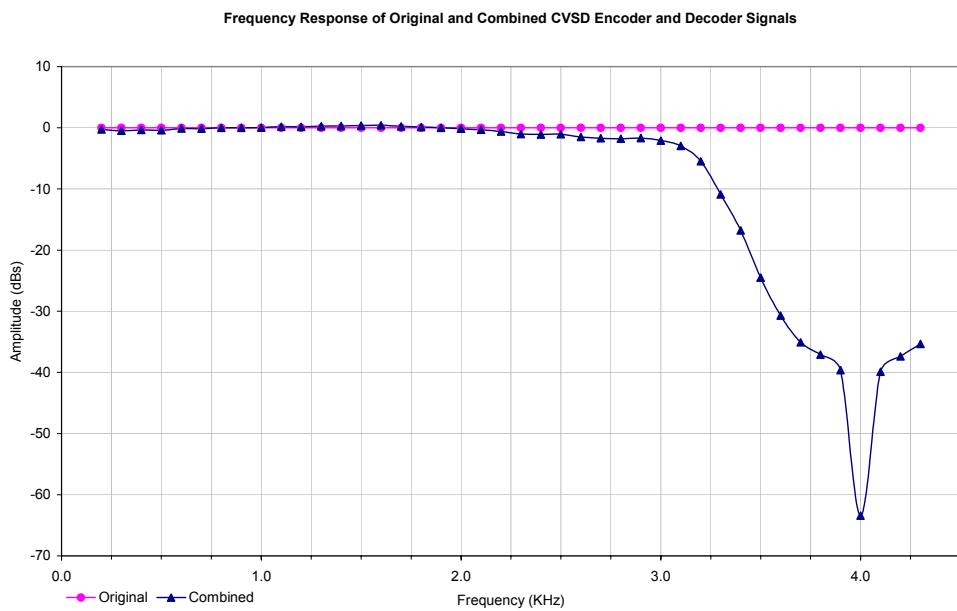


Figure 10.28: Response of CVSD Interpolation/Decimation Filter

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10.8 PCM CODEC Interface

Pulse Code Modulation (PCM) is a standard method used to digitise audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, BlueCore4-Audio ROM has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for wireless headset applications. BlueCore4-Audio ROM offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore4-Audio ROM allows the data to be sent to and received from a SCO connection. (1)

Up to three SCO connections can be supported by the PCM interface at any one time.

BlueCore4-Audio ROM can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. BlueCore4-Audio ROM is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ -law or A-law companded sample formats at 8ksamples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PS KEY_PCM_CONFIG32 (0x1b3).

BlueCore4-Audio ROM interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ -law CODEC
- Motorola MC145481 8-bit A-law and μ -law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- BlueCore4-Audio ROM is also compatible with the Motorola SSI interface

10.8.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore4-Audio ROM generates PCM_CLK and PCM_SYNC.

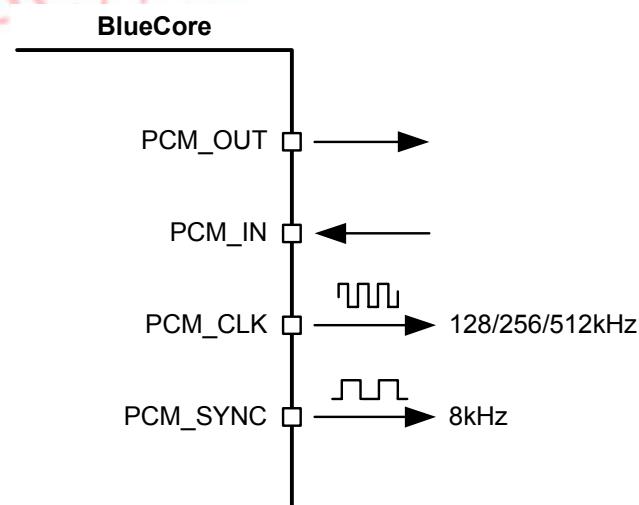


Figure 10.29: BlueCore4-Audio ROM as PCM Interface Master

When configured as the Slave of the PCM interface, BlueCore4-Audio ROM accepts PCM_CLK rates up to 2048kHz.

(1) Subject to firmware support. Contact CSR for current status.

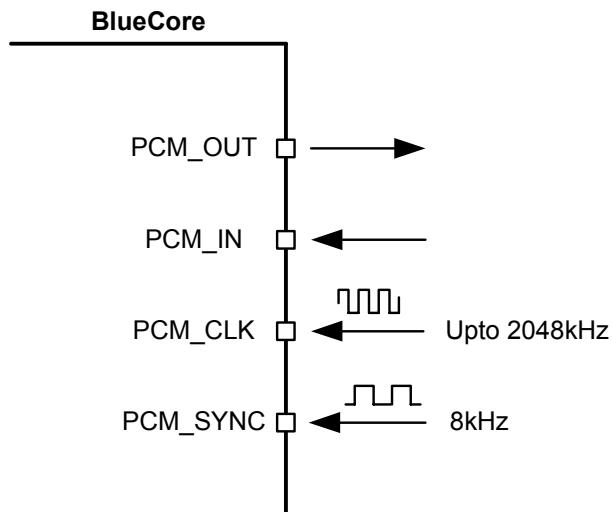


Figure 10.30: BlueCore4-Audio ROM as PCM Interface Slave

10.8.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore4-Audio ROM is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore4-Audio ROM is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5 μ s long.

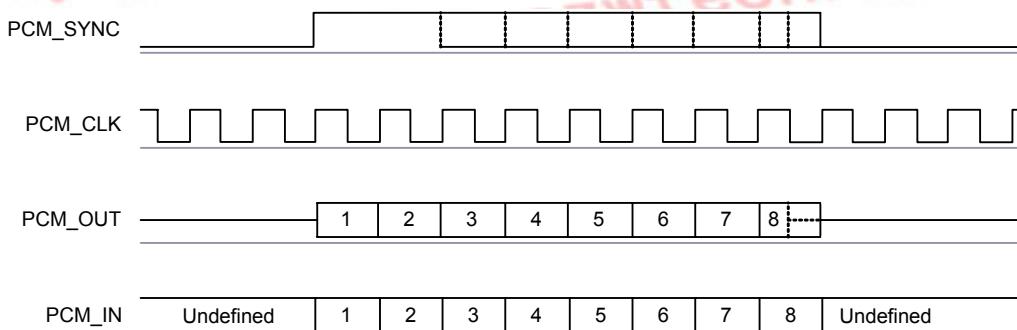


Figure 10.31: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore4-Audio ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.8.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

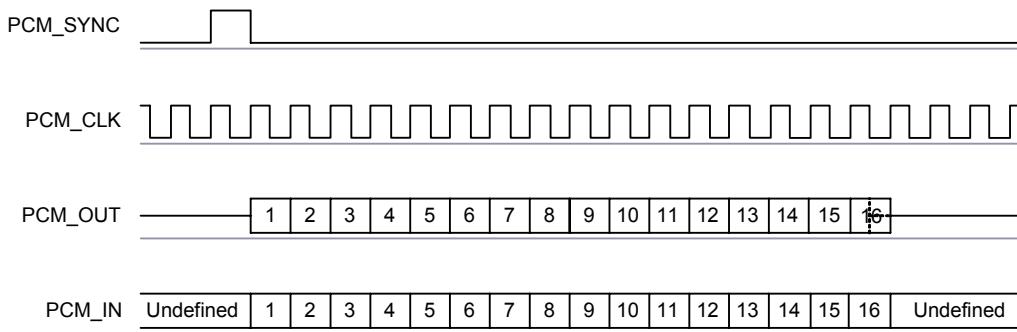


Figure 10.32: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore4-Audio ROM samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.8.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

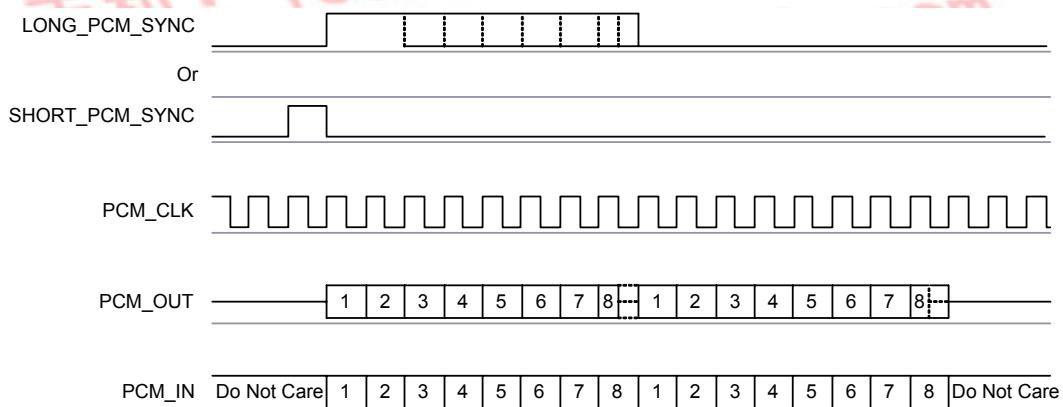


Figure 10.33: Multi-slot Operation with Two Slots and 8-bit Companded Samples

10.8.5 GCI Interface

BlueCore4-Audio ROM is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

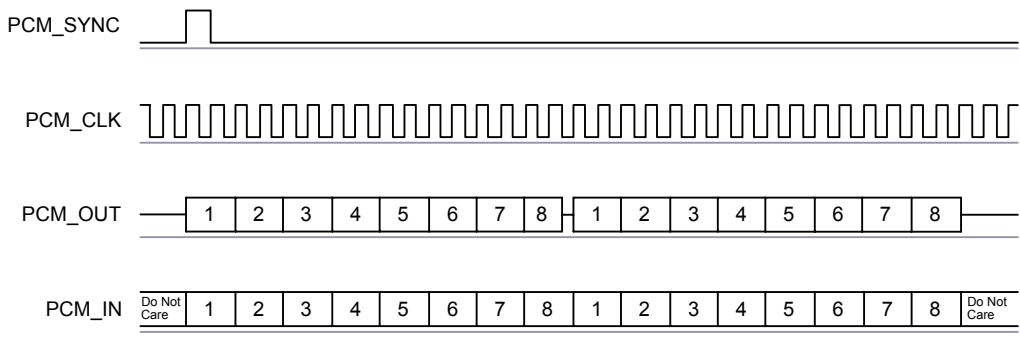


Figure 10.34: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With BlueCore4-Audio ROM in Slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

10.8.6 Slots and Sample Formats

BlueCore4-Audio ROM can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore4-Audio ROM supports 13-bit linear, 16-bit linear and 8-bit μ -law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

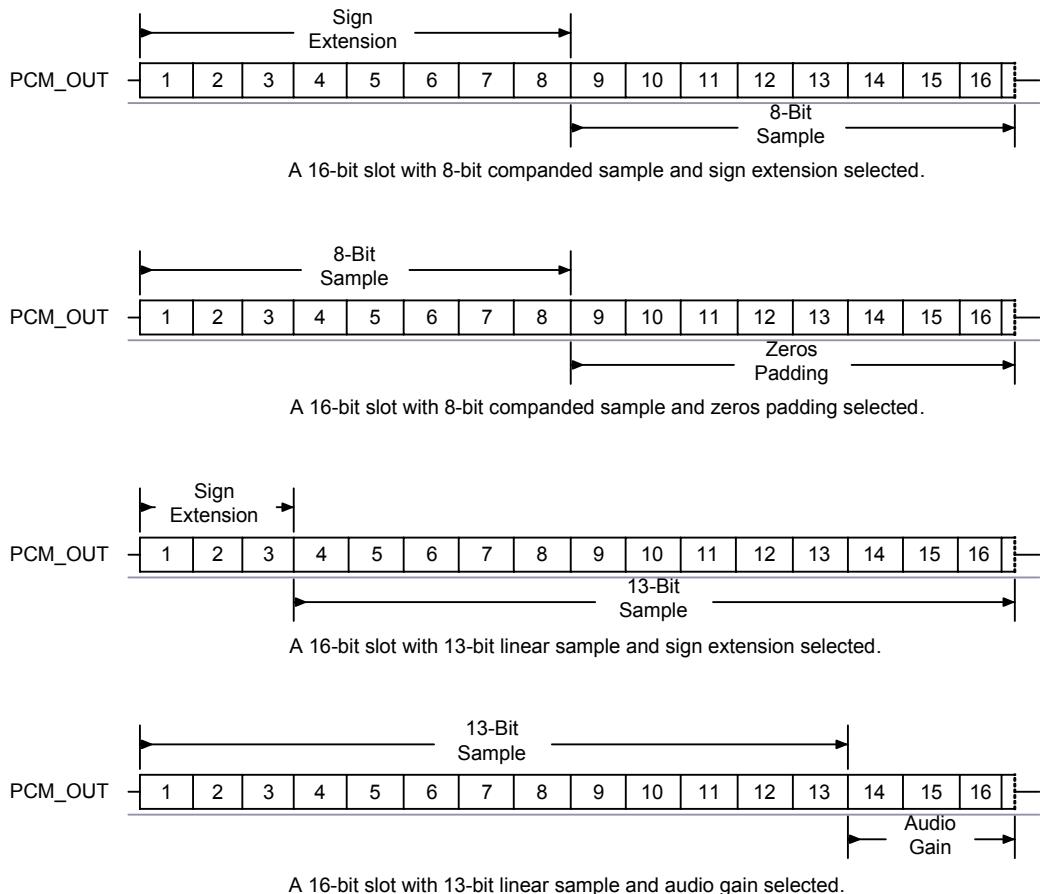


Figure 10.35: 16-Bit Slot Length and Sample Formats

10.8.7 Additional Features

BlueCore4-Audio ROM has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

10.8.8 PCM Timing Information

| Symbol | Parameter | | Min | Typ | Max | Unit |
|-------------------|--|---|-----|-----|-----|----------|
| f_{mclk} | PCM_CLK frequency | 4MHz DDS generation. Selection of frequency is programmable. See Table 10.13. | - | 128 | - | kHz |
| | | 48MHz DDS generation. Selection of frequency is programmable. See Table 10.14 and PCM_CLK and PCM_SYNC Generation on page 97. | | 256 | | |
| | | | | 512 | | |
| | PCM_SYNC frequency | | 2.9 | | - | kHz |
| $t_{mclkh}^{(a)}$ | PCM_CLK high | 4MHz DDS generation | 980 | - | - | ns |
| $t_{mclkl}^{(a)}$ | PCM_CLK low | 4MHz DDS generation | 730 | - | - | ns |
| - | PCM_CLK jitter | 48MHz DDS generation | | | 21 | ns pk-pk |
| $t_{dmclksynch}$ | Delay time from PCM_CLK high to PCM_SYNC high | | | - | 20 | ns |
| $t_{dmclkpout}$ | Delay time from PCM_CLK high to valid PCM_OUT | | | - | 20 | ns |
| $t_{dmclksyncl}$ | Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only) | | - | - | 20 | ns |
| $t_{dmclkhsyncl}$ | Delay time from PCM_CLK high to PCM_SYNC low | | - | - | 20 | ns |
| $t_{dmclkpoutz}$ | Delay time from PCM_CLK low to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{dmclkhpoutz}$ | Delay time from PCM_CLK high to PCM_OUT high impedance | | - | - | 20 | ns |
| $t_{supinclk}$ | Set-up time for PCM_IN valid to PCM_CLK low | 30 | - | - | - | ns |
| $t_{hpinclk}$ | Hold time for PCM_CLK low to PCM_IN invalid | 10 | - | - | - | ns |

Table 10.11: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

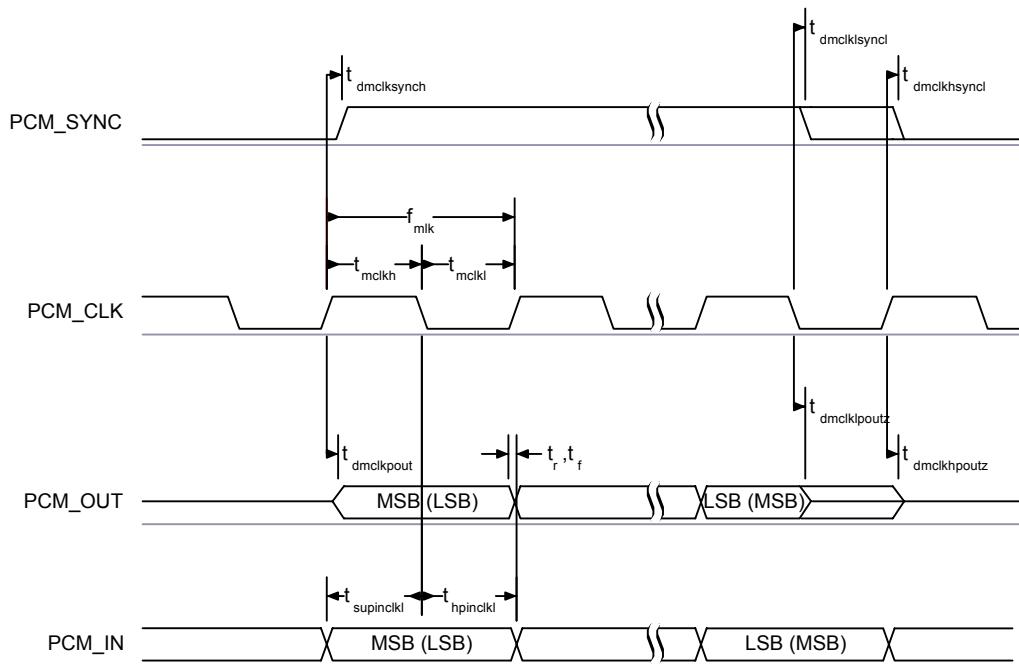


Figure 10.36: PCM Master Timing Long Frame Sync

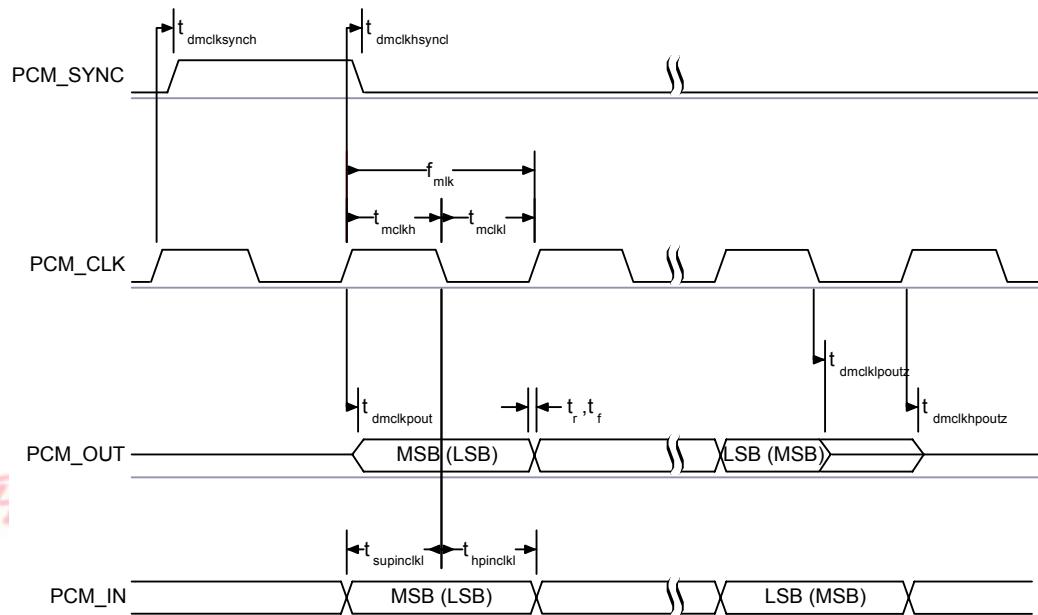


Figure 10.37: PCM Master Timing Short Frame Sync

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|--|-----|-----|------|------|
| f_{sclk} | PCM clock frequency (Slave mode: input) | 64 | - | 2048 | kHz |
| f_{sclk} | PCM clock frequency (GCI mode) | 128 | - | 4096 | kHz |
| t_{sclkL} | PCM_CLK low time | 200 | - | - | ns |
| t_{sclkH} | PCM_CLK high time | 200 | - | - | ns |
| $t_{hsclkSynch}$ | Hold time from PCM_CLK low to PCM_SYNC high | 30 | - | - | ns |
| $t_{susclkSynch}$ | Set-up time for PCM_SYNC high to PCM_CLK low | 30 | - | - | ns |
| t_{dpout} | Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only) | - | - | 20 | ns |
| $t_{dsclkhout}$ | Delay time from CLK high to PCM_OUT valid data | - | - | 20 | ns |
| t_{dpoutz} | Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance | - | - | 20 | ns |
| $t_{supinsclkL}$ | Set-up time for PCM_IN valid to CLK low | 30 | - | - | ns |
| $t_{hpinsclkL}$ | Hold time for PCM_CLK low to PCM_IN invalid | 30 | - | - | ns |

Table 10.12: PCM Slave Timing

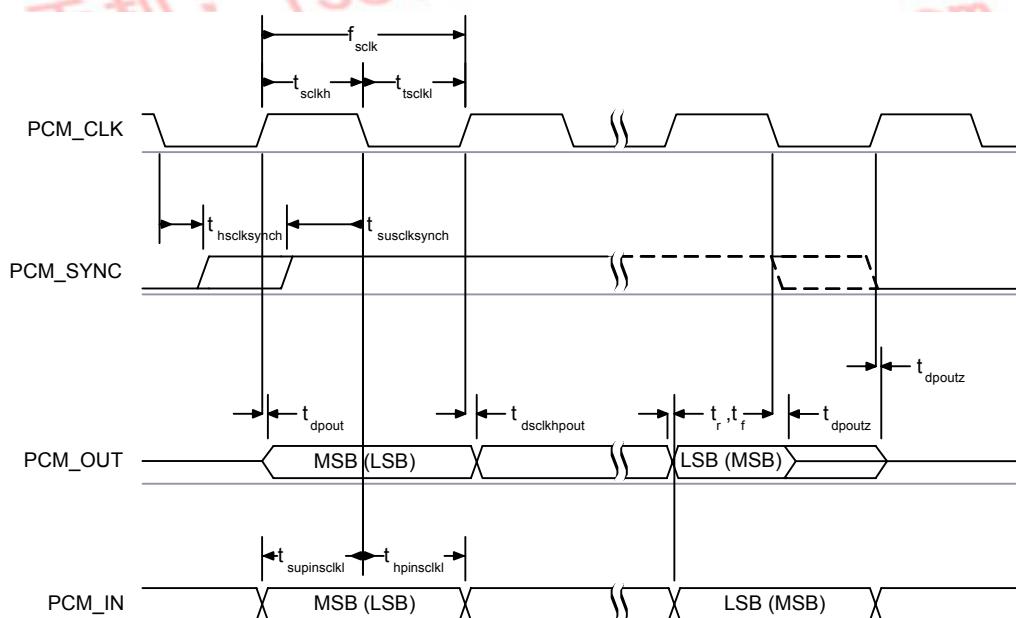


Figure 10.38: PCM Slave Timing Long Frame Sync

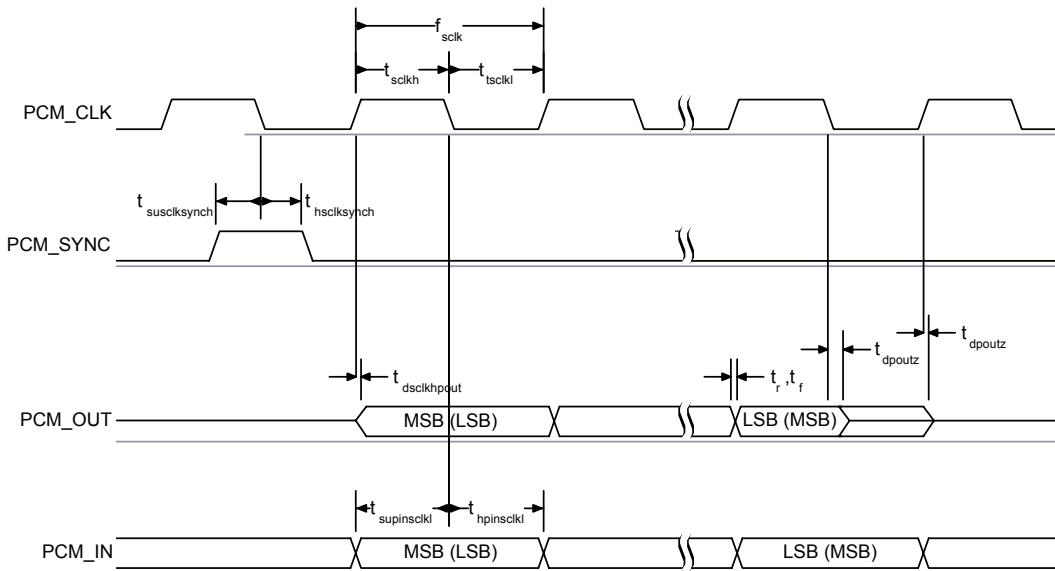


Figure 10.39: PCM Slave Timing Short Frame Sync

PCM_CLK and PCM_SYNC Generation

BlueCore4-Audio ROM has two methods of generating PCM_CLK and PCM_SYNC in master mode. The first is generating these signals by Direct Digital Synthesis (DDS) from BlueCore4-Audio ROM internal 4MHz clock (which is used in BlueCore2-External). Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz. The second is generating PCM_CLK and PCM_SYNC by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). This second method is selected by setting bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

The Equation 10.11 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{\text{CNT_RATE}}{\text{CNT_LIMIT}} \times 24\text{MHz}$$

Equation 10.11: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

The frequency of PCM_SYNC relative to PCM_CLK can be set using Equation 10.12:

$$f = \frac{\text{PCM_CLK}}{\text{SYNC_LIMIT} \times 8}$$

Equation 10.12: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

10.8.9 PCM Configuration

The PCM configuration is set using two PS Keys, PSKEY_PCM_CONFIG32 detailed in Table 10.13 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 10.14. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e., first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tri-state of PCM_OUT.

| Name | Bit Position | Description |
|----------------------------|--------------|---|
| - | 0 | Set to 0 |
| SLAVE_MODE_EN | 1 | 0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC. |
| SHORT_SYNC_EN | 2 | 0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame). |
| - | 3 | Set to 0. |
| SIGN_EXTEND_EN | 4 | 0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension. |
| LSB_FIRST_EN | 5 | 0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples. |
| TX_TRISTATE_EN | 6 | 0 = drive PCM_OUT continuously. 1 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active. |
| TX_TRISTATE_RISING_EDGE_EN | 7 | 0 = tri-state PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tri-state PCM_OUT after rising edge of PCM_CLK. |
| SYNC_SUPPRESS_EN | 8 | 0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC whilst keeping PCM_CLK running. Some CODECS utilise this to enter a low power state. |
| GCI_MODE_EN | 9 | 1 = enable GCI mode |
| MUTE_EN | 10 | 1 = force PCM_OUT to 0 |
| 48M_PCM_CLK_GEN_EN | 11 | 0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4 MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48 MHz clock. |
| LONG_LENGTH_SYNC_EN | 12 | 0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1. |
| - | [20:16] | Set to 0b00000 |
| MASTER_CLK_RATE | [22:21] | Selects 128 (0b01), 256 (0b00), 512 (0b10) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low. |
| ACTIVE_SLOT | [26:23] | Default is 0001. Ignored by firmware. |

| Name | Bit Position | Description |
|---------------|--------------|--|
| SAMPLE_FORMAT | [28:27] | Selects between 13 (0b00), 16 (0b01), 8 (0b10) bit sample with 16 cycle slot duration or 8 (0b11) bit sample with 8 cycle slot duration. |

Table 10.13: PSKEY_PCM_CONFIG32 Description

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手机: 13510662515
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| Name | Bit Position | Description |
|------------|--------------|--|
| CNT_LIMIT | [12:0] | Sets PCM_CLK counter limit |
| CNT_RATE | [23:16] | Sets PCM_CLK count rate |
| SYNC_LIMIT | [31:24] | Sets PCM_SYNC division relative to PCM_CLK |

Table 10.14: PSKEY_PCM_LOW_JITTER_CONFIG Description

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10.9 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-Audio ROM where either device can turn on the clock without having to wake up the other device. PIO[3] can be used as the host clock enables input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-Audio ROM.

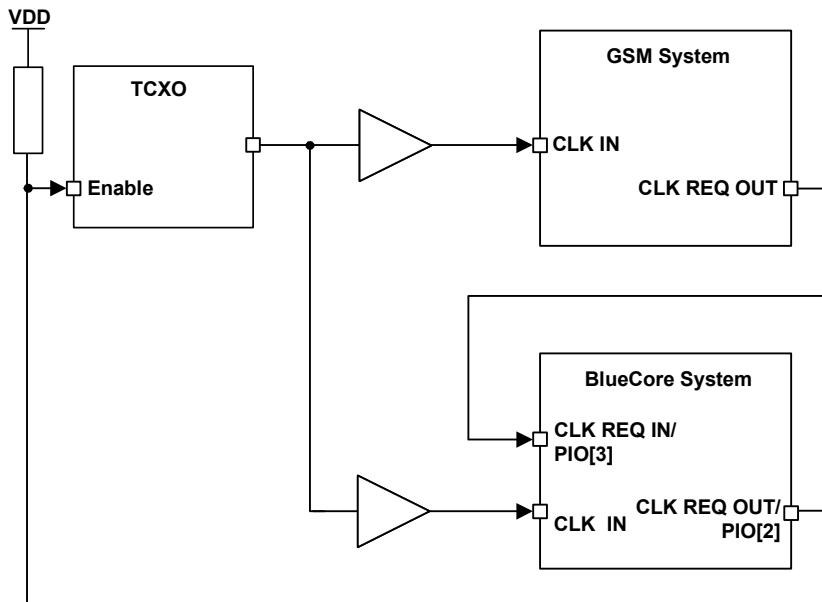


Figure 10.40: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] will be tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a $470\text{k}\Omega$ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

10.10 RESETB

BlueCore4-Audio ROM may be reset from several sources: RESETB pin, power on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

The power on reset occurs when the VDD_CORE supply falls below typically 1.5V and is released when VDD_CORE rises above typically 1.6V. At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-downs. Following a reset, BlueCore4-Audio ROM assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-Audio ROM is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-Audio ROM free runs, again at a safe frequency.

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10.10.1 Pin States on Reset

| Pin Name | State |
|-----------|---------------------------------------|
| PIO[10:0] | Input with weak pull-down |
| PCM_OUT | Tri-stated with weak pull-down |
| PCM_IN | Input with weak pull-down |
| PCM_SYNC | Input with weak pull-down |
| PCM_CLK | Input with weak pull-down |
| UART_TX | Output tri-stated with weak pull-up |
| UART_RX | Input with weak pull-down |
| UART_RTS | Output tri-stated with weak pull-up |
| UART_CTS | Input with weak pull-down |
| USB_DP | Input with weak pull-down |
| USB_DN | Input with weak pull-down |
| SPI_CSB | Input with weak pull-up |
| SPI_CLK | Input with weak pull-down |
| SPI_MOSI | Input with weak pull-down |
| SPI_MISO | Output tri-stated with weak pull-down |
| AIO[2:0] | Output tri-stated with weak pull-down |
| RESETB | Input with weak pull-up |
| TEST_EN | Input with strong pull-down |
| AUX_DAC | High impedance |
| RX_IN | High impedance |
| XTAL_IN | High impedance, 250kΩ to XTAL_OUT |
| XTAL_OUT | High impedance, 250kΩ to XTAL_IN |

Table 10.15: Pin States of BlueCore4-Audio ROM on Reset

10.10.2 Status after Reset

The chip status after a reset is as follows:

- Warm Reset: Baud rate and RAM data remain available
- Cold Reset⁽¹⁾ : Baud rate and RAM data not available

(1) A Cold Reset is either Power cycle, system reset (firmware fault code) or Reset signal. See .

10.11 Power Supply

10.11.1 Power Regulators

BlueCore4-Audio ROM contains two 1.8V regulators, either of which may be used to power the 1.8V supplies of this device. The device pin VREG_EN is used to enable and disable both of these regulators.

10.11.2 Supply Domains and Sequencing

The 1.8V supplies are VDD_ANA, VDD_VCO, VDD_RADIO and VDD_CORE. It is recommended that the 1.8V supplies are all powered at the same time. The order of powering the 1.8V supplies relative to the other I/O supplies (VDD_PIO, VDD_PADS, VDD_USB and VDD_MEM) is not important, however if the I/O supplies are powered before the 1.8V supplies all digital IO will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_VCO, and VDD_RADIO should be connected directly to the 1.8V supply; a simple RC filter is recommended for VDD_CORE to reduce transients put back onto the power supply rails.

The I/O supplies may be connected together or independently to supplies at an appropriate voltage. They should be simply decoupled.

10.11.3 External Voltage Source

If the 1.8V rails of BlueCore4-Audio ROM are supplied from an external voltage source, it is recommended that VDD_VCO, VDD_RADIO, and VDD_ANA, should have less than 10mV rms noise levels between 0 to 10MHz.

Single tone frequencies are also to be avoided. The transient response of any regulator used should be 20 μ s or less. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption will jump to high levels (see average current consumption section).

10.11.4 Switch-mode Regulator

The on-chip switch-mode 1.8V regulator can be used to power the 1.8V supplies. The required external filter circuit should consist of a low resistance 33 μ H series inductor (between the LX terminal and the 1.8V supply), followed by a low ESR 4.7 μ F shunt capacitor (between the 1.8V supply and ground). For optimum efficiency the 33 μ H inductor must have low resistance. To optimise reliability and enable temperature derating, it must also be able to support at least 150mA.

It is recommended that the series resistance of tracks between the BAT_P and BAT_N terminals, the filter components and the external voltage source are minimised to maintain high efficiency power conversion and low supply ripple. The regulator may be enabled by the VREG_EN pin, by the device firmware, or by the internal battery charger. The regulator is switched into a low power pulse skipping mode automatically when the device enters Deep-Sleep mode. When this regulator is not used the terminals BAT_P and LX must be grounded or left unconnected.

10.11.5 Linear Regulator

The on-chip 1.8V linear regulator may also be used to power the 1.8V dependent supplies. It is recommended that a smoothing circuit be used, consisting of an output regulator connected to ground via a 2.2 Ω resistor and a series connected 2.2 μ F low ESR capacitor.

The regulator may be enabled by the VREG_EN pin or by the device firmware. The regulator switches into a low power mode automatically when the device enters Deep-Sleep mode. When this regulator is not used the terminals VREG_IN and VREG_OUT must be grounded or left unconnected.

10.11.6 VREG_EN Pin

The regulator enable pin, VREG_EN can be used to enable and disable the BlueCore4-Audio ROM device if one of the on-chip regulators is being used. The pin is active high and has a weak pull down.

When the pin is pulled high the active regulator is enabled, allowing the device to boot-up. The firmware is then able to latch the regulator on and the VREG_EN pin may be released.

10.11.7 Battery Charger

The battery charger is a constant current/constant voltage charger circuit and is suitable for Lithium Ion/Polymer batteries only. It must be used in conjunction with the switch-mode regulator as the two circuits share a connection with the battery terminal, BAT_P.

The constant current provided by the charger may be set between 25mA and 100mA (typical) allowing different capacity batteries to be charged at their optimum rate. The required current setting is stored in and read by the battery charger during the first boot-up sequence. The charger circuit also requires a float voltage calibration setting which must be measured for each device during production test. This should be stored in external PROM memory, and will be read by the battery charger during the boot-up sequence.

Whenever the charger is powered the switch-mode regulator is enabled automatically. Internal interfaces are provided to allow firmware to monitor the precise battery voltage and the status of the battery charger. The firmware may also disable the charger, for example, if temperature limits for safe charging are exceeded.

By default, an LED connected to the terminal LED[0] will illuminate at full intensity when a battery is being charged. This behaviour may be overridden by the firmware if required.

When the charger supply is not connected to V_CHG the terminal must be left open.

Important Note:

Protection Module

Lithium Ion/Polymer batteries are capable of delivering high currents of several amperes when short-circuited. This can damage connecting wires and Printed Circuit Board (pcb) components. More seriously, pressure can build up in the cell envelope, causing it to explode and injure the user.

CSR strongly suggests that Lithium/Ion Polymer batteries incorporate an integral protection module. This is typically a small Integrated Circuit (IC) and Field Effect Transistor (FET) interposed between the battery body and its connecting wires. The protection module limits the short circuit current. Good modules will also prevent over-charge and over-discharge, which can also cause damage to the battery.

Additional Precautions

CSR also suggests that the following additional precautions are observed:

- The direct current (dc) inlet socket used on the appliance should be of a proprietary design, preventing users from attaching the charger or supply connector for another appliance (e.g., a mobile phone or laptop computer). The use of popular 2.1mm and 2.5mm DC jack sockets must be avoided for this reason.
- Include a voltage limiting circuit (clamp) on the charger inlet. Remember that this circuit could be exposed to voltages as high as 30V (of either polarity) if a laptop computer power supply has been connected. Include a small fuse in series with the DC inlet, but prior to the clamp.
- Never bring the Lithium Ion/Polymer battery connections directly to charging pins on the outside of the appliance casing, where they could be short-circuited by keys in the user's pocket, for example.

Temperature Extremes

Some Lithium Ion/Polymer cells can be damaged by charging at temperature extremes (e.g., below 0° or above 50°). Consult the battery manufacture for guidance.

For more information, see the CSR document Lithium Ion/Polymer Battery Safety Information Note.

10.11.8 LED Drivers

BlueCore4-Audio ROM includes two 4.2V tolerant pads dedicated to driving LED indicators. Both pads may be controlled by firmware, while LED[0] can also be set by the battery charger. The intensity of the LEDs may be adjusted by firmware.

The terminals are low output impedance open-drain outputs, so the LED must be connected in series with a current limiting resistor between the battery terminal or positive supply and the pad.

11 Typical Radio Performance - Basic Data Rate

Important Note:

Results obtained using CSR's evaluation circuit as shown in Figure 13.1 with ceramic filter bypassed.

11.1 Transmitter Performance - Basic Data Rate

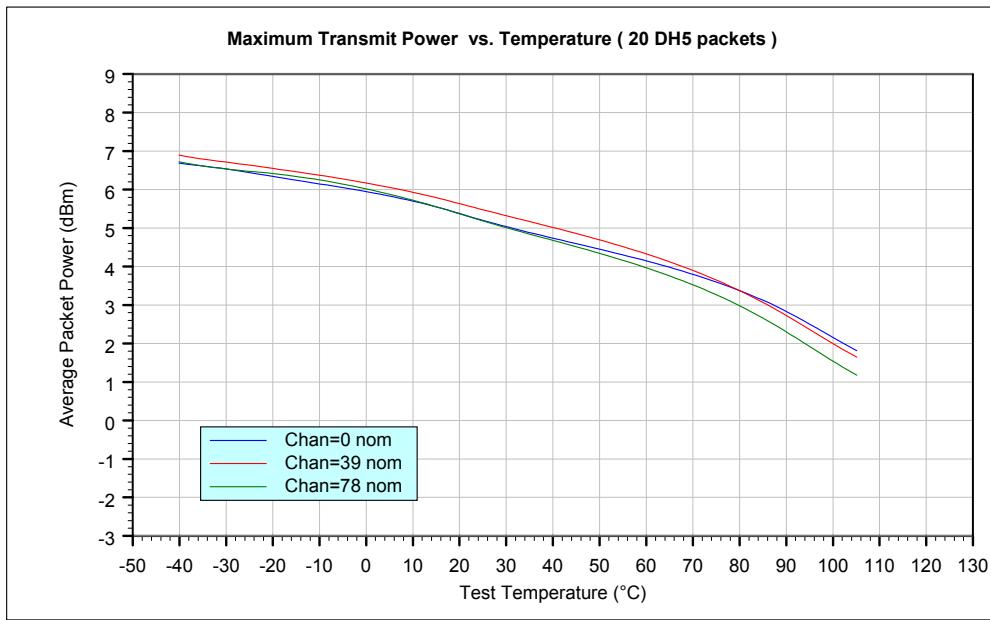


Figure 11.1: Maximum Transmit Power vs. Temperature (20 DH5 Packets)

Note:

Output power temperature compensation disabled.

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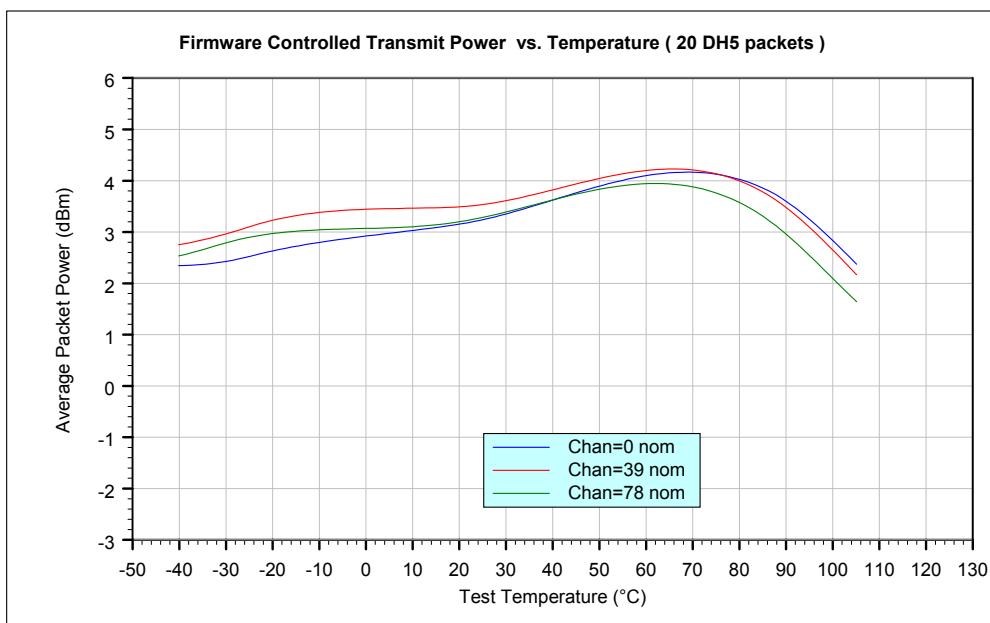


Figure 11.2: Firmware Controlled Transmit Power vs. Temperature (20 DH5 Packets)

Note:

Output power temperature compensation enabled.

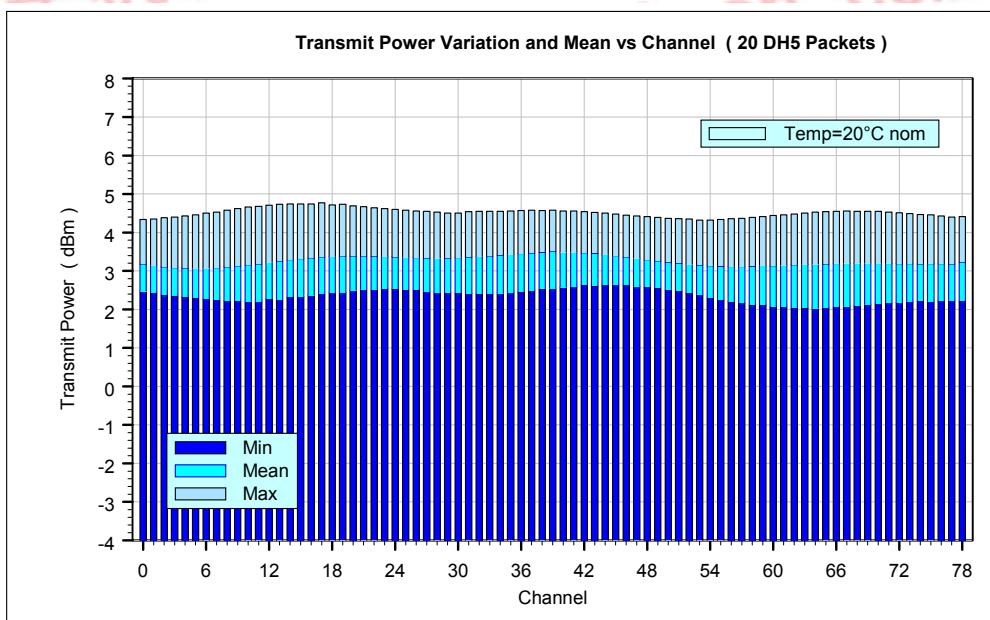


Figure 11.3: Transmit Power Variation and Mean vs. Channel (20 DH5 Packets)

Note:

Output power as per Figure 11.2

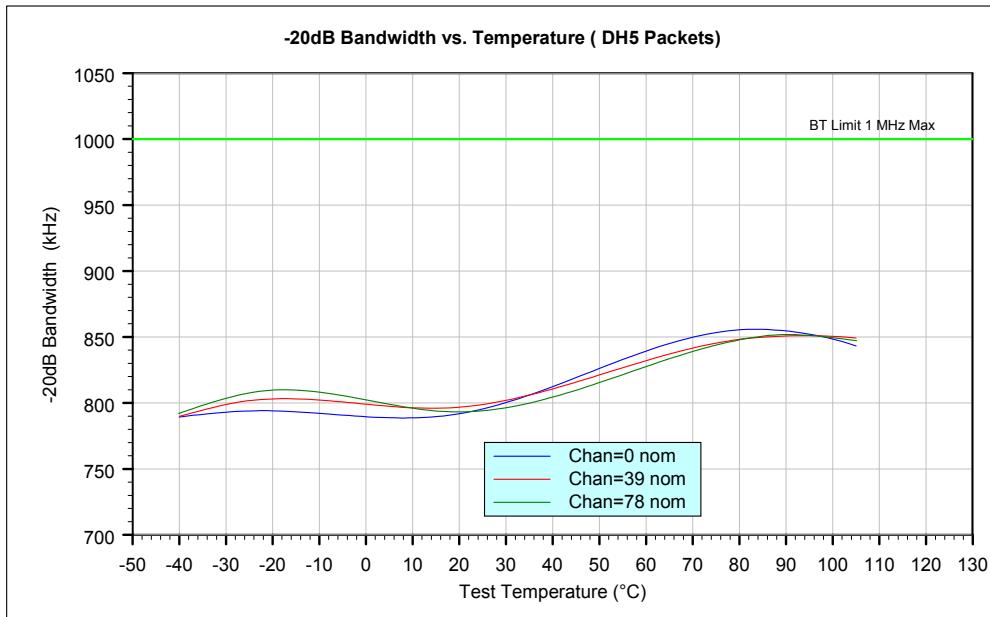


Figure 11.4: -20dB Bandwidth vs. Temperature (DH5 Packets)

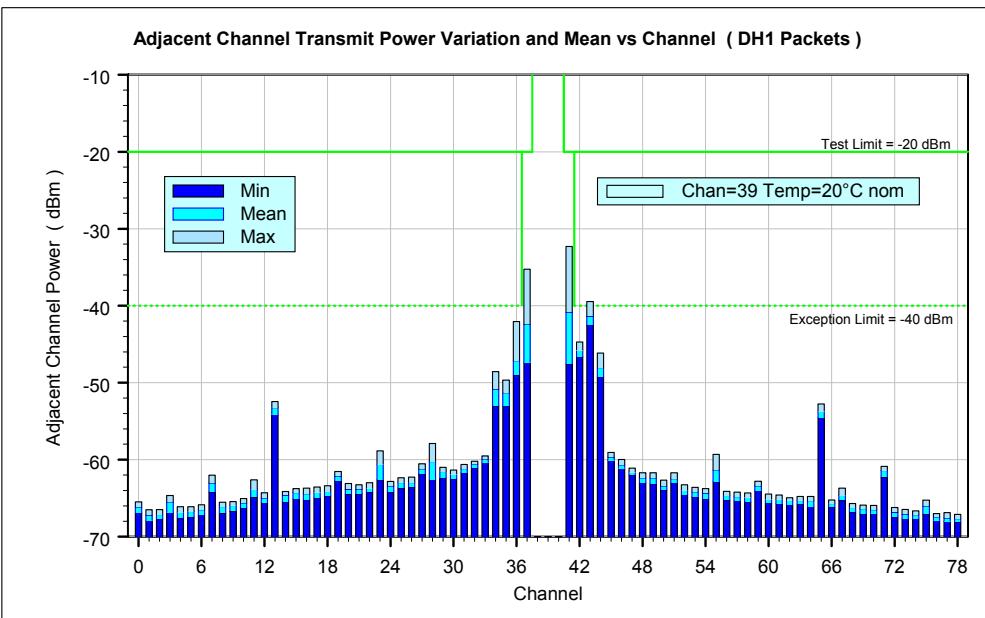


Figure 11.5: Adjacent Channel Transmit Power Variation and Mean vs. Channel (DH1 Packets)

Note:

Output power as per Figure 11.2

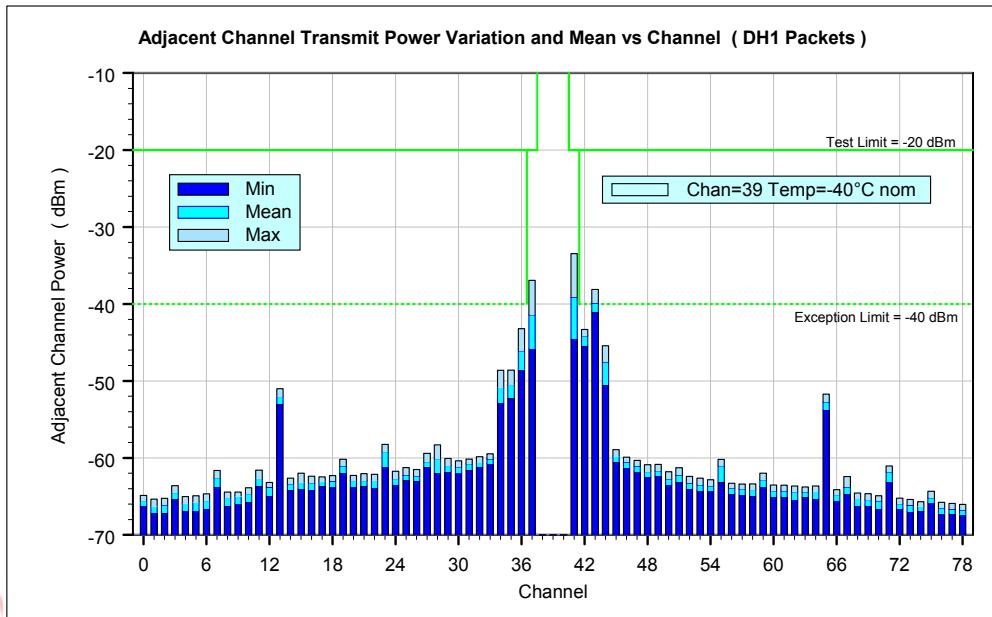


Figure 11.6: Adjacent Channel Transmit Power Variation and Mean vs. Channel (DH1 Packets), -40°C

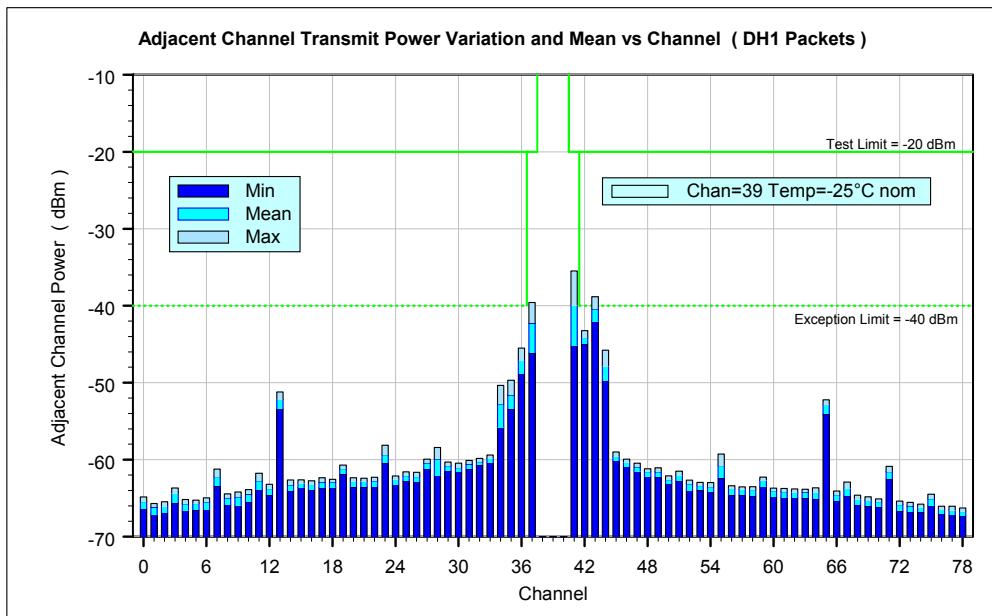


Figure 11.7: Adjacent Channel Transmit Power Variation and Mean vs. Channel (DH1 Packets), -25°C

Note:

Output power as per Figure 11.2

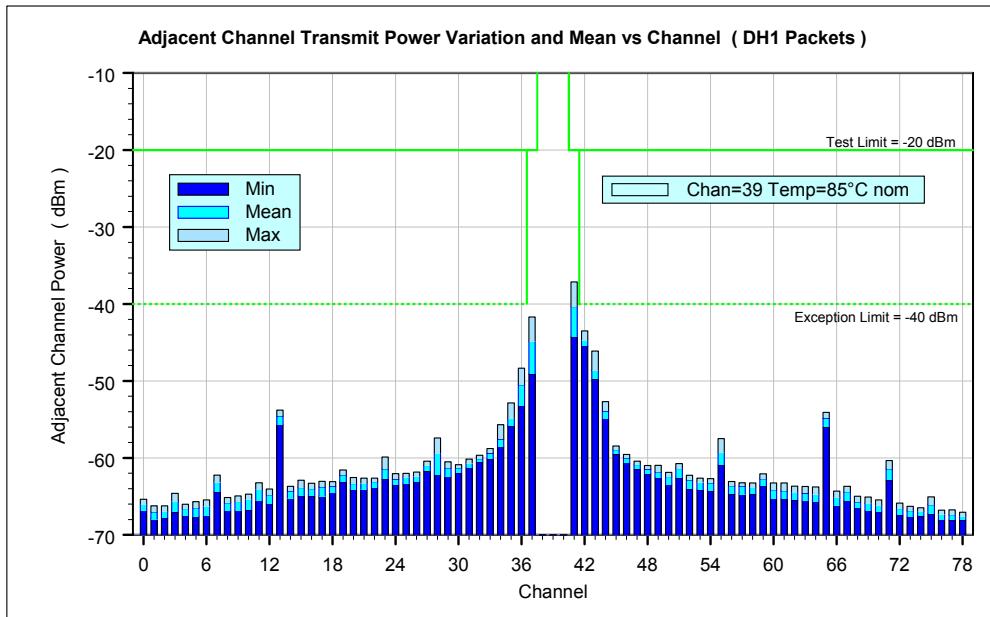


Figure 11.8: Adjacent Channel Transmit Power Variation and Mean vs. Channel (DH1 Packets), +85°C

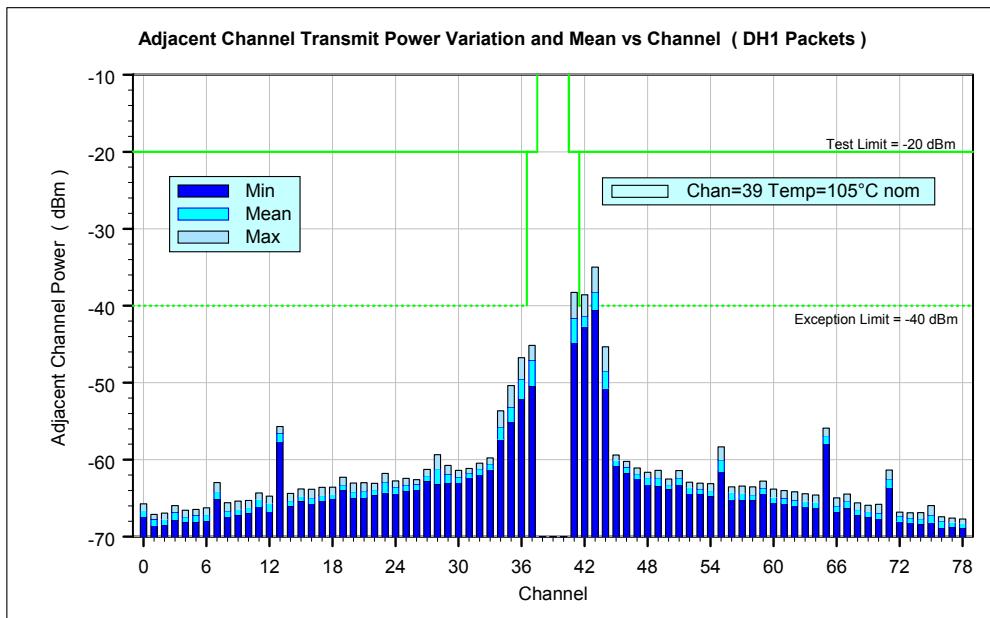


Figure 11.9: Adjacent Channel Transmit Power Variation and Mean vs. Channel (DH1 Packets), +105°C

Note:

Output power as per Figure 11.2

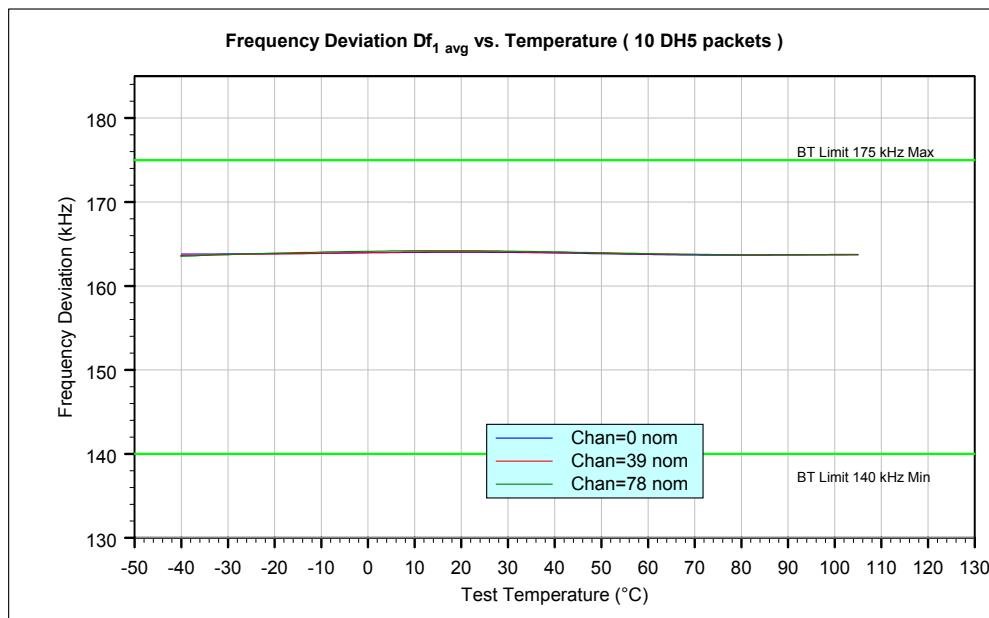


Figure 11.10: Frequency Deviation $\Delta f_1 \text{ avg}$ vs. Temperature (10 DH5 Packets)

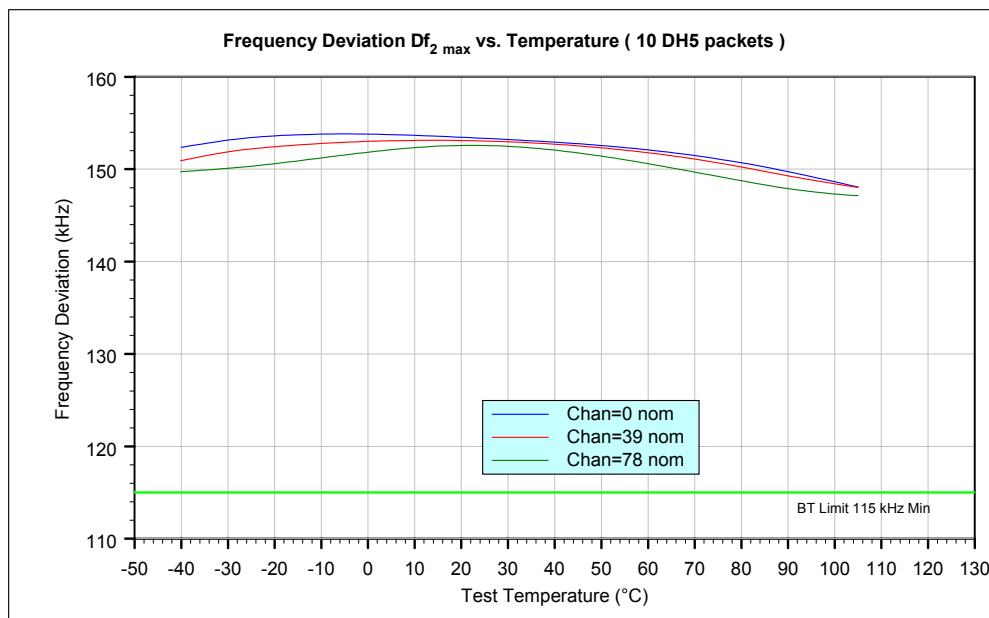


Figure 11.11: Frequency Deviation $\Delta f_2 \text{ max}$ vs. Temperature (10 DH5 Packets)

Note:

Output power as per Figure 11.2

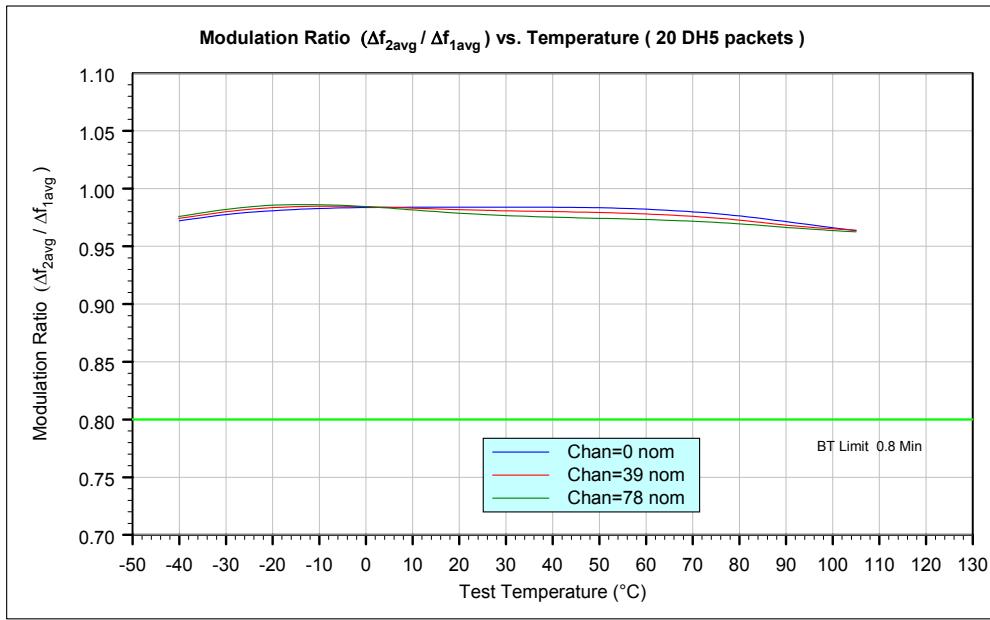


Figure 11.12: Modulation Ratio ($\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$) vs. Temperature (20 DH5 Packets)

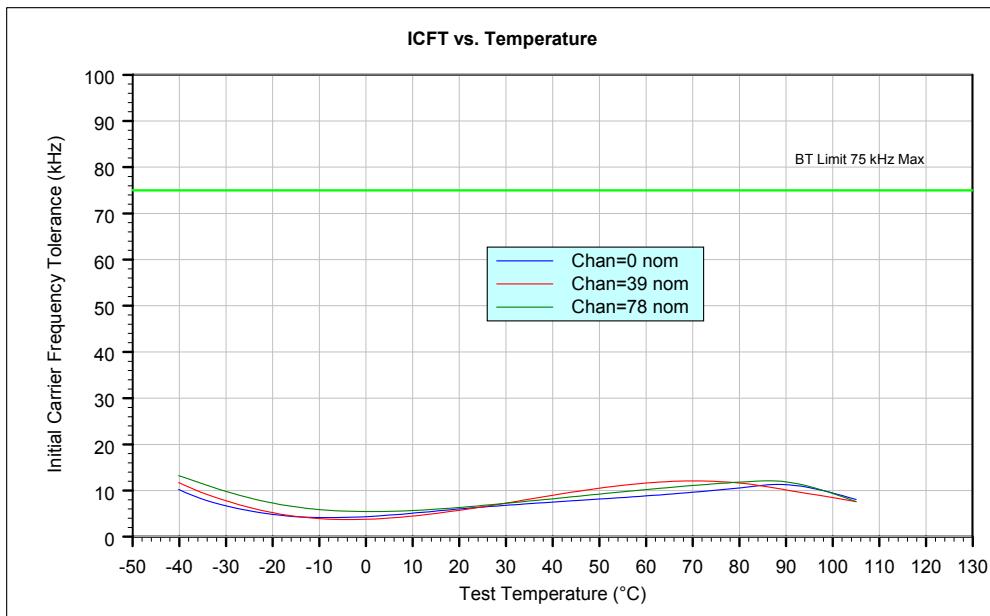


Figure 11.13: ICFT vs. Temperature

Note:

Output power as per Figure 11.2

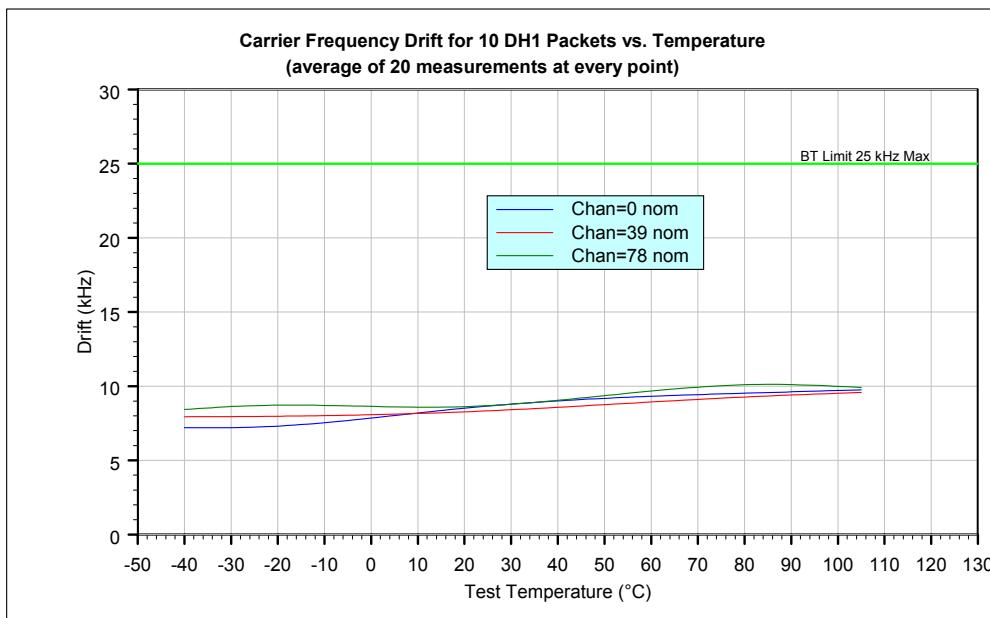


Figure 11.14: Carrier Frequency Drift for 10 DH1 Packets vs. Temperature

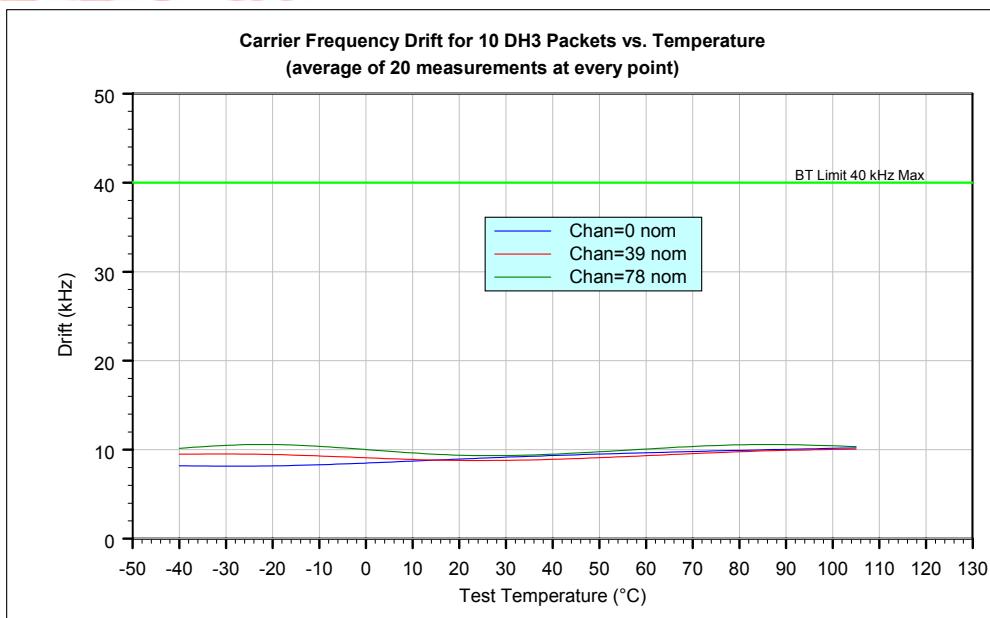


Figure 11.15: Carrier Frequency Drift for 10 DH3 Packets vs. Temperature

Note:

Output power as per Figure 11.2

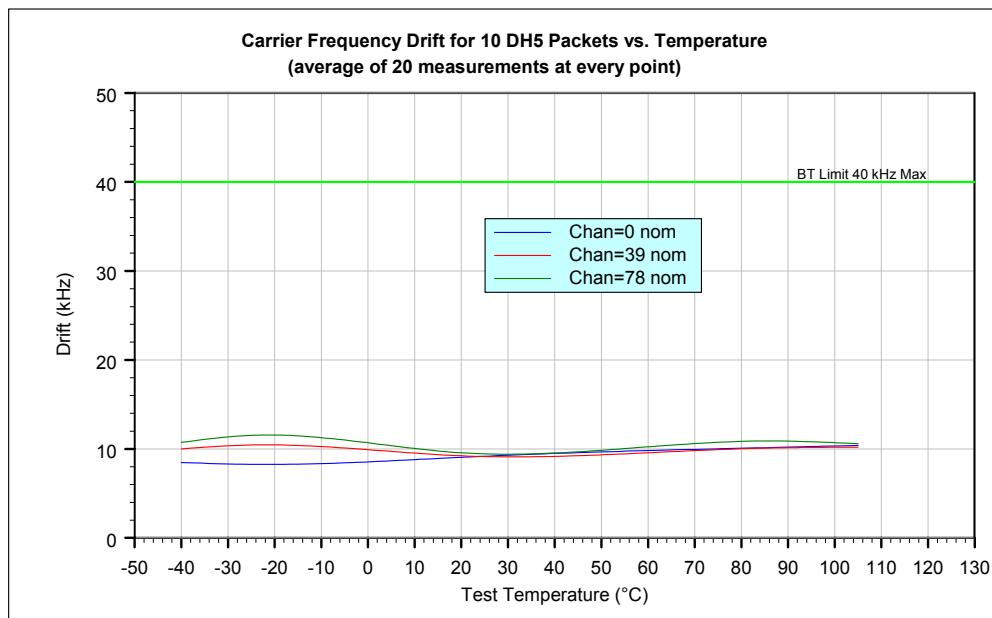


Figure 11.16: Frequency Drift for 10 DH5 Packets vs. Temperature

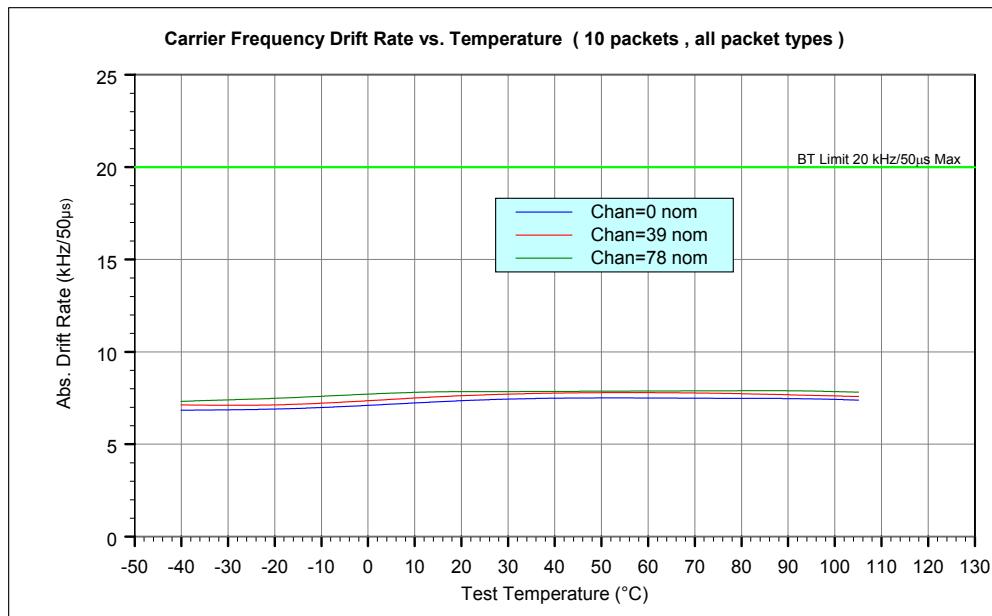


Figure 11.17: Carrier Frequency Drift Rate vs. Temperature (10 Packets, All Packet Types)

Note:

Output power as per Figure 11.2

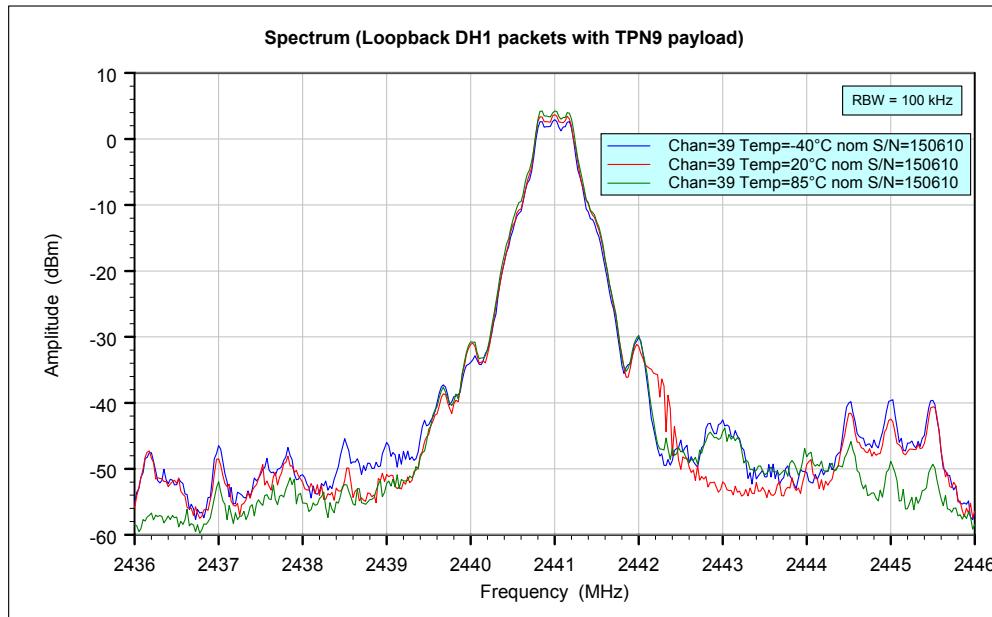


Figure 11.18: Spectrum (Loopback DH1 Packets with TPN9 Payload)

Note:

Output power as per Figure 11.2

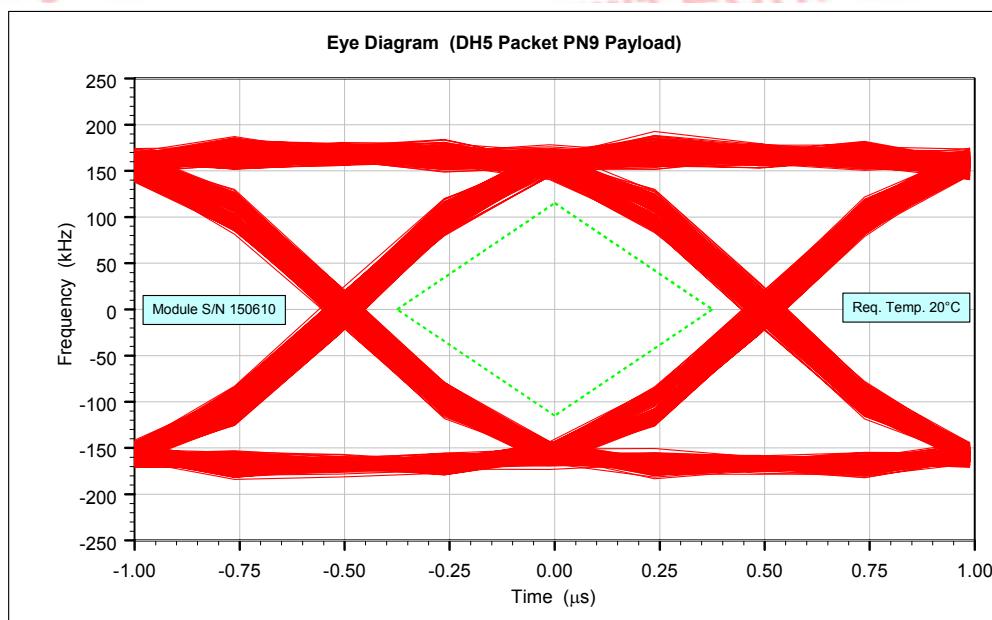


Figure 11.19: Eye Diagram (DH5 Packet PN9 Payload), 20°C

Notes:

Data: complete DH5 packet including preamble

Output power as per Figure 11.2

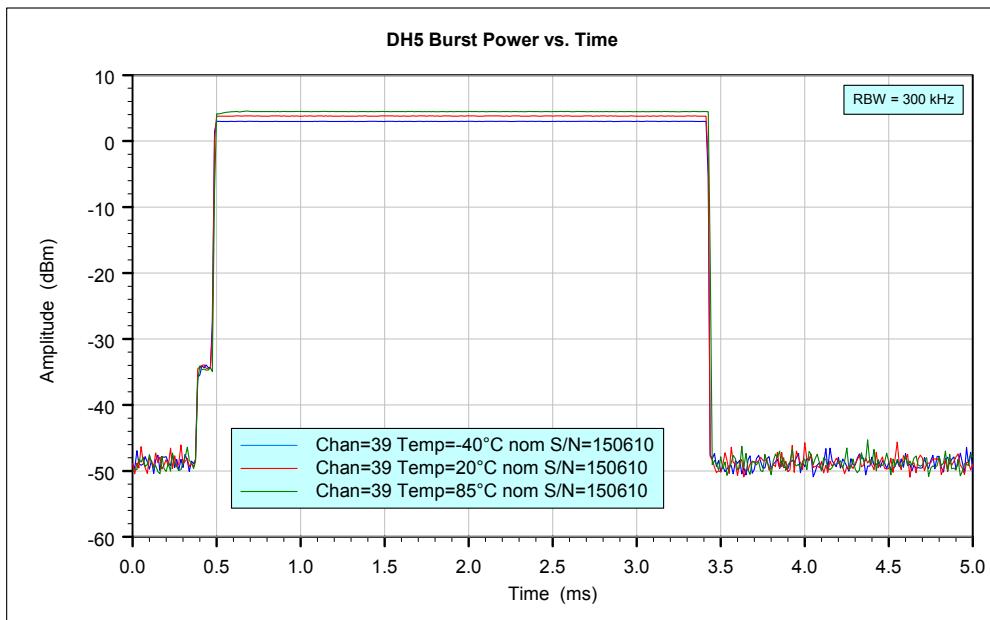


Figure 11.20: DH5 Burst Power vs. Time

Note:

Output power as per Figure 11.2

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11.2 Receiver Performance - Basic Data Rate

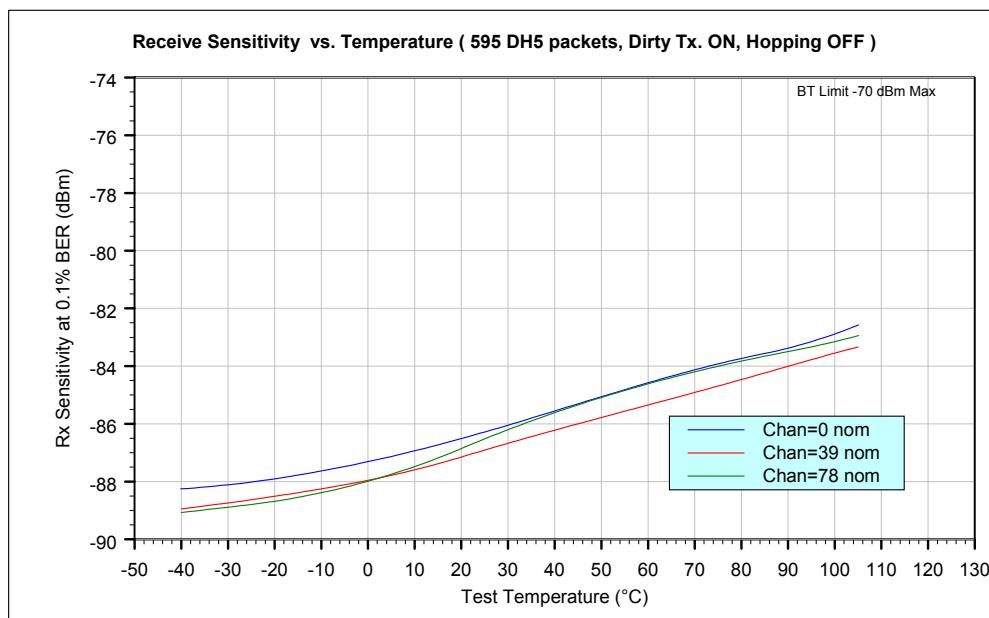


Figure 11.21: Receiver Sensitivity vs. Temperature (595 DH5 Packets)

Note:

DH5 packets with dirty transmitter on, Hopping off.

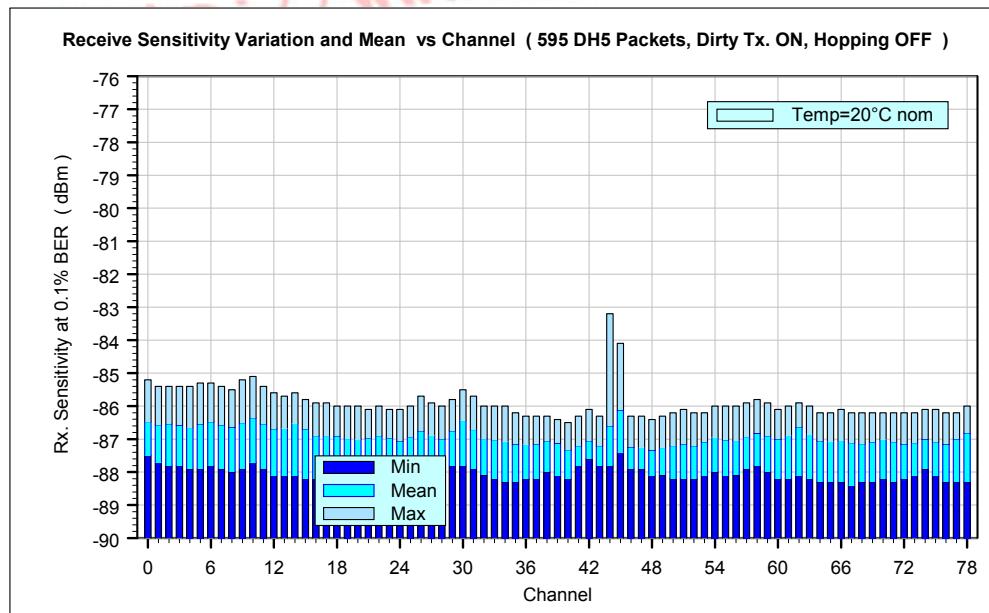


Figure 11.22: Receive Sensitivity Variation and Mean vs. Channel (595 DH5 Packets)

Note:

DH5 packets with dirty transmitter on, Hopping off.

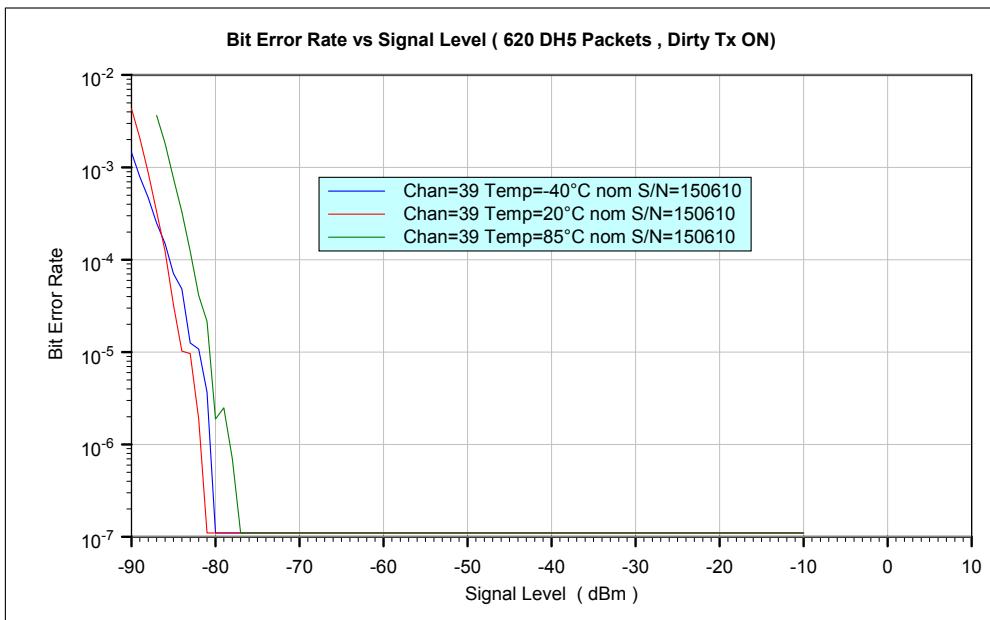


Figure 11.23: Bit Error Rate vs. Signal Level (620 DH5 Packets)

Note:

DH5 packets with dirty transmitter on, Hopping off.

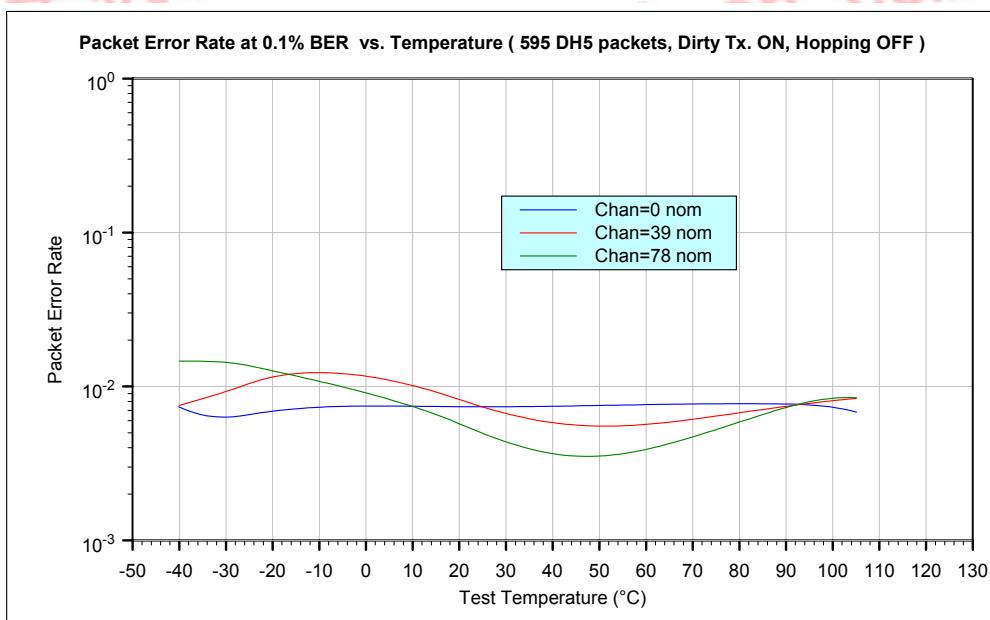


Figure 11.24: Packet Error Rate vs. Signal Level (620 DH5 Packets)

Note:

DH5 packets with dirty transmitter on, Hopping off.

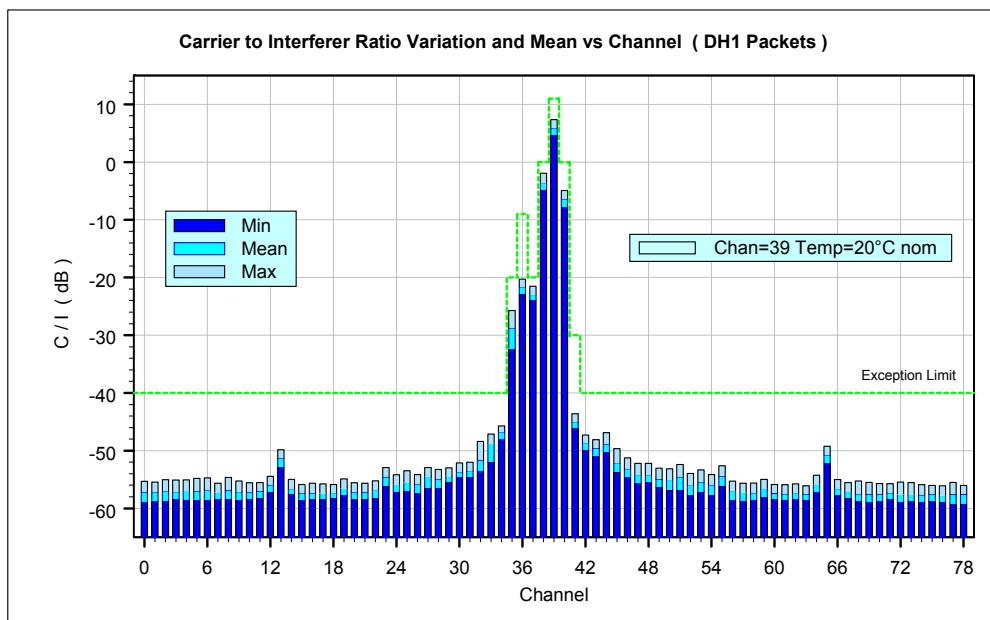


Figure 11.25: Carrier to Interferer Ratio and Mean vs. Channel (DH1 Packets), 20°C

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12 Typical Radio Performance - EDR

12.1 Transmitter Performance - Enhanced Data Rate

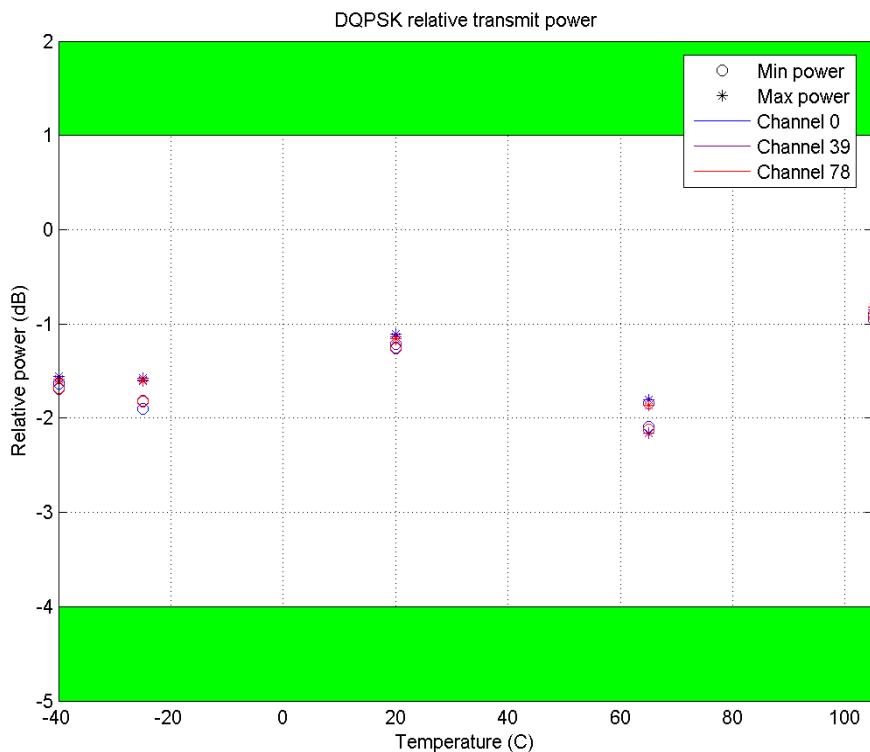


Figure 12.1: $\pi/4$ DQPSK Relative Transmit Power

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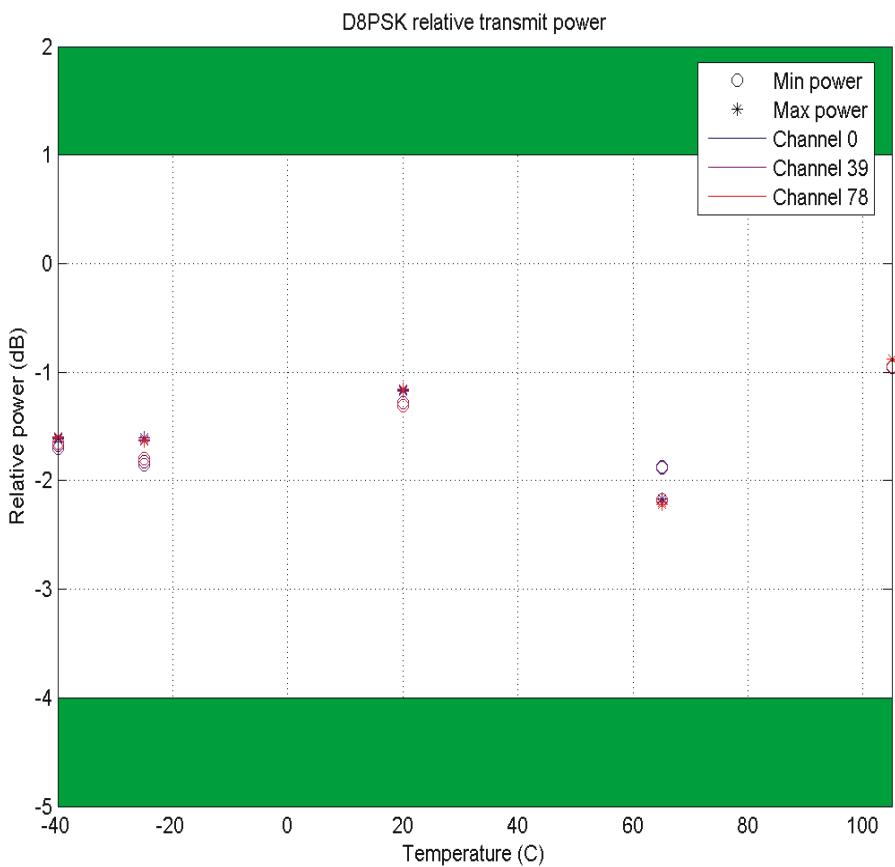


Figure 12.2: D8PSK Relative Transmit Power

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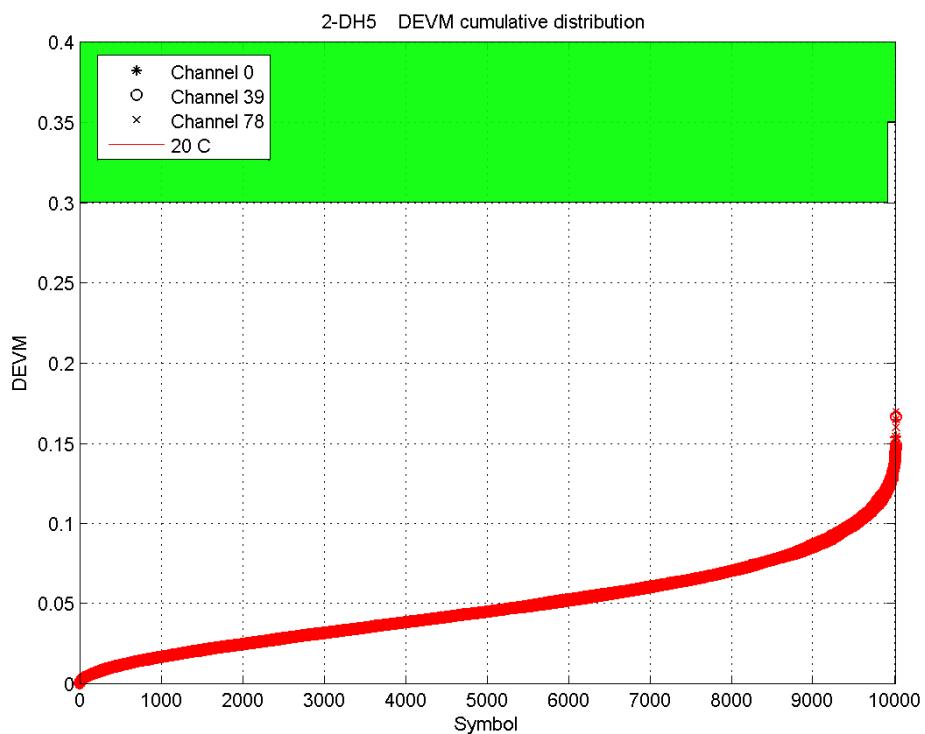


Figure 12.3: $\pi/4$ DQPSK 2-DH5 DEVM Cumulative Distribution, 20°C

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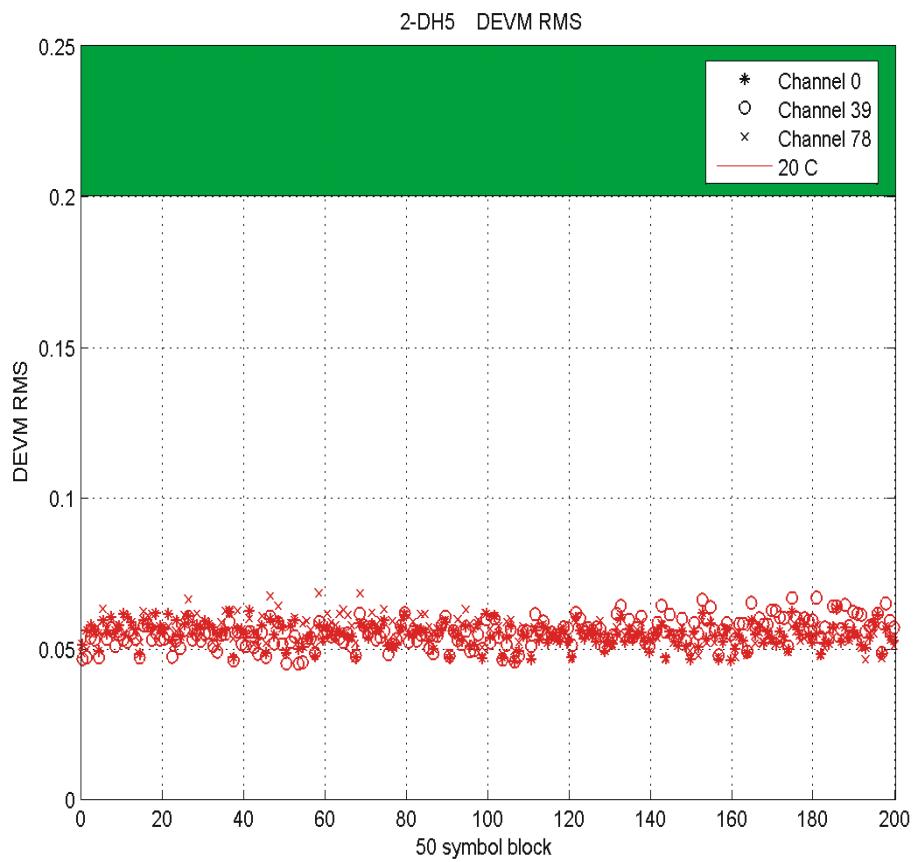


Figure 12.4: $\pi/4$ DQPSK 2-DH5 DEVM RMS, 20°C

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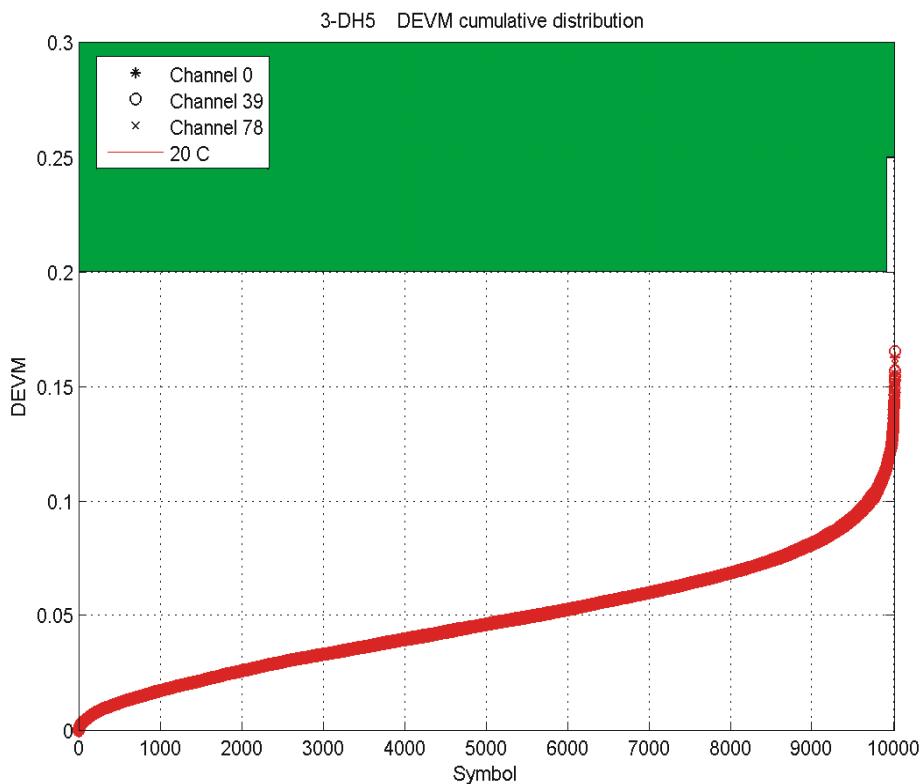


Figure 12.5: D8PSK 3-DH5 DEVM Cumulative Distribution, 20°C

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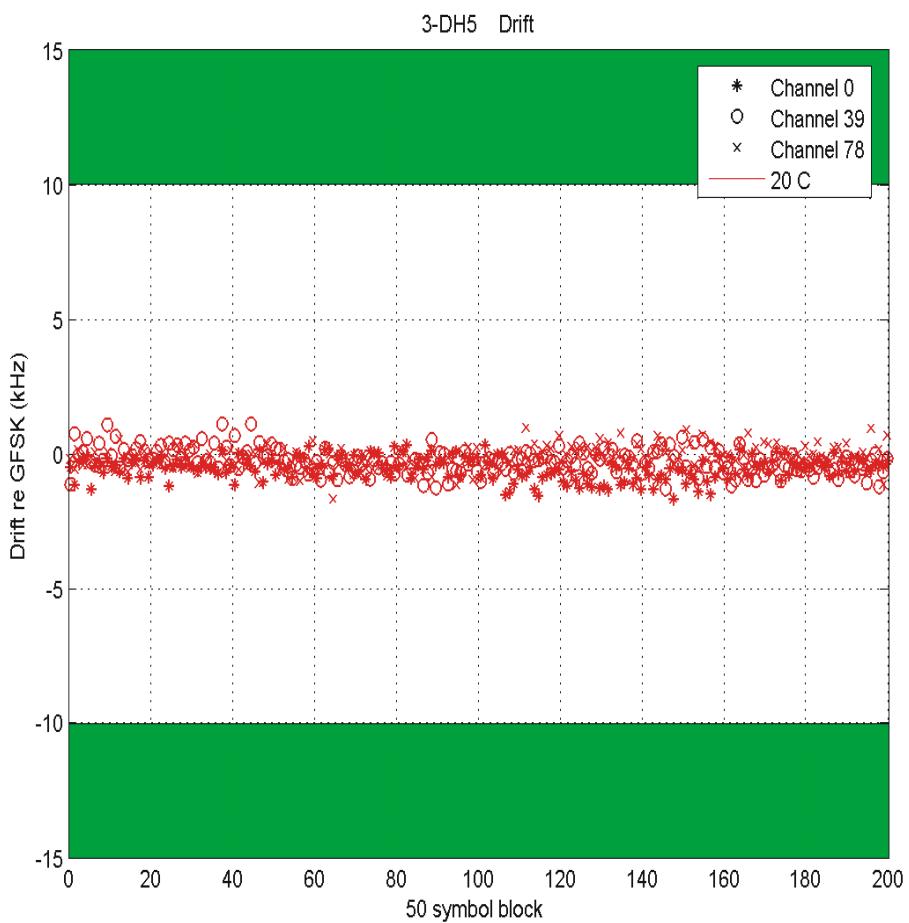


Figure 12.6: D8PSK 3-DH5 Drift, 20°C

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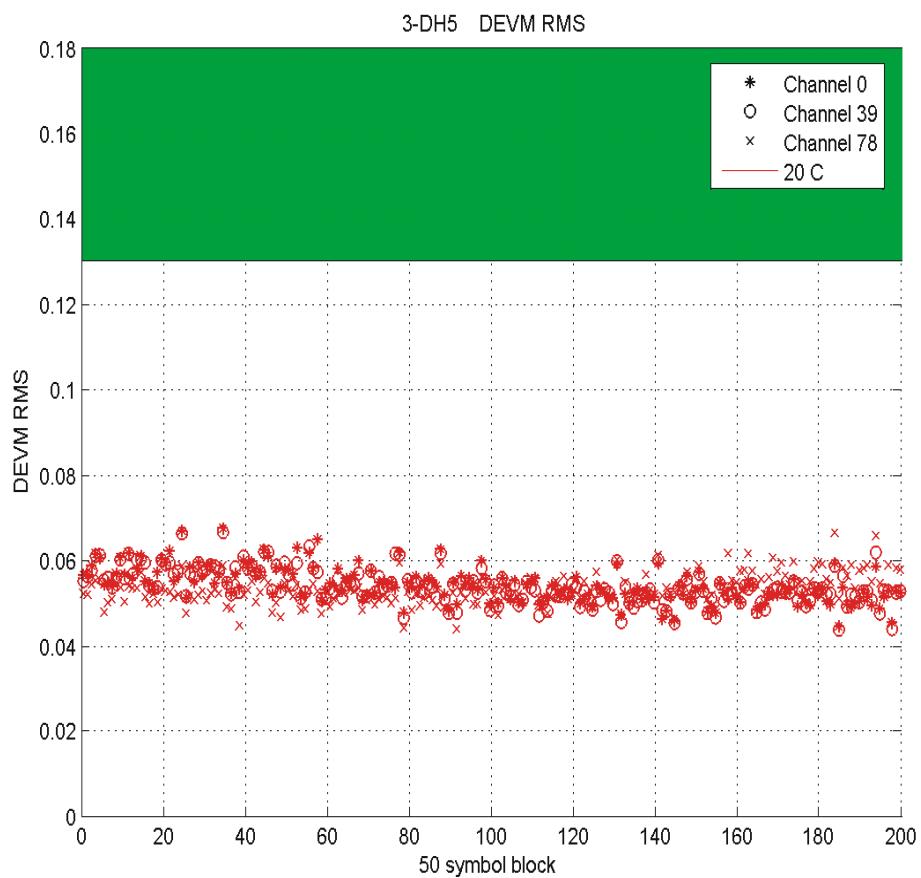


Figure 12.7: D8PSK 3-DH5 DEVM RMS, 20°C

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12.2 Receiver Performance - Enhanced Data Rate

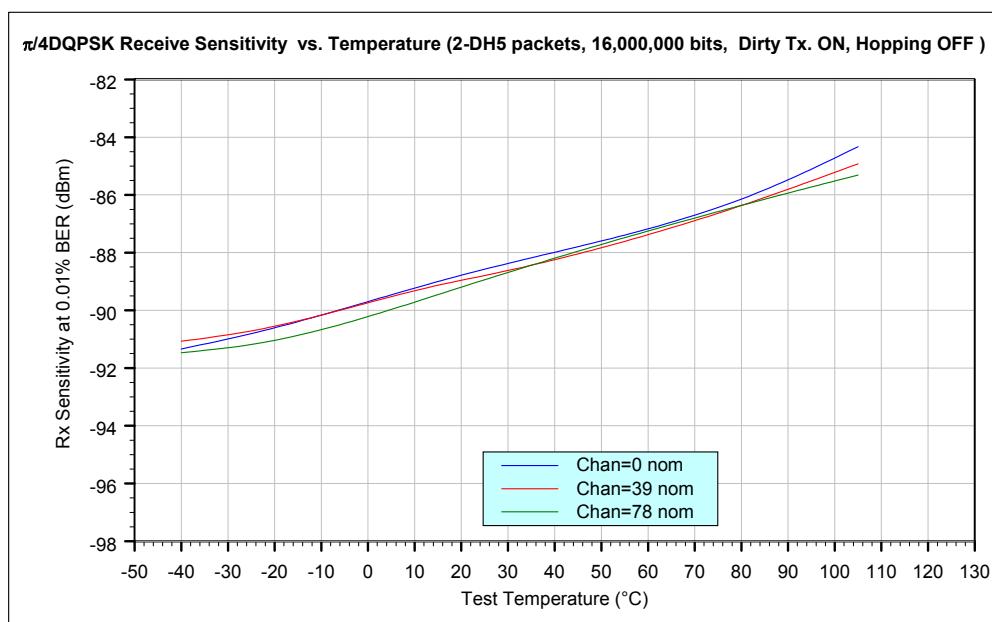


Figure 12.8: $\pi/4$ DQPSK Receive Sensitivity vs. Temperature, 20°C

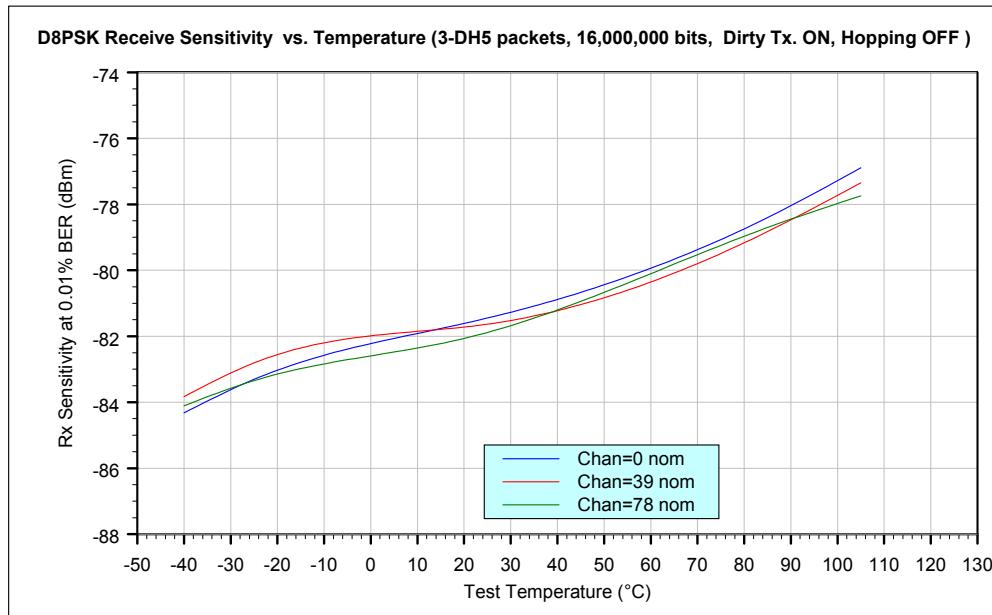


Figure 12.9: D8PSK Receive Sensitivity vs. Temperature, 20°C

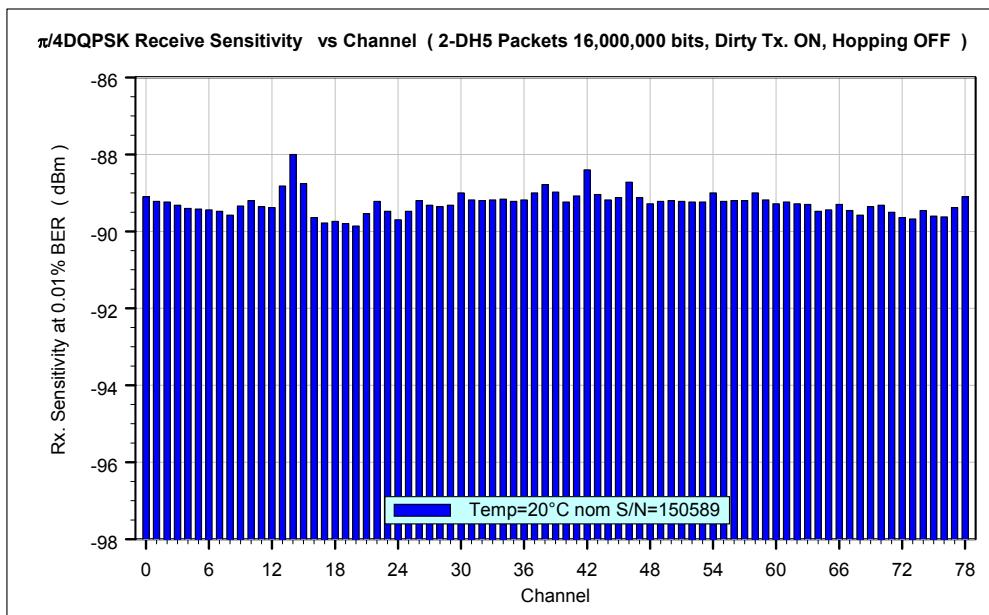


Figure 12.10: $\pi/4$ DQPSK Receive Sensitivity vs. Channel, 20°C

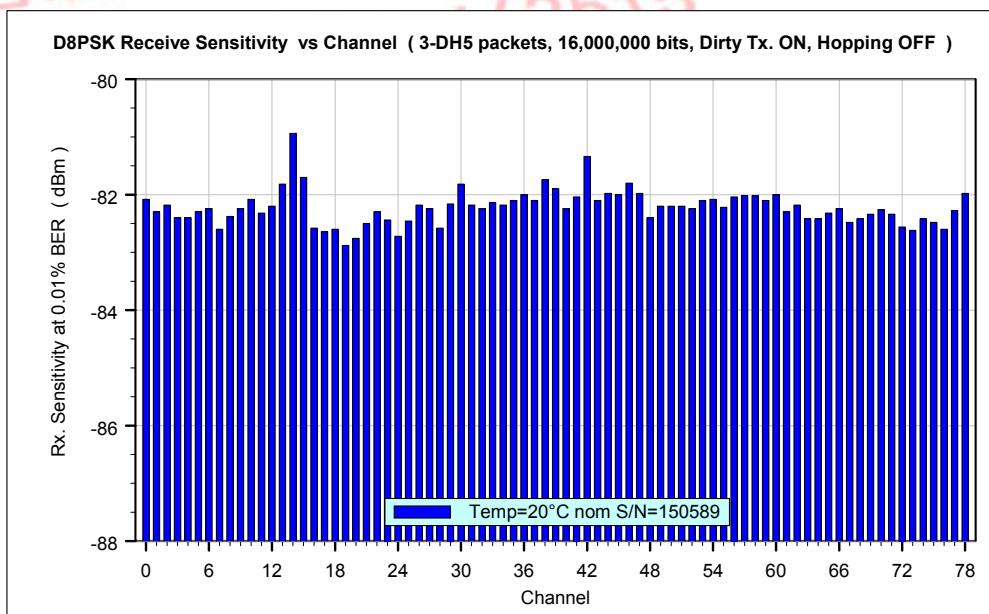


Figure 12.11: D8PSK Receive Sensitivity vs. Channel, 20°C

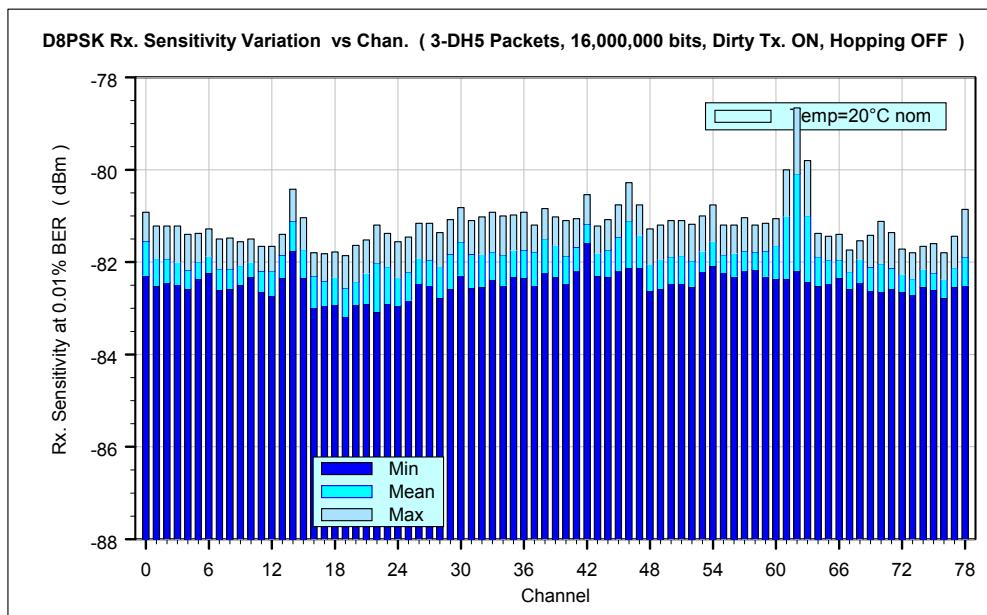


Figure 12.12: $\pi/4$ DQPSK Receive Sensitivity Variation vs. Channel, 20°C

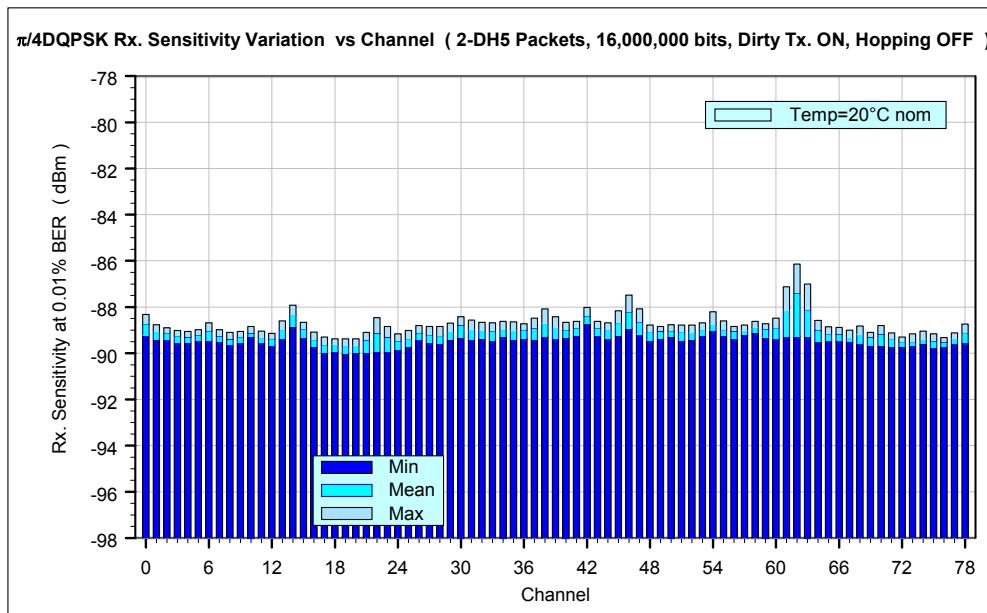


Figure 12.13: D8PSK Receive Sensitivity Variation vs. Channel, 20°C

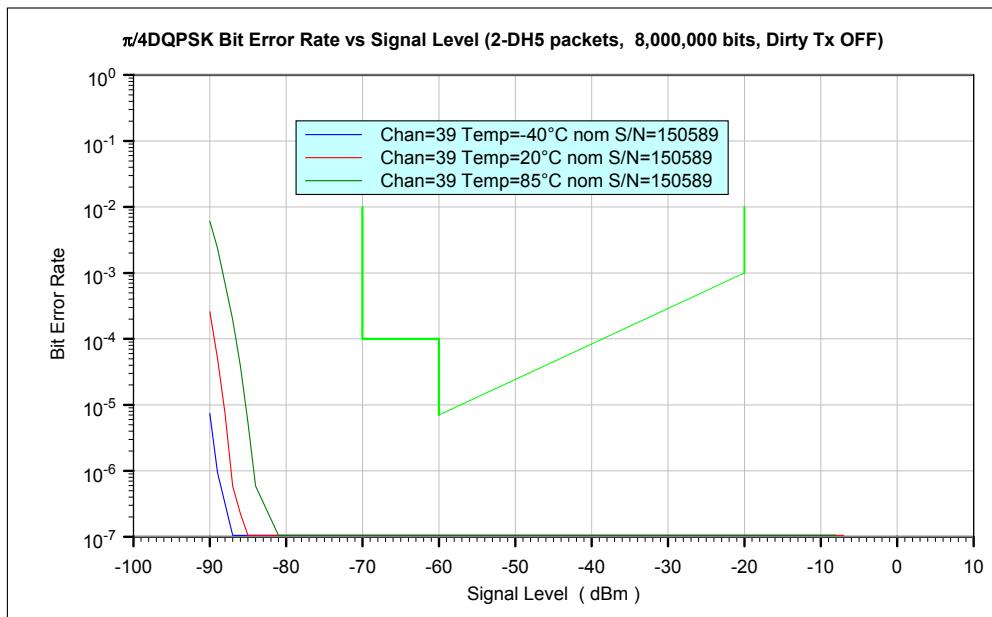


Figure 12.14: $\pi/4$ DQPSK Bit Error Rate vs. Signal Level

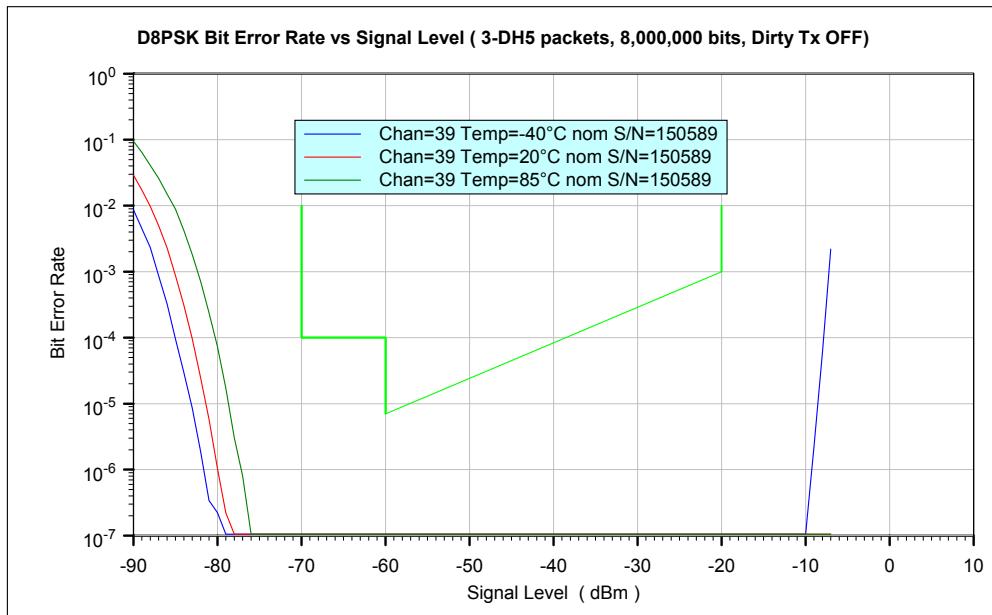
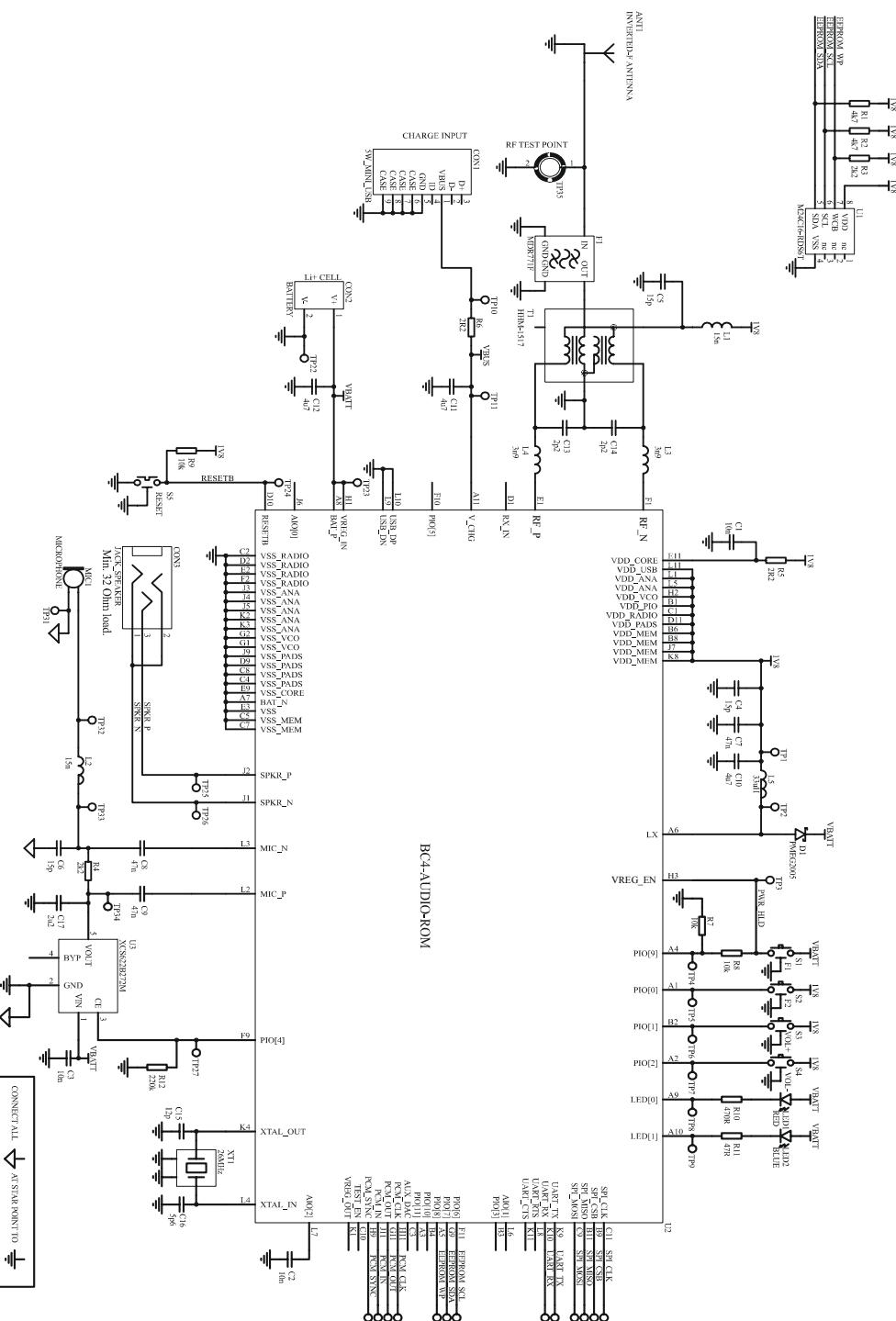


Figure 12.15: D8PSK Bit Error Rate vs. Signal Level

13 Application Schematic



14 Package Dimensions

14.1 8 x 8mm TFBGA 96-Ball Package

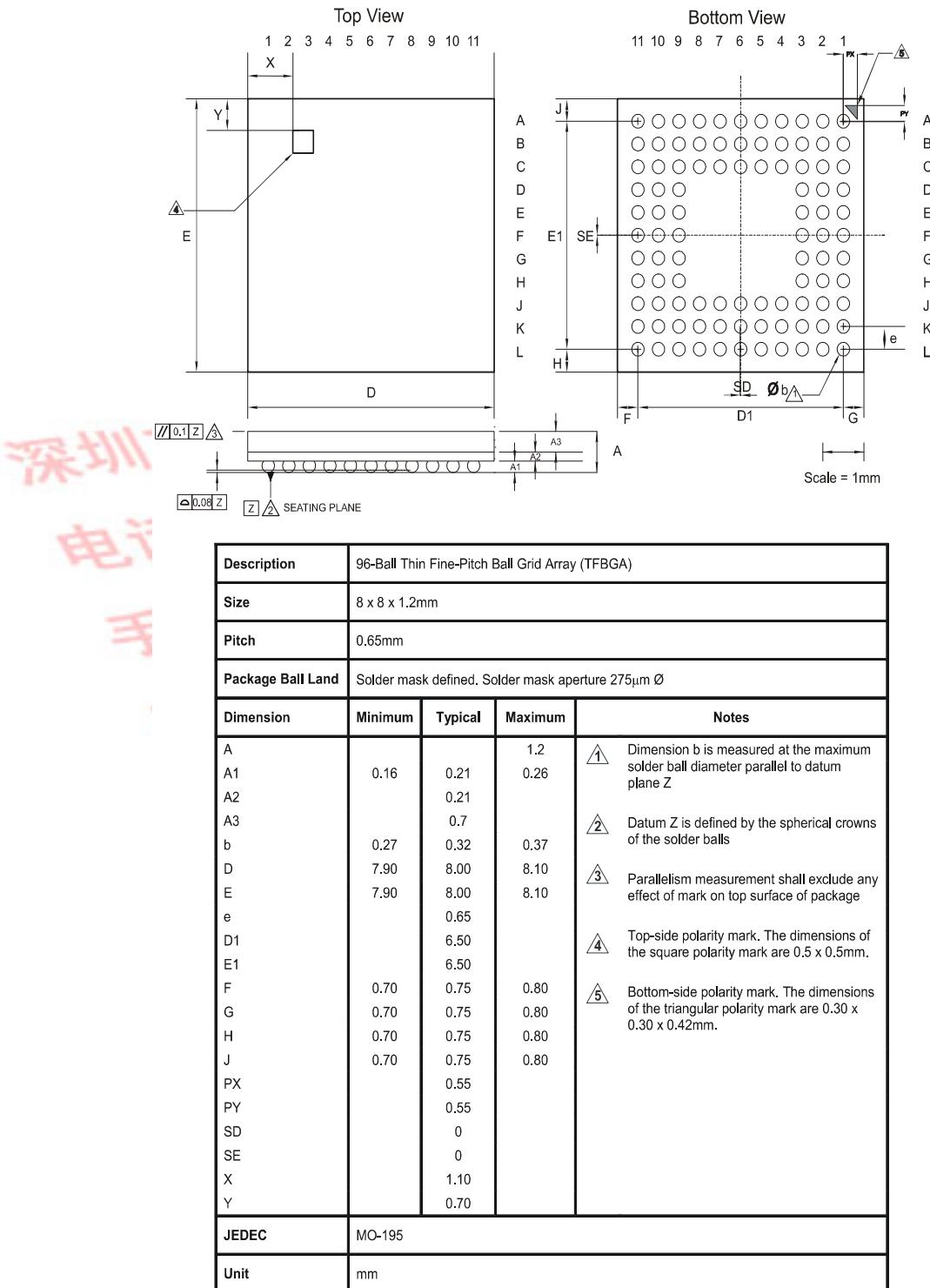


Figure 14.1: BlueCore4-Audio ROM 96-Ball TFBGA Package Dimensions

15 Tape and Reel Information

15.1 Tape Orientation and Dimensions

The general orientation of the TFBGA in the tape is as shown in Figure 15.1.

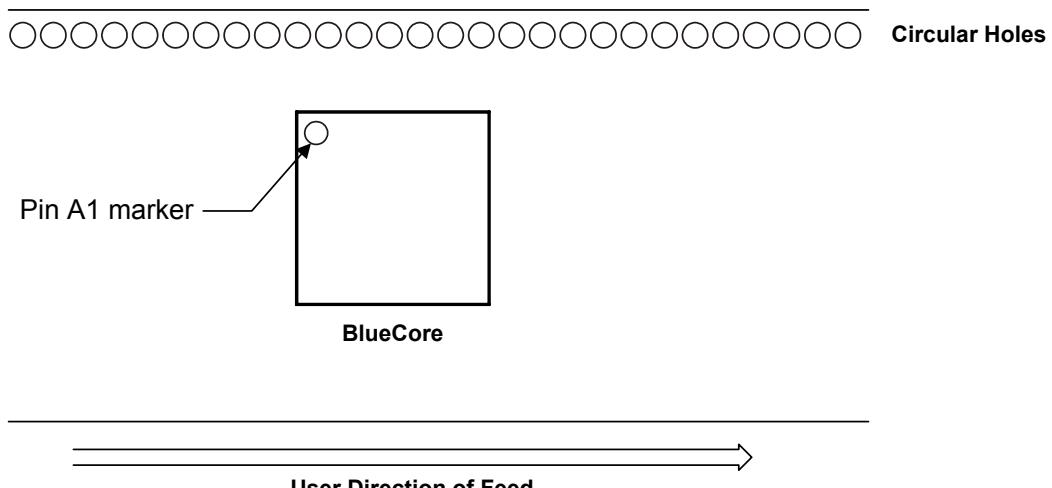
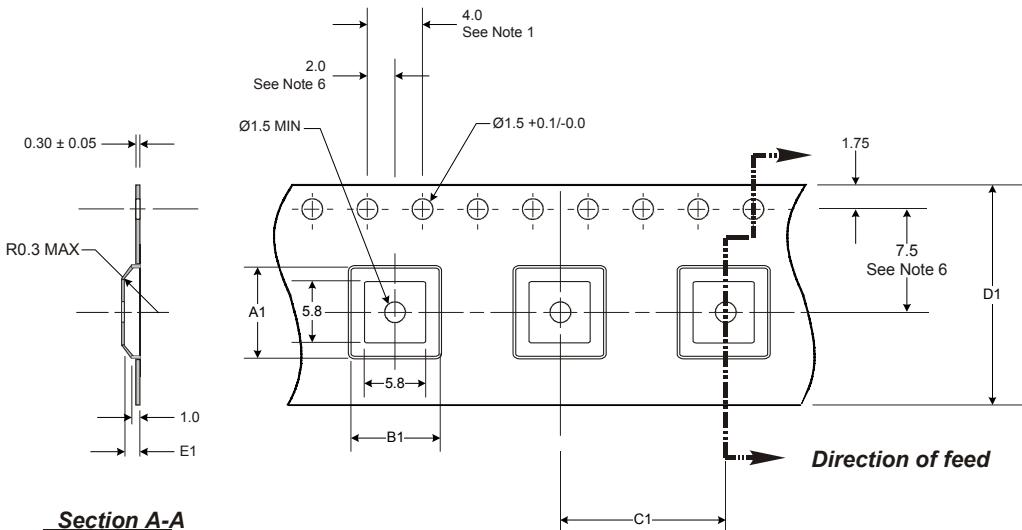


Figure 15.1: Tape and Reel Orientation

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15.2 Package Tape Dimensions

outlines the dimensions of the tape used for the BlueCore4-Audio ROM package.



Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 2.0 mm
2. Carrier camber not to exceed 1mm in 250mm.
3. Material: PS + C.
4. A1 and B1 measured on a plane 0.3mm above the bottom of the pocket.
5. E1 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

$A1 = 8.3\text{mm}$
 $B1 = 8.3\text{mm}$
 $C1 = 12.0\text{mm}$
 $D1 = 16.0 \pm 0.3\text{mm}$
 $E1 = 2.0\text{mm}$

Figure 15.2: Package Tape Dimensions

The cover tape has a total peel strength of 0.1N to 1.3N. The direction of the pull should be opposite the direction of the carrier tape such that the cover tape makes an angle of between 165° and 180° with the top of the carrier tape. The carrier and/or cover tape should be pulled with a velocity of 300±10mm during peeling.

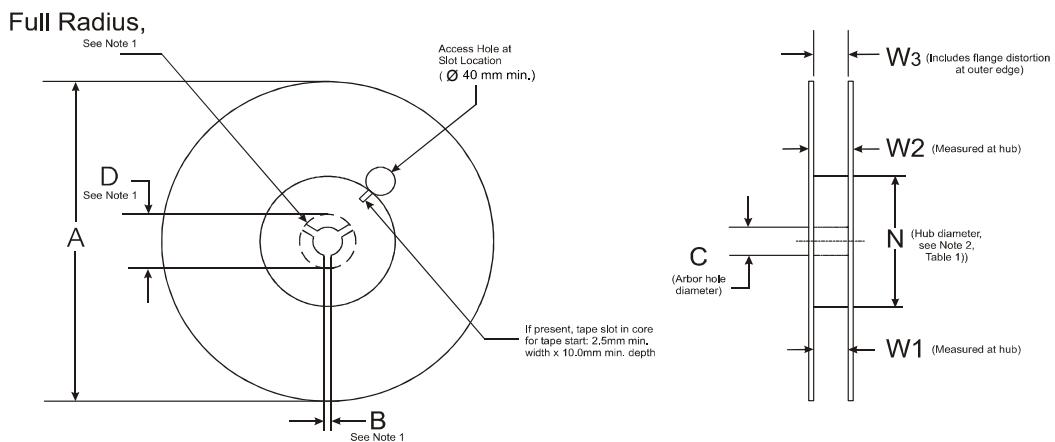
Maximum component rotation inside the cavity is 10°. The cavity pitch tolerance (dimension P1) is $\pm 0.1\text{mm}$.

The reel is made of high impact injection molded polystyrene. The carrier tape is made of polystyrene with carbon. The cover tape is made of antistatic polyester film and an antistatic heat activated adhesive coating.

15.3 Reel Information

Reel dimensions

(All dimensions in millimeters)



Notes:

1. Drive spokes optional; if used, dimensions B and D shall apply.
2. Maximum weight of reel and contents 13.6kg.

Figure 15.3: Reel Dimensions

| Package Type | Tape Width | A Max | B | C | D Min | N Min | W1 | W2 Max | W3 | | Units |
|---------------------|------------|-------|-----|---------------------|-------|-------|---------------------|--------|------|------|-------|
| | | | | | | | | | Min | Max | |
| 8 x 8 x 1.2mm TFBGA | 16 | 332 | 1.5 | 13.0 (+0.5/-0.2) | 20.2 | 50 | 16.4 (+2.0/-0.0) | 22.4 | 15.9 | 19.4 | mm |

Table 15.1: Reel Dimensions

| Package Type | Tape Width | A Max | B | C | D Min | N Min | W1 | W2 Max | W3 | | Units |
|-----------------------|------------|-------|-----|---------------------|-------|-------|---------------------|--------|------|------|-------|
| | | | | | | | | | Min | Max | |
| 10 x 10 x 1.6mm LFBGA | 16 | 332 | 1.5 | 13.0 (+0.5/-0.2) | 20.2 | 50 | 16.4 (+2.0/-0.0) | 22.4 | 15.9 | 19.4 | mm |

Table 15.2: Reel Dimensions

15.4 Dry Pack Packaging Information

The primary packed product is dry packed in accordance with Joint IPC / JEDEC J-STD-033. The number of units of desiccant added should ensure Moisture Sensitivity Level performance is not degraded. A humidity indicator card and a moisture sensitivity label are inserted into the bag prior to sealing.

All materials used in dry packing conform to EIA-541 and EIA-583.

Figure 15.4 shows reel dry packs.

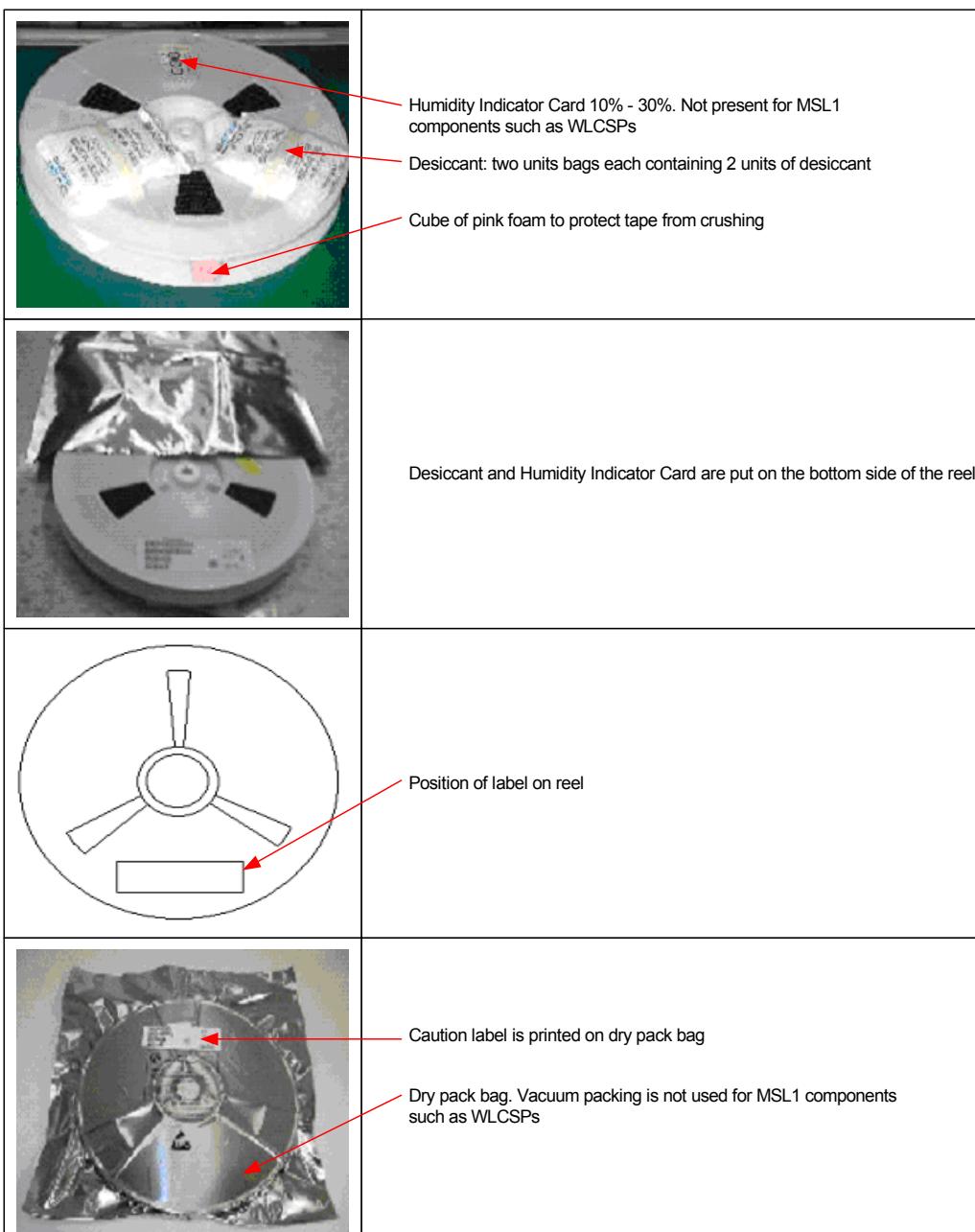


Figure 15.4: Tape and Reel Packaging

15.5 Moisture Sensitivity Level (MSL)

BlueCore4-Audio ROM is qualified to MSL3 in accordance with JEDEC J-STD-020.

Devices shipped in dry-pack bags will withstand storage in normal environmental conditions, such as 30°C and 60% RH for one year minimum as long as the dry-pack bag has not become punctured.

15.6 Baking Conditions

Devices may, if necessary, be re-baked at 125°C for 24 hours. If devices are still on the reel, which cannot withstand such high temperatures, they should be baked at 45°C for 192 hours at relative humidity less than 5%.

Solder wettability of parts will be unaffected by three such bakes.

15.7 Product Information

A product information label is placed on each reel, primary package and shipment package. An example of product information labels is shown in Figure 15.5.

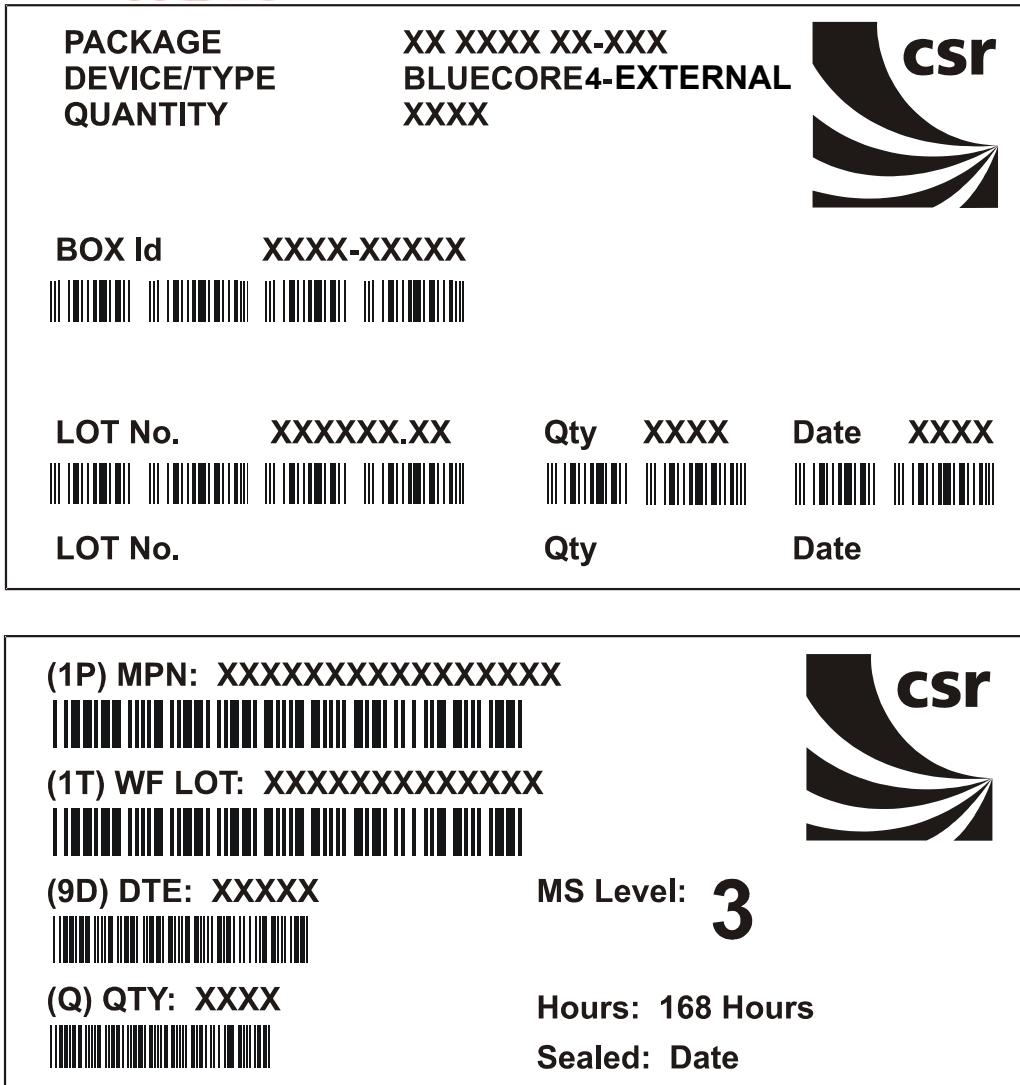


Figure 15.5: Example Product Information Labels

16 PCB Design and Assembly Considerations

16.1 8 x 8mm TFBGA 96-Ball Package

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8mm TFBGA 96-ball package:

- Non solder mask defined (NSMD) lands (that is, lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, via-in-pad technology should be used to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible – taking into consideration its current carrying and the radio frequency (RF) requirements.
- 35 μ m thick (1oz) copper lands are recommended rather than 17 μ m thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be the same as that on the package to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process because this adds to the final volume of solder in the joint, increasing its reliability.
- Where a nickel gold plating finish is used, the gold thickness should be kept below 0.5 μ m to prevent brittle gold/tin intermetallics forming in the solder.

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17 Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. **Preheat Zone** - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. **Equilibrium Zone** - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
3. **Reflow Zone** - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discolouration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. **Cooling Zone** - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

17.1 Typical Solder Re-flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

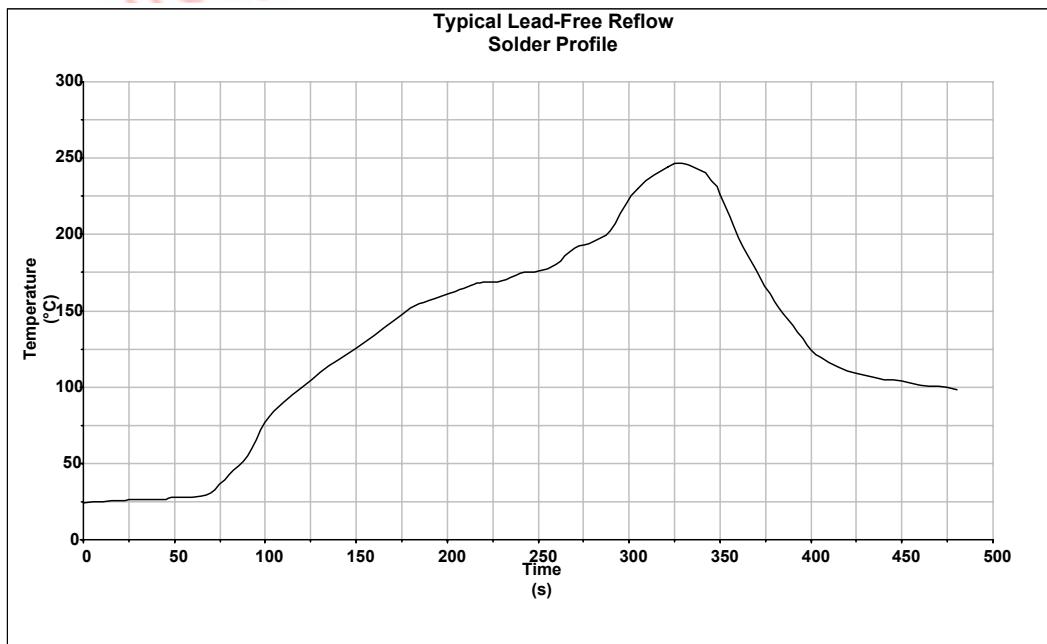


Figure 17.1: Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (245°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile.

Lead-free devices will withstand up to three reflows to a maximum temperature of 260°C.

18 RoHS Statement with a List of Banned Materials

18.1 RoHS Statement

BlueCore4-Audio ROM where explicitly stated in this Data Book meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

18.1.1 List of Banned Materials

The following banned substances are not present in BlueCore4-Audio ROM which is compliant with RoHS:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- PBB (Polybrominated Bi-Phenyl)
- PBDE (Polybrominated Diphenyl Ether)

In addition, BlueCore4-Audio ROM is free from the following substances:

- PVC (Poly Vinyl Chloride)

19 Ordering Information

19.1 BlueCore4-Audio ROM

| Interface Version | Package | | | Order Number |
|-------------------|----------------------------|---------------|-----------------|--------------------|
| | Type | Size | Shipment Method | |
| UART and USB | 96-Ball TFBGA (Pb free) | 8 x 8 x 1.2mm | Tape and reel | BC413159AXX-IPK-E4 |

Minimum Order Engineering Sample Quantity

2kpcs taped and reeled

Minimum Order Production Quantity

2kpcs taped and reeled

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e-mail: sales@csr.com

To contact a CSR representative, go to www.csr.com/contacts.htm

21 Document References

| Document | Reference |
|---|----------------------------------|
| Specification of the Bluetooth System | v2.0 + EDR, 04 November 2004 |
| Universal Serial Bus Specification | v2.0, 27 April 2000 |
| Selection of I ² C EEPROMS for Use with BlueCore | bcore-an008Pb, 30 September 2003 |
| Lithium Ion/Polymer Battery Safety Information Note | bcore-an-057P, 25 November 2004 |
| EDR RF Test Specification v2.0.E.2 | v2.0.E.20, D07r22, 16 March 2004 |
| RF Prototyping Specification for Enhanced Data Rate IP | v.90, r29, 2004 |

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22 Terms and Definitions

| | |
|---------------|--|
| ACL | Asynchronous Connection-Less, a Bluetooth data packet type |
| ADC | Analogue to Digital Converter |
| AGC | Automatic Gain Control |
| A-law | Audio encoding standard |
| API | Application Programming Interface |
| ASIC | Application Specific Integrated Circuit |
| BCSP | BlueCore™ Serial Protocol |
| BER | Bit Error Rate. Used to measure the quality of a link |
| BIST | Built-In Self-Test |
| BlueCore™ | Group term for CSR's range of Bluetooth chips |
| Bluetooth™ | Set of technologies providing audio and data transfer over short-range radio connections |
| BMC | Burst Mode Controller |
| CMOS | Complementary Metal Oxide Semiconductor |
| CODEC | Coder Decoder |
| CQDDR | Channel Quality Driven Data Rate |
| CSB | Chip Select (Active Low) |
| CSR | Cambridge Silicon Radio |
| CTS | Clear to Send |
| CVSD | Continuous Variable Slope Delta Modulation |
| DAC | Digital to Analogue Converter |
| dBm | Decibels relative to 1mW |
| DC | Direct Current |
| DEVM | Differential Error Vector Magnitude |
| DFU | Device Firmware Upgrade |
| DSP | Digital Signal Processor |
| EDR | Enhanced Data Rate |
| ESR | Equivalent Series Resistance |
| FSK | Frequency Shift Keying |
| GSM | Global System for Mobile communications |
| HCI | Host Controller Interface |
| HID | Human Interface Device |
| IF | Intermediate Frequency |
| IQ Modulation | In-Phase and Quadrature Modulation |
| ISDN | Integrated Services Digital Network |
| ISM | Industrial, Scientific and Medical |
| ksamples/s | KiloSamples Per Second |
| L2CAP | Logical Link Control and Adaptation Protocol (protocol layer) |

| | |
|------------------|---|
| LC | Link Controller |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| LMP | Link Manager Protocol |
| LNA | Low Noise Amplifier |
| LSB | Least-Significant Bit |
| MCU | MicroController Unit |
| μ -law | Audio Encoding Standard |
| MISO | Master In Serial Out |
| MMU | Memory Management Unit |
| MSL | Moisture Sensitivity Level |
| OHCI | Open Host Controller Interface |
| PA | Power Amplifier |
| PCM | Pulse Code Modulation. Refers to digital voice data |
| Persistent Store | Storage of BlueCore's configuration values in non-volatile memory |
| PIO | Parallel Input Output |
| PLL | Phase Lock Loop |
| ppm | parts per million |
| PS Key | Persistent Store Key |
| RAM | Random Access Memory |
| RF | Radio Frequency |
| RFCOMM | Protocol layer providing serial port emulation over L2CAP |
| RISC | Reduced Instruction Set Computer |
| rms | root mean squared |
| RoHS | The Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC) |
| RSSI | Receive Signal Strength Indication |
| RTS | Ready To Send |
| RX | Receive or Receiver |
| SCO | Synchronous Connection-Oriented. Voice oriented Bluetooth packet |
| SDK | Software Development Kit |
| SDP | Service Discovery Protocol |
| SIG | Special Interest Group |
| SPI | Serial Peripheral Interface |
| SSI | Synchronous Serial Interface |
| TBD | To Be Defined |
| TX | Transmit or Transmitter |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus or Upper Side Band (depending on context) |
| VCO | Voltage Controlled Oscillator |

| | |
|--------|--|
| VFBGA | Very Fine Ball Grid Array |
| VM | Virtual Machine |
| W-CDMA | Wideband Code Division Multiple Access |

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23 Document History

| Date | Revision | Reason for Change |
|---------|----------|--|
| MAR 05 | a | Original publication of this document. (CSR reference: BC413159A-ds-001Pa) |
| MAR 05 | b | Updated Order Number in Ordering Information section |
| APR 05 | c | VDD_MEM description updated, 8 x 8 TFBGA Package Information, Device Terminal Functions Correction made to I/O Parallel Ports, Device Terminal Descriptions |
| MAY 05 | d | Power Consumption added to Electrical Characteristics |
| JULY 05 | e | Amendment to note concerning VREG_EN and VREG_IN in Linear Regulator table, Electrical Characteristics section Updated Enhanced Data Rate section. Changed title of Record of Changes to Document History; changed title of Acronyms and Abbreviations to Terms and Definitions Changed copyright information on Status Information page Updated Contact Information |
| OCT 05 | f | Document moved to Pre-Production Status Added Application Schematic Removed Device Firmware Upgrade subsection, CSR Bluetooth Software Stacks |
| NOV 05 | g | Switch-mode Regulator and Linear Regulator updated, Power Supplies, Device Terminal Descriptions |
| FEB 06 | h | Document moved to Production Status Major upgrades to Data Book include: Updated Radio Characteristics - Basic Data Rate section Addition of Typical Radio Performance - Basic Data Rate section Addition of Tape and Reel Information and PCB Design and Assembly Consideration sections |
| MAY 06 | i | Correction to pin descriptions for V_CHG (A11), BAT_P (A8), BAT_N (A7) Device Terminal Functions in Package Information. Correction to Battery Charger, Description of Functional Blocks |

BlueCore™4-Audio ROM

Product Data Book

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