Features

- 6th generation 1-mic CVC audio enhancements
- A2DP v1.2 for high-quality mono music streaming
- Supports mSBC wideband speech codec
- Programmable audio prompts: available from either EEPROM or a low-cost SPI flash
- Bidirectional noise reduction: *Hear and Be Heard*
- Long-tail echo cancellation for low-cost speakerphones and car-kits
- Low power consumption: over 11 hours talk time from a 120mAhr battery
- Advanced multipoint support: enables a headset (HFP) connection to 2 phones for voice
- Multipoint A2DP streaming: enables a mono headset (A2DP) connection to 2 A2DP source devices for music playback
- Secure simple pairing, CSR's proximity pairing and CSR's proximity connection
- 64MIPS Kalimba DSP coprocessor
- HFP v1.5 and HSP v1.2.
- Integrated linear and switch-mode regulators
- 150mA lithium battery charger, with fast charge and external boost charge for a total 240mA
- High-quality mono codec with 95dB SNR DAC
- 48-lead 7 x 7 x 0.9mm, 0.5mm pitch QFN, pin compatible with BC6140™ QFN and BC6130™ QFN
- Green (RoHS compliant and no antimony or halogenated flame retardants)

BlueCore® BC6145™ QFN

1-mic CVC Mono Headset Solution
Advanced Echo and Noise Cancellation
Fully Qualified Single-chip
Bluetooth® v3.0 System

Production Information

BC6145A04

Issue 2

BC6145 QFN Data Sheet

General Description

BlueCore® BC6145™ QFN is a low-cost fully-featured ROM IC solution for Bluetooth mono headsets with extremely low power consumption. The BC6145 QFN ensures increased speech clarity and improves intelligibility through spectral enhancement, with the bidirectional noise reduction *Hear and Be Heard* feature.

BC6145 QFN reduces the number of external components required, minimising production costs. It includes a Bluetooth radio, baseband, Kalimba DSP, DAC/ADC, switch-mode power supply and battery charger in a QFN package for low-cost designs.

The Kalimba DSP coprocessor supports enhanced audio applications. A2DP streaming enables music playback on a mono headset.

Applications

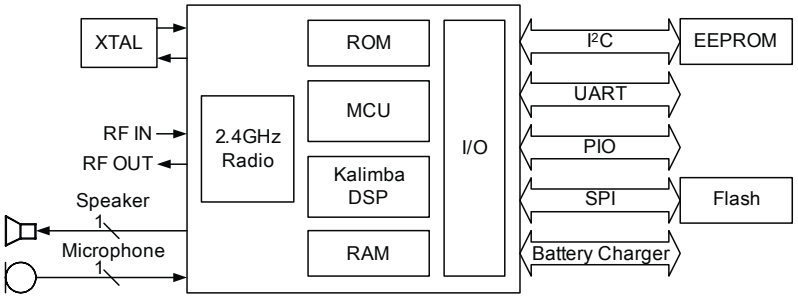
- BC6145 QFN DSP mono headset solution
- Low-cost speakerphones and car-kits

BC6145 QFN includes CVC single-microphone echo and noise reduction, which reduces headset echo enabling the headset-user to be heard more clearly. A low-power wind noise reduction feature improves intelligibility in windy environments.

BC6145 QFN supports secure simple pairing which simplifies the pairing process and makes it easier to use a Bluetooth headset.

The device includes auto-calibration and BIST routines to simplify development, type approval and production test.

See *CSR Glossary* at www.csrsupport.com.



Device Details

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- Bluetooth v3.0 specification compliant

Transmitter

- 8.5dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range typically >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Receiver sensitivity of -91dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 26MHz

Baseband and Software

- Support for Bluetooth v3.0 specification when using updated configuration as described in the BC6145 QFN software release note, see www.csrsupport.com
- Internal ROM
- 48KB of internal RAM, enables full-speed data transfer, mixed voice/data and full piconet support
- Logic for FEC, HEC, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, μ-law and linear voice from host and A-law, μ-law and CVSD voice over air
- Configurable mono headset ROM software to set-up headset features and user interface
- HFP v1.5 and HSP v1.2
- Secure simple pairing
- CSR's proximity pairing (headset-initiated pairing)
- Supports mSBC wideband speech decoder
- Advanced multipoint support, enables a headset to connect to 2 mobile phones or 1 mobile phone and a VoIP dongle
- DSP-based 6th generation 1-mic CVC echo and noise cancellation for effective noise cancellation under all conditions
- Bidirectional noise reduction ensures increased speech clarity in preparation for improving intelligibility through spectral enhancement for the user and the person they are speaking to

Kalimba DSP

- Very low-power Kalimba DSP coprocessor, 64MIPS, 24-bit fixed point core
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- Separate program memory and dual data memory
- Program memory cache when executing from ROM

Audio Codec

- 16-bit resolution mono codec
- Integrated amplifiers for driving a 16Ω speaker; no need for external components
- Support for single-ended speaker termination and line output
- Integrated low-noise microphone bias
- Digital enhancements to add bass cut and side tone
- Analogue enhancements to support single-ended speaker drive capability and reference availability

Physical Interfaces

- Synchronous serial interface for system debugging
- I²C compatible interface communicates with an external EEPROM which contains all of the device configuration (PS Keys)
- Synchronous serial interface communicates with an external SPI flash device, which can store programmable audio prompts
- UART interface with data rates up to 3Mbits/s

Auxiliary Features

- BIST minimises production test time
- Crystal oscillator with built-in digital trimming
- Device can run in low power modes from an external 32.768kHz clock signal
- Programmable audio prompts
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Integrated regulators: 1.5V output from 1.7V to 2.8V input and 1.9V output from 2.7V to 5.5V input
- Integrated high-efficiency switch-mode regulator; 1.5V output from 2.2V to 4.4V input
- Power-on-reset cell detects low supply voltage
- Arbitrary sequencing of power supplies permitted
- 10-bit ADC
- Battery charger with programmable current, 20mA to 150mA for lithium ion/polymer battery. Supports external boost charge for up to a total of 240mA fast charge current.
- 2 LED drivers with faders

Package Option

- 48-lead 7 x 7 x 0.9mm, 0.5mm pitch QFN

Functional Block Diagram

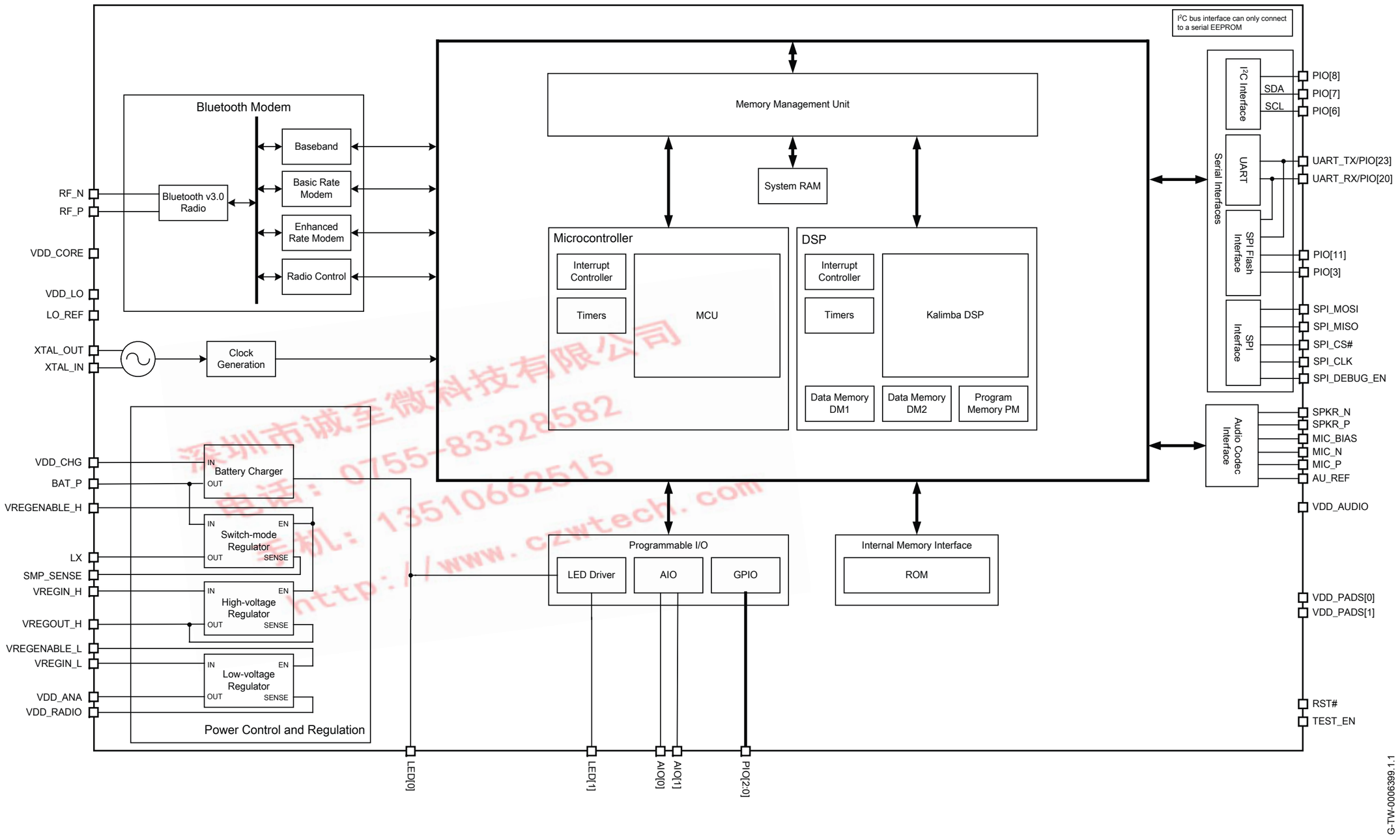


Figure : Functional Block Diagram

Document History

Revision	Date	Change Reason
1	04 AUG 10	Original publication of this document.
2	16 NOV 10	Production information added. Ordering information and ROM code updated. ESD information and power consumption updated. Clarification of boost charge current definition and update to example application schematic. Added input decoupling capacitor requirement to high-voltage linear regulator. Minor editorial changes. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Life Support Policy and Use in Safety-critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

CSR Green Semiconductor Products and RoHS Compliance

BC6145 QFN devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

BC6145 QFN devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

Trademarks, Patents and Licences

Unless otherwise stated, words and logos marked with ™ or ® are trademarks registered or owned by CSR plc or its affiliates. Bluetooth ® and the Bluetooth ® logos are trademarks owned by Bluetooth ® SIG, Inc. and licensed to CSR. Other products, services and names used in this document may have been trademarked by their respective owners.

The publication of this information does not imply that any license is granted under any patent or other rights owned by CSR plc and/or its affiliates.

CSR reserves the right to make technical changes to its products as part of its development programme.

While every care has been taken to ensure the accuracy of the contents of this document, CSR cannot accept responsibility for any errors.

Refer to www.csrsupport.com for compliance and conformance to standards information.

No statements or representations in this document are to be construed as advertising, marketing, or offering for sale in the United States imported covered products subject to the Cease and Desist Order issued by the U.S. International Trade Commission in its Investigation No. 337-TA-602. Such products include SiRFstarIII™ chips that operate with SiRF software that supports SiRFInstantFix™, and/or SiRFLoc® servers, or contains SyncFreeNav functionality.

Contents

List of Figures

List of Tables

List of Equations

1 Package Information

1.1 Pinout Diagram

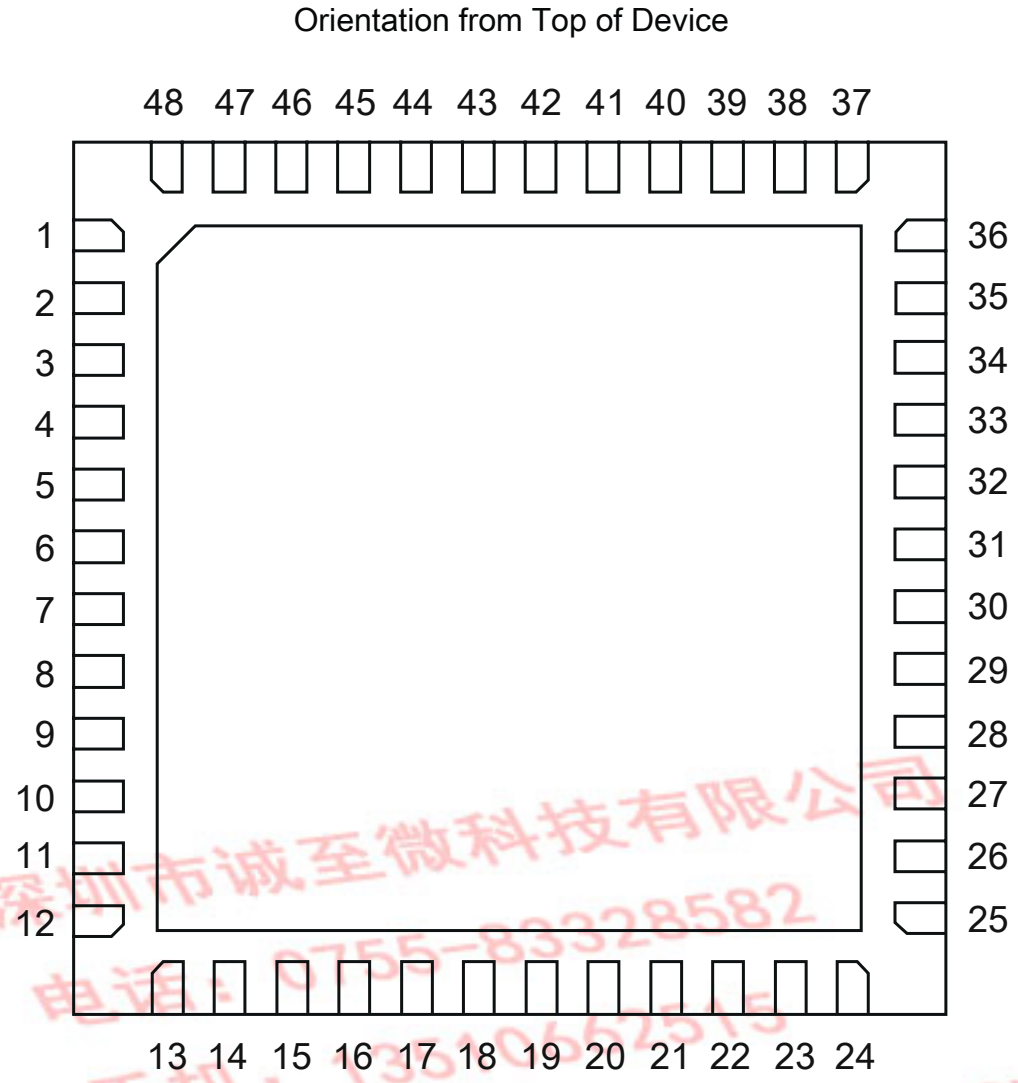


Figure 1.1: Device Pinout

1.2 Device Terminal Functions

Bluetooth Radio	Lead	Pad Type	Supply Domain	Description
RF_N	8	RF	VDD_RADIO	Transmitter output/switched receiver
RF_P	7	RF	VDD_RADIO	Complement of RF_N

Synthesiser and Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	13	Analogue	VDD_ANA	For crystal or external clock input
XTAL_OUT	14	Analogue	VDD_ANA	Drive for crystal
LO_REF	15	Analogue	VDD_ANA	Reference voltage to decouple the synthesiser

SPI Interface	Lead	Pad Type	Supply Domain	Description
SPI_MOSI	38	Input, with weak internal pull-down	VDD_PADS[1]	SPI data input
SPI_CS#	40	Bidirectional with weak internal pull-down	VDD_PADS[1]	Chip select for SPI, active low
SPI_CLK	39	Bidirectional with weak internal pull-down	VDD_PADS[1]	SPI clock
SPI_MISO	41	Bidirectional with weak internal pull-down	VDD_PADS[1]	SPI data output
SPI_DEBUG_EN	42	Input with strong internal pull-down	VDD_PADS[1]	Debug interface input, not required for production / debug SPI access on BC6145 QFN

UART Interface	Lead	Pad Type	Supply Domain	Description
UART_TX / PIO[23]	19	Bidirectional with weak internal pull-up	VDD_PADS[0]	UART data output, active high. PIO[23] is data output for SPI flash interface (BC6145 QFN is master).
UART_RX / PIO[20]	18	Bidirectional with weak internal pull-down	VDD_PADS[0]	UART data input, active high. PIO[20] is clock for SPI flash interface (BC6145 QFN is master).

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[11]	27	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[0]	Programmable input/output line. PIO[11] is data input for SPI flash interface (BC6145 QFN is master).
PIO[8]	44	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[1]	Programmable input/output line
PIO[7]	45			
PIO[6]	46			
PIO[3]	21	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[0]	Programmable input/output line PIO[3] is chip select for SPI flash interface (BC6145 QFN is master).
PIO[2]	22	Bidirectional with programmable strength internal pull-up/down	VDD_PADS[0]	Programmable input/output line
PIO[1]	23			
PIO[0]	24			
AIO[0]	17	Bidirectional	VDD_ANA	Programmable input/output line
AIO[1]	16			

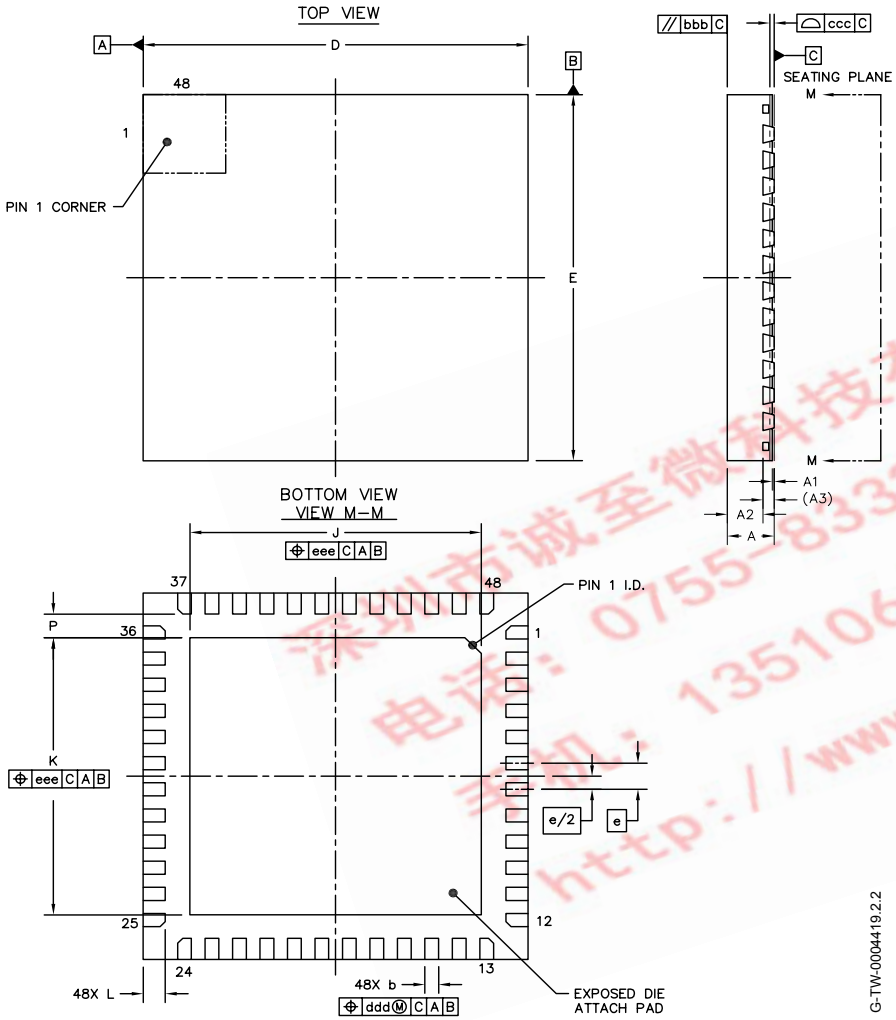
Audio	Lead	Pad Type	Supply Domain	Description
SPKR_N	3	Analogue	VDD_AUDIO	Speaker output, negative
SPKR_P	4	Analogue	VDD_AUDIO	Speaker output, positive
MIC_N	2	Analogue	VDD_AUDIO	Microphone input, negative
MIC_P	1	Analogue	VDD_AUDIO	Microphone input, positive
MIC_BIAS	47	Analogue	VDD_AUDIO, BAT_P	Microphone bias
AU_REF	5	Analogue	VDD_AUDIO	Decoupling of audio reference (for high quality audio)

LED Drivers	Lead	Pad Type	Supply Domain	Description
LED[1]	28	Open drain output	Open drain	LED driver
LED[0]	29	Open drain output	Open drain	LED driver

Test and Debug	Lead	Pad Type	Supply Domain	Description
RST#	26	Input with weak internal pull-up	VDD_PADS[0]	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	25	Input with strong internal pull-down	VDD_PADS[0]	For test purposes only (leave unconnected)

Power Supplies Control	Lead	Description
VREGENABLE_L	10	Take high to enable low-voltage regulator
VREGENABLE_H	33	Take high to enable both high-voltage regulator and switch-mode regulator
VREGIN_L	11	Input to internal low-voltage regulator
VREGIN_H	32	Input to internal high-voltage regulator
LX	35	Switch-mode power regulator output
VREGOUT_H	31	High-voltage regulator output
VDD_PADS[1]	43	Positive supply for digital input/output ports including PIO[8:6] and SPI interface
VDD_PADS[0]	20	Positive supply for digital input/output ports including PIO[11,3:0]
VDD_CORE	30	Positive supply for internal digital circuitry
VDD_RADIO	6	Positive supply for RF circuitry
VDD_ANA	12	Positive supply for analogue circuitry, AIO[1:0]. Output from internal 1.5V regulator
VDD_LO	9	Positive supply for local oscillator circuitry
VDD_AUDIO	48	Positive supply for audio
BAT_P	36	Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator
VDD_CHG	37	Lithium ion/polymer battery charger input
SMP_SENSE	34	Positive supply for switch-mode control circuitry
VSS	Exposed Pad	Ground connections

1.3 Package Dimensions



Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.8	0.85	0.9	J	5.2	5.3	5.4
A1	0	0.035	0.05	K	5.2	5.3	5.4
A2	-	0.65	0.67	L	0.35	0.4	0.45
A3	-	0.203	-	bbb	-	0.1	-
b	0.2	0.25	0.3	ccc	-	0.08	-
D	6.9	7	7.05	ddd	-	0.1	-
E	6.9	7	7.05	eee	-	0.1	-
e	-	0.5	-	P	0.3	-	-

Notes

1. Coplanarity applies to leads, corner leads and die attach pad.
2. Exposed die attach pad smaller than BlueVox2 QFN. Dimensions have been reduced to enhance solderability. Backward pin-for-pin compatibility with BlueVox2 QFN is maintained

Description	48-lead Quad Flat No-lead Package		
Size	7 x 7 x 0.9mm	**JEDEC**	MO-220
Pitch	0.5	**Units**	mm

1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 7 x 7 x 0.9mm QFN 48-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern to be in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

2 Bluetooth Modem

2.1 RF Ports

2.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

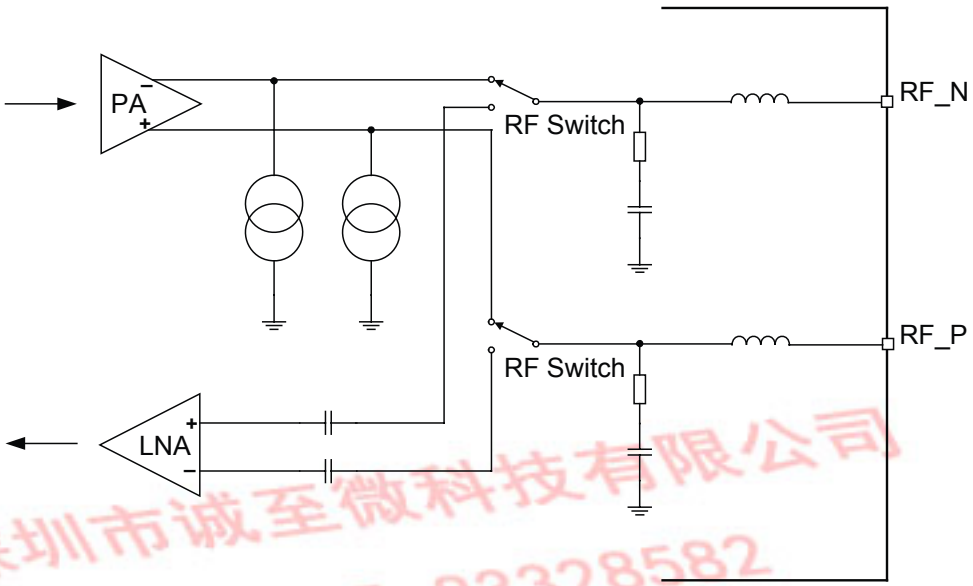


Figure 2.1: Simplified Circuit RF_N and RF_P

RF_N and RF_P require an external DC bias. The DC level must be set at VDD_RADIO.

2.2 RF Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die.

A digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise enables BC6145 QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA on the BC6145 QFN has a maximum output power that enables it to operate as a Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v3.0 specification.

2.5 Baseband

2.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

2.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of the Bluetooth v3.0 specification including AFH and eSCO.

3 Clock Generation

BC6145 QFN requires a Bluetooth reference clock frequency, derived from an externally connected crystal in the range 16MHz to 26MHz.

All BC6145 QFN internal digital clocks are generated by a phase locked loop, locked to the frequency of the external reference clock.

The Bluetooth operation determines the watchdog clock operation in low-power modes.

3.1 Clock Architecture

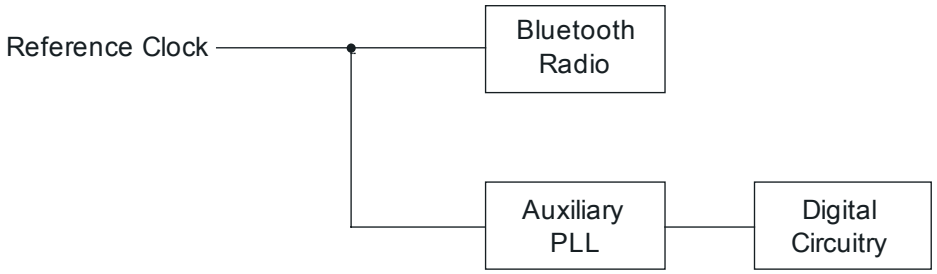


Figure 3.1: Clock Architecture

3.2 Input Frequencies and PS Key Settings

BC6145 QFN is configured to operate with a chosen reference frequency. PSKEY_ANA_FREQ sets this reference frequency for all frequencies using an integer multiple of 250kHz. The input frequency default setting for BC6145 QFN is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

3.3 Crystal Oscillator: XTAL_IN and XTAL_OUT

BC6145 QFN contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 3.2 shows the external crystal is connected to pins XTAL_IN, XTAL_OUT.

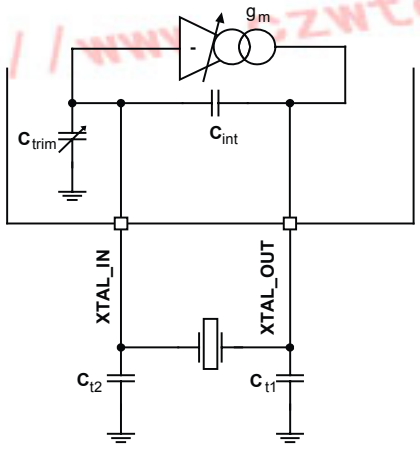
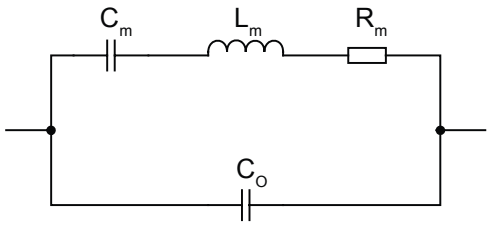


Figure 3.2: Crystal Driver Circuit

Figure 3.3 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.



G-TW-0000245.4.4

Figure 3.3: Crystal Equivalent Circuit

The resonant frequency can be trimmed with the crystal load capacitance. BC6145 QFN contains variable internal capacitors to provide a fine trim.

Table 3.1 shows the specification for an external crystal.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	26	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF

Table 3.1: Crystal Specification

The BC6145 QFN driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and can be set for optimum performance.

3.3.1 Crystal PS Key Settings

The BC6145 QFN firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. The firmware uses PSKEY_XTAL_TARGET_AMPLITUDE to servo the required amplitude of crystal oscillation. For more information see the software build release note.

Configure the BC6145 QFN to operate with the chosen reference frequency.

3.4 External 32kHz Clock

Apply a 32kHz clock to AIO[0] by setting DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE.

If the external clock is applied to the analogue pad AIO[0], drive the digital signal with a maximum 1.5V.

Note:

If the 32kHz clock is accurate and stable to within 200ppm, then further power saving features are available. See the relevant software release note for more information.

4 Bluetooth Stack Microcontroller

BC6145 QFN uses a 16-bit RISC MCU for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

4.1 Programmable I/O Ports

BC6145 QFN provides 8 lines of programmable bidirectional I/O.

Note:

PIO[11,3:0] are powered from VDD_PADS[0] and PIO[8:6] are powered from VDD_PADS[1]. AIO[1:0] are powered from VDD_ANA.

Any of the PIO lines are configurable as button inputs or control outputs. Certain PIOs also have dedicated functions that are accessed using appropriate PS Keys. PSKEY_CLOCK_REQUEST_ENABLE configures PIO[6] or PIO[2] as a request line for an external clock source. This is useful for detecting when BC6145 QFN is entering or leaving deep sleep.

Note:

See the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BC6145 QFN has 2 general-purpose analogue interface pins, AIO[1:0], to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC. Signals selectable on this interface include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (output from AIO[0] only) and the XTAL and XTAL/2 clock frequency (output from AIO[1] and AIO[0]). When operating with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, VDD_ANA determines the output voltage level.

5 Kalimba DSP

The Kalimba DSP is an open platform DSP enabling signal processing functions to be performed on over-air data or codec data to enhance audio applications. The Kalimba DSP is dedicated to processing the audio enhancement algorithms, which are hard-coded into the ROM. Figure 5.1 shows the Kalimba DSP interfaces to other functional blocks within BC6145 QFN.

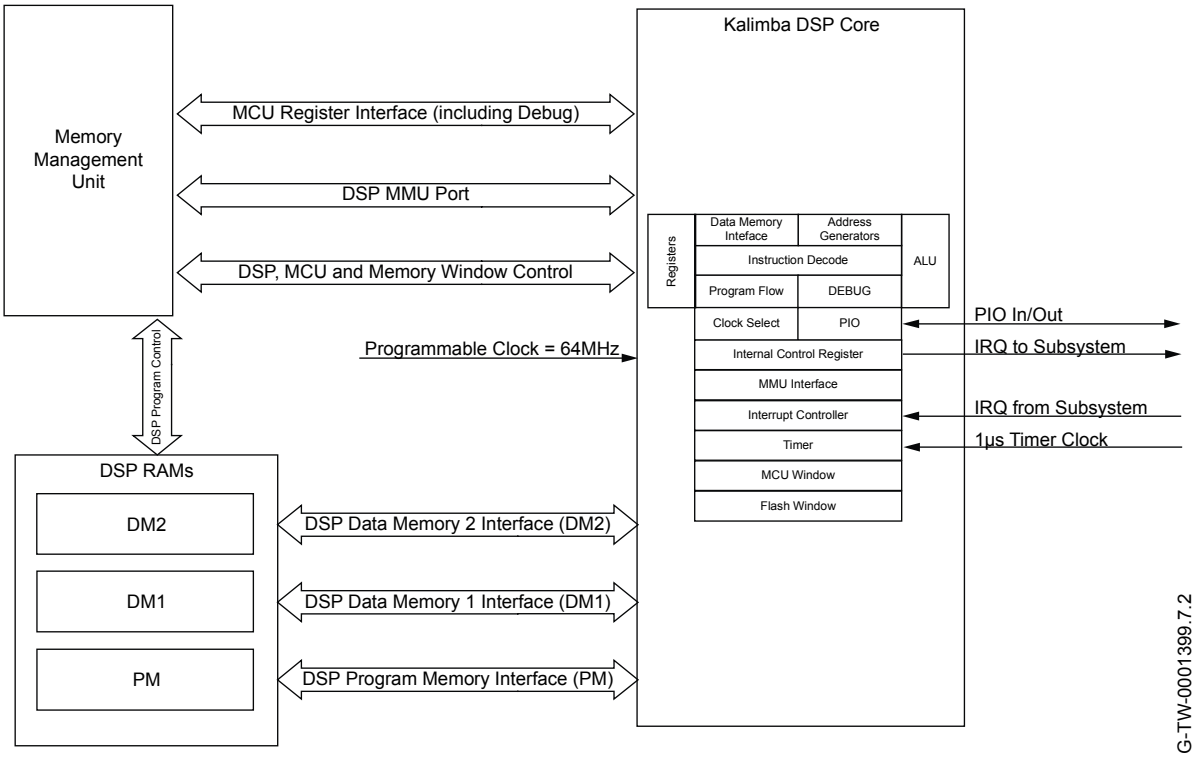


Figure 5.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 64MIPS performance, 24-bit fixed point DSP core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, enabling an ALU operation and up to 2 memory accesses in a single cycle
- Zero overhead looping
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

6 Memory Interface and Management

6.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

6.2 System RAM

48KB of integrated RAM supports the RISC MCU and is shared between the ring buffers for holding voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

6.3 Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 8K x 24-bit for data memory 1 (DM1)
- 4K x 24-bit for data memory 2 (DM2)
- 4K x 32-bit for program memory (PM)

Note:

The Kalimba DSP can also execute directly from internal ROM, using a 64-instruction on-chip cache.

6.4 Internal ROM

Internal ROM is provided for system firmware implementation.

7 Serial Interfaces

7.1 UART Interface

BC6145 QFN has a standard UART serial interface that provides a simple communications channel for test and debug using RS232 protocol.

2 signals implement the UART function, UART_TX and UART_RX. When BC6145 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.

UART configuration parameters, such as baud rate and packet format, are set using BC6145 QFN firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 7.1: Possible UART Settings

The UART interface resets BC6145 QFN on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 7.1 shows. If t_{BRK} is longer than the value, defined by the HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature enables a host to initialise the system to a known state. Also, BC6145 QFN can issue a break character for waking the host.

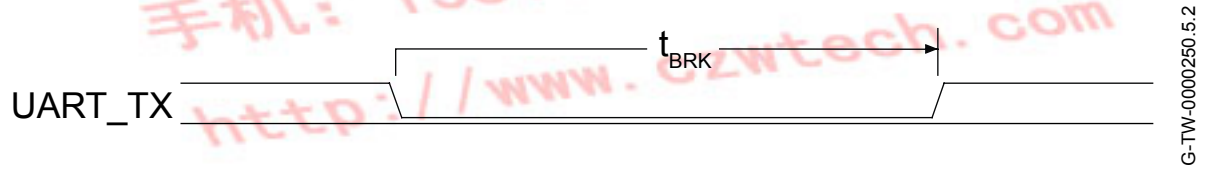


Figure 7.1: Break Signal

Table 7.2 shows a list of common baud rates and their associated values for PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range is set in the PS Key according to the formula in Equation 7.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 7.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 7.2: Standard Baud Rates

7.1.1 UART Configuration While Reset is Active

The UART interface is tristate while BC6145 QFN is being held in reset. This enables the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BC6145 QFN reset is de-asserted and the firmware begins to run.

7.2 Programming and Debug Interface

Important Note:

The SPI is for programming, configuring (PS Keys) and debugging the BC6145 QFN. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

BC6145 QFN uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

7.2.1 Instruction Cycle

The BC6145 QFN is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 7.3 shows the instruction cycle for a SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 7.3: Instruction Cycle for a SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BC6145 QFN on the rising edge of the clock line SPI_CLK. When reading, BC6145 QFN replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. Taking SPI_CS# high terminates the transaction.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when transferring large amounts of data. To overcome this BC6145 QFN offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

7.2.2 Multi-slave Operation

Avoid connecting BC6145 QFN in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BC6145 QFN is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BC6145 QFN outputs 0 if the processor is running or 1 if it is stopped.

7.3 I²C Interface

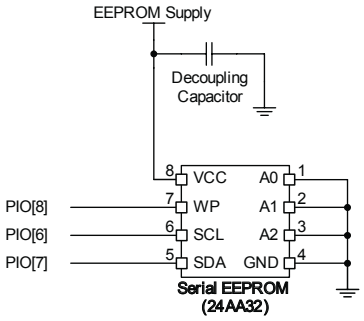
PIO[8:6] are available to form a master I²C interface. The interface is formed using software to drive these lines.

Note:

The program memory for the BC6145 QFN is internal ROM so the I²C interface only connects to a serial EEPROM, Figure 7.2 shows an example. The EEPROM stores programmable audio prompts, see Section 14.1.5, as well as PS Keys and configuration information. The programmable audio prompts option requires a larger EEPROM than Figure 7.2 shows, up to 512Kb.

When a SPI flash is used to store programmable audio prompts, see Section 7.4, an EEPROM is still required to store the PS Keys and configuration information.

The EEPROM Supply in Figure 7.2 is 1.9V.



G-TW-0000207.5.3

Figure 7.2: Example EEPROM Connection

7.4 SPI Flash Interface

PIO[23, 20, 11, 3] form a software-driven master SPI flash interface, Figure 7.3 shows an example connection to a serial SPI flash IC.

The SPI flash is only for programmable audio prompts storage, see Section 14.1.5.

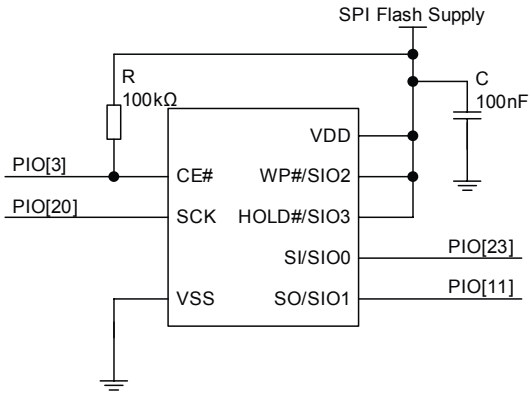


Figure 7.3: Example SPI Flash Interface

Note:

The SPI Flash Supply in Figure 7.3 is 1.9V.

For more information on supported SPI flash ICs contact CSR.

8 Audio Interface

The audio interface circuit consists of:

- Mono audio codec
- Audio inputs and outputs

8.1 Audio Input and Output

The audio input circuitry consists of:

- 1 channel of microphone input:
  - The microphone input is configurable to be either single-ended or fully differential
  - The input has an analogue and digital programmable gain stage for optimisation of different microphones

The audio output circuitry consists of a single differential class AB output stage.

8.2 Mono Audio Codec Block Diagram

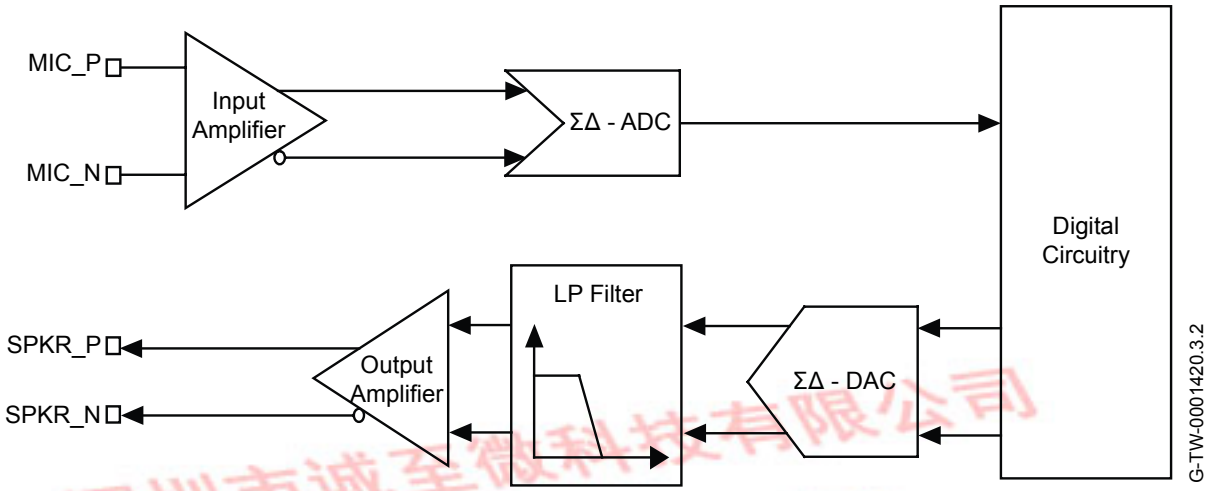


Figure 8.1: Mono Codec Audio Input and Output Stages

The mono audio codec uses a fully differential architecture in the analogue signal path, which results in low noise-sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components.

8.3 ADC

The ADC consists of:

- A second-order Sigma-Delta converter, as Figure 8.1 shows.
- 2 gain stages; one of which is an analogue gain stage and the other is a digital gain stage.

8.3.1 ADC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarised in Table 8.1. There is also a high resolution digital gain mode, which enables gain changes in 1/32 steps. Contact CSR for more information.

Gain Selection Value	ADC Digital Gain Setting (dB)	Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 8.1: ADC Digital Gain Rate Selection

8.3.2 ADC Analogue Gain

Figure 8.2 shows the equivalent block diagram for the ADC analogue amplifier. It is a two-stage amplifier:

- The first stage amplifier has a selectable gain of either bypass for line input mode or gain of 24dB gain for the microphone mode.
- The second stage has a programmable gain with 7 individual 3dB steps. By combining the 24dB gain selection of the microphone input with the 7 individual 3dB gain steps, the overall range of the analogue amplifier is approximately -3dB to 42dB in 3dB steps. The BC6145 QFN controls all the gain control of the ADC.

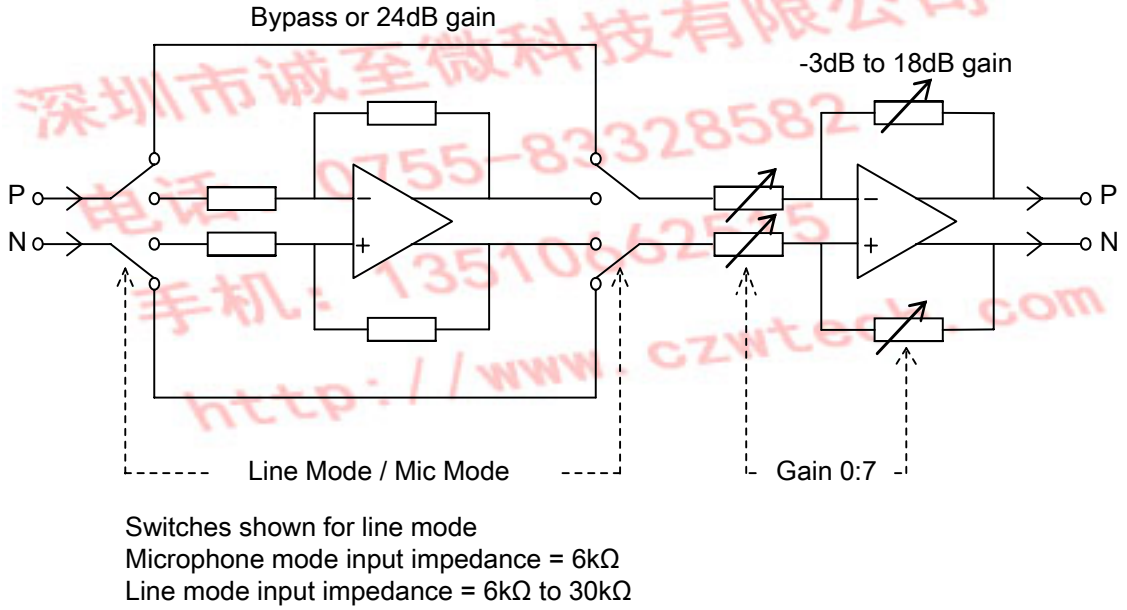


Figure 8.2: ADC Analogue Amplifier Block Diagram

8.4 DAC

The DAC consists of:

- A second-order Sigma-Delta converter, as Figure 8.1 shows.
- 2 gain stages; one of which is an analogue gain stage and the other is a digital gain stage.

8.4.1 DAC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings, summarised in Table 8.2. There is also a high resolution digital gain mode, which enables gain changes in 1/32 steps. Contact CSR for more information.

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 8.2: DAC Digital Gain Rate Selection

8.4.2 DAC Analogue Gain

Table 8.3 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	3	3	-9
6	0	2	-12
5	-3	1	-15
4	-6	0	-18

Table 8.3: DAC Analogue Gain Rate Selection

8.5 Microphone Input

Figure 8.3 shows recommended biasing for each microphone. The microphone bias, MIC_BIAS, derives its power from the BAT_P and requires a 1µF capacitor on its output.

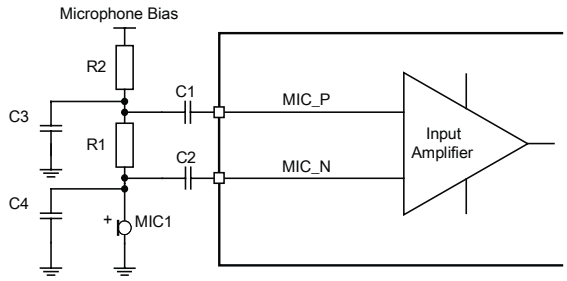


Figure 8.3: Microphone Biasing

The MIC_BIAS is like any voltage regulator and requires a minimum load to maintain regulation. The MIC_BIAS maintains regulation within the limits 0.200mA to 1.230mA. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.

The audio input range is from 1µA to 10µA at 94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV.

The input impedance at MIC_N and MIC_P is typically 6.0kΩ.

C1 and C2 are 150nF if low frequency roll-off is required to limit wind noise on the microphone.

R1 sets the microphone load impedance and is normally in the range of 1kΩ to 2kΩ.

R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Select the values as required. R2 can connect to a convenient supply, in which case the bias network is permanently enabled, or to the MIC_BIAS output (which is ground referenced and provides good rejection of the supply), which is configurable to provide bias only when the microphone is required.

Table 8.4 shows the 4-bit programmable output voltage that the microphone bias provides, and Table 8.5 shows the 4-bit programmable output current.

The characteristics of the microphone bias include:

- Power supply:
  - BC6145 QFN microphone supply is BAT_P
  - Minimum input voltage = Output voltage + drop-out voltage
  - Maximum input voltage is 4.4V
  - Typically the microphone bias is between 2V and 2.5V, or as specified by the microphone vendor
- Drop-out voltage:
  - 300mV minimum
  - Guaranteed for configuration of voltage or current output shown in Table 8.4 and Table 8.5
- Output voltage:
  - 4-bit programmable from 1.7V to 3.6V
  - Tolerance 90% to 110%
- Output current:
  - 4-bit programmable from 200µA to 1.230mA
  - Maximum current guaranteed >1mA
- Load capacitance:
  - Unconditionally stable for 1µF ± 20% and 2.2µF ± 20% pure C

Output Step	VOL_SET[3:0]	Typ	Units	Output Step	VOL_SET[3:0]	Typ	Units
0	0000	1.71	V	8	1000	2.32	V
1	0001	1.76	V	9	1001	2.43	V
2	0010	1.82	V	10	1010	2.56	V
3	0011	1.87	V	11	1011	2.69	V
4	0100	1.95	V	12	1100	2.90	V
5	0101	2.02	V	13	1101	3.08	V
6	0110	2.10	V	14	1110	3.33	V
7	0111	2.18	V	15	1111	3.57	V

Table 8.4: Voltage Output Steps

Output Step	CUR_SET[3:0]	Typ	Units	Output Step	CUR_SET[3:0]	Typ	Units
0	0000	0.200	mA	8	1000	0.750	mA
1	0001	0.280	mA	9	1001	0.810	mA
2	0010	0.340	mA	10	1010	0.860	mA
3	0011	0.420	mA	11	1011	0.950	mA
4	0100	0.480	mA	12	1100	1.000	mA
5	0101	0.530	mA	13	1101	1.090	mA
6	0110	0.610	mA	14	1110	1.140	mA
7	0111	0.670	mA	15	1111	1.230	mA

Table 8.5: Current Output Steps

Note:

For BAT_P, the PSRR at 100Hz to 22kHz, with >300mV supply headroom, decoupling capacitor of 1.1µF, is typically 58.9dB and worst case 53.4dB.

For VDD_AUDIO, the PSRR at 100Hz to 22kHz, decoupling capacitor of 1.1µF, is typically 88dB and worst case 60dB.

8.6 Line Input

If the input analogue gain is set to less than 24dB, BC6145 QFN automatically selects line input mode. In line input mode the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode the input impedance varies from 6kΩ to 30kΩ, depending on the volume setting. Figure 8.4 and Figure 8.5 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

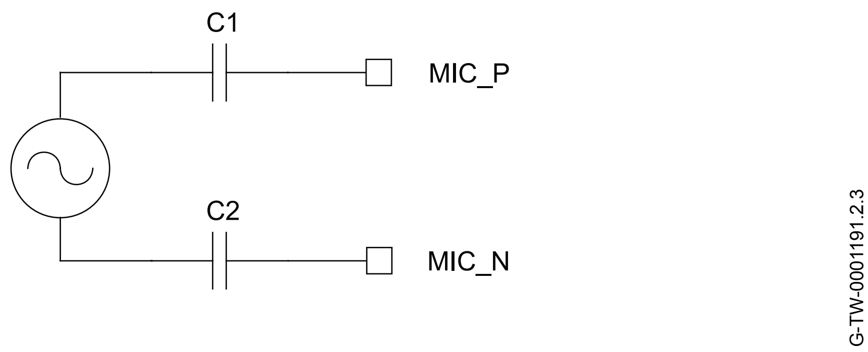


Figure 8.4: Differential Input

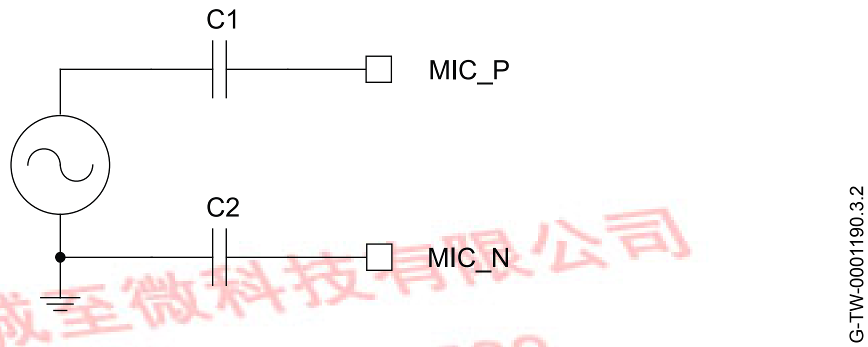


Figure 8.5: Single-ended Input

8.7 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The output stage circuit comprises a DAC with gain setting and class AB output stage amplifier. The output is available as a differential signal between SPKR_N and SPKR_P, as Figure 8.6 shows.

The output stage is capable of driving a speaker directly when its impedance is at least 8Ω.

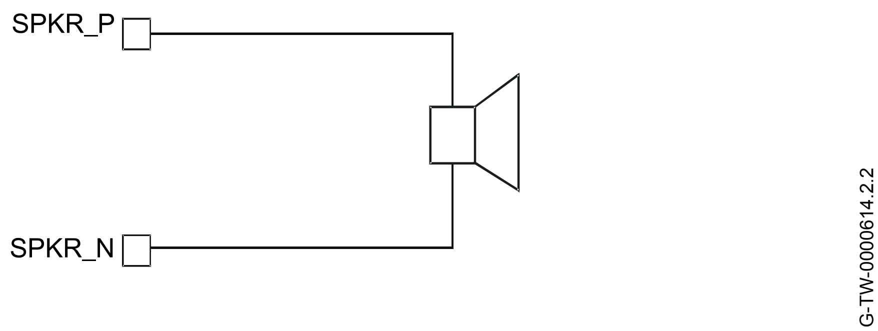


Figure 8.6: Speaker Output

A 3-bit programmable resistive divider controls the analogue gain of the output stage, which sets the gain in steps of approximately 3dB.

8.8 Integrated Digital IIR Filter

BC6145 QFN has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2-stage, second order IIR and is for functions such as custom wind noise reduction. The filter also has optional DC blocking.

The filter has 10 configuration words:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format `NN.NNNNNNNNNN`.

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

```
01.1111111111 = most positive number, close to 2
01.0000000000 = 1
00.0000000000 = 0
11.0000000000 = -1
10.0000000000 = -2, most negative number
```

Equation 8.1 shows the equation for the IIR filter. Equation 8.2 shows the equation for when the DC blocking is enabled.

The filter is configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps. This requires firmware support. The configuration function takes 10 variables in the following order:

```
0 : Gain
1 : b01
2 : b02
3 : a01
4 : a02
5 : b11
6 : b12
7 : a11
8 : a12
9 : DC Block (1 = enable, 0 = disable)
```

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01} z^{-1} + b_{02} z^{-2})}{(1 + a_{01} z^{-1} + a_{02} z^{-2})} \times \frac{(1 + b_{11} z^{-1} + b_{12} z^{-2})}{(1 + a_{11} z^{-1} + a_{12} z^{-2})}$$

Equation 8.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 8.2: IIR Filter plus DC Blocking Transfer Function, $H_{DC}(z)$

8.8.1 Integrated Digital Filter Configuration

The behaviour of the integrated digital IIR filter described in Section 8.8, is configurable through 12 values stored in PSKEY_USR29:

- 10-words for the IIR filter parameters in Section 8.8
- 1-word for the audio energy estimation threshold
- 1-word for the gain applied when the audio energy estimation is above the threshold

Adjusting these values configures the IIR filter for different functions.

Note:

The IIR filter is switched off at initialisation.

8.9 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BC6145 QFN codec contains side tone circuitry to do this. The side tone hardware is configured through the following PS Keys:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

9 Power Control and Regulation

BC6145 QFN contains 3 regulators:

- A switch-mode regulator, which generates a 1.5V rail
- A low-voltage regulator, which generates an optional 1.5V rail
- A high-voltage linear regulator, which generates a 1.9V rail for powering the EEPROM

Various configurations for power control and regulation with BC6145 QFN are available, but Figure 9.1 shows a typical configuration. This configuration shows the switch-mode regulator generating a 1.5V supply rail, and the high-voltage linear regulator generating a 1.9V supply rail.

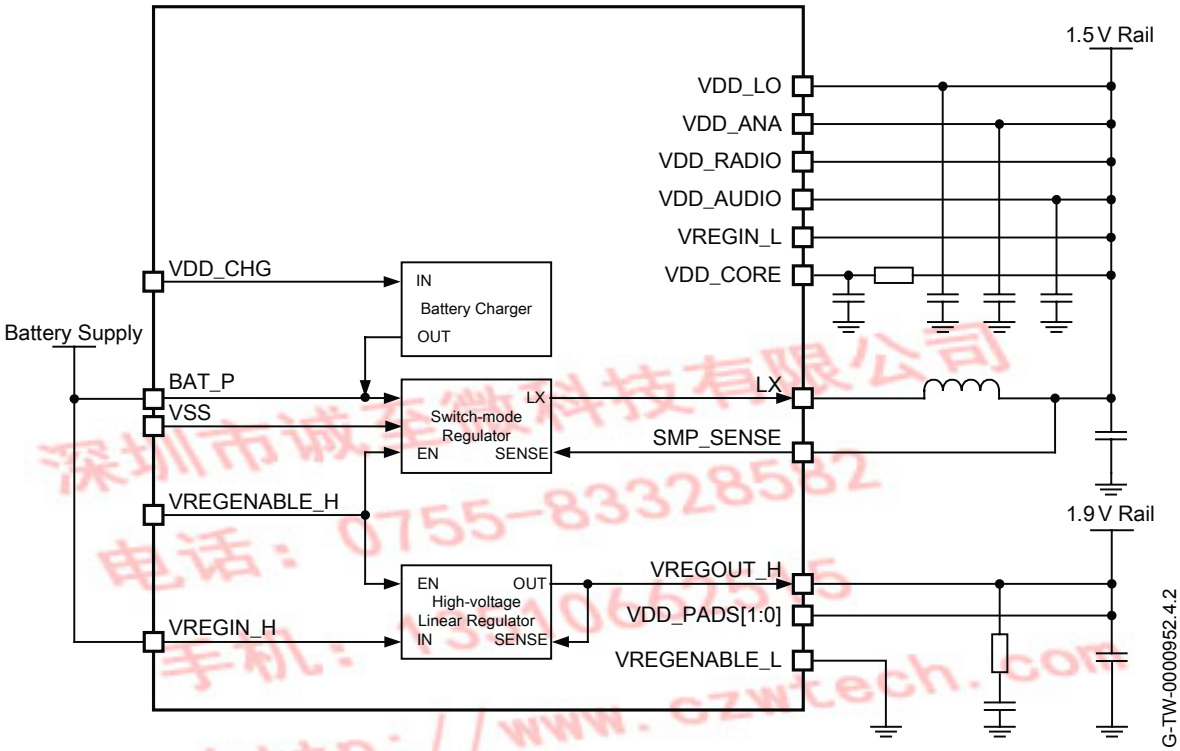


Figure 9.1: Voltage Regulator Configuration

9.1 Power Sequencing

The 1.5V supply rails are VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO. CSR recommends that these supply rails are all powered at the same time.

The digital I/O supply rails are VDD_PADS[1:0].

The sequence of powering the 1.5V supply rails relative to the digital I/O supply rails is not important. If the digital I/O supply rails are powered before the 1.5V supply rails, all digital I/Os have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_AUDIO, VDD_LO and VDD_RADIO can connect directly to a 1.5V supply.

A simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The digital I/O supply rails are connected either together or independently to an appropriate voltage rail. CSR recommends decoupling of the digital I/O supply rails.

9.2 External Voltage Source

If supplying any of the power rails for BC6145 QFN from an external voltage source, rather than one of the internal voltage regulators, CSR recommends that VDD_AUDIO, VDD_LO and VDD_RADIO have less than 10mV rms noise level between 0 and 10MHz. Also avoid single tone frequencies.

The transient response of any external regulator should match or better the internal regulator available on BC6145 QFN. For more information, see the regulator characteristics in Section 11. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

9.3 Switch-mode Regulator

CSR recommends the on-chip switch-mode regulator to power the 1.5V supply rail.

An external LC filter circuit of a low-resistance series inductor, L1 (22µH), followed by a low ESR shunt capacitor, C1 (4.7µF), is required between the LX terminal and the 1.5V supply rail. A connection between the 1.5V supply rail and the SMP_SENSE pin is required.

A 2.2µF decoupling capacitor is required between BAT_P and VSS.

To maintain high-efficiency power conversion and low supply ripple, it is essential that the series resistance of tracks between the BAT_P and VSS terminals, the filter and decoupling components, and the external voltage source are minimised.

The switch-mode regulator is enabled by any of the following:

- VREGENABLE_H pin
- BC6145 QFN device firmware
- BC6145 QFN battery charger

The switch-mode regulator switches into a low-power pulse skipping mode when the device is sent into deep sleep mode, or in reset.

When the switch-mode regulator is not required, either ground the terminals BAT_P and LX, or leave them unconnected.

9.4 High-voltage Linear Regulator

The 1.9V high-voltage linear regulator provides power for an external EEPROM. The external EEPROM stores PS Key and configuration information, see Section 7.3. CSR does not recommend using the high-voltage linear regulator to power any additional circuitry.

Connect a decoupling capacitor of at least 100nF (preferably 470nF) to the input of the high-voltage linear regulator to maintain stability.

Connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground, to the output of the high-voltage linear regulator, VREGOUT_H. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The high-voltage linear regulator is enabled by any of the following:

- VREGENABLE_H pin
- BC6145 QFN device firmware
- BC6145 QFN battery charger

The regulator is switched into a low-power mode when the device is in deep sleep mode, or in reset.

9.5 Low-voltage Linear Regulator

The low-voltage linear regulator is available to power a 1.5V supply rail. Its output is connected internally to VDD_ANA, and can connect externally to the other 1.5V power inputs.

Connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground to the output of the low-voltage linear regulator, VDD_ANA. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage linear regulator is enabled by any of the following:

- VREGENABLE_L pin
- BC6145 QFN device firmware
- BC6145 QFN battery charger

The low-voltage linear regulator switches into a low power mode when the device is in deep sleep mode, or in reset.

When the low-voltage linear regulator is not required, either leave the terminal VREGIN_L unconnected, or tie it to VDD_ANA.

9.6 Voltage Regulator Enable Pins

VREGENABLE_H and VREGENABLE_L enable the BC6145 QFN if the integrated regulators are used. Table 9.1 shows the appropriate enable pin responsible for each voltage regulator.

Enable Pin	Regulator
VREGENABLE_H	High-voltage Linear Regulator and Switch-mode Regulator
VREGENABLE_L	Low-voltage Linear Regulator

Table 9.1: BC6145 QFN Voltage Regulator Enable Pins

The voltage regulator enable pins are active high, with weak pull-downs.

BC6145 QFN boots-up when the voltage regulator enable pins are pulled high, enabling the appropriate regulators. The firmware then latches the regulators on, release of the voltage regulator enable pins is then permitted.

The status of the VREGENABLE_H pin is available to firmware through an internal connection. VREGENABLE_H also works as an input line.

9.7 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, BAT_P, with the switch-mode regulator. Although it operates in conjunction with either of the high-voltage regulators on the BC6145 QFN.

The constant current level is varied to enable charging of different capacity batteries.

The charger enters various states of operation as it charges a battery, as listed below. A full operational description is in *BlueCore5 Charger Description and Calibration Procedure Application Note*:

- Off: entered when charger is disconnected.
- Trickle charge: entered when battery is below 2.9V. The battery is charged at a nominal 4.5mA. This mode is for the safe charge of deeply discharged cells.
- Fast charge constant current: entered when battery is above 2.9V. The charger enters the main fast charge mode. This mode charges the battery at the selected constant current, I_{chgset}.
- Fast charge constant voltage: entered when battery has reached a selected voltage, V_{float}. The charger switches mode to maintain the cell voltage at the V_{float} voltage by adjusting the charge current.
- Standby: this is the state when the battery is fully charged and no charging takes place. The battery voltage is continuously monitored and if it drops by more than 150mV below the V_{float} voltage the charger will re-enter the fast charge constant current mode to keep the battery fully charged.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, the charger operates and an LED connected to the terminal LED[0] illuminates. By default, until the firmware is running, the LED pulses at a low duty cycle to minimise current consumption.

The battery charger circuitry auto-detects the presence of a power source, enabling the firmware to detect, via an internal status bit, when the charger is powered. Therefore, when the charger supply is not connected to VDD_CHG, leave the terminal open-circuit. When not connected, the VDD_CHG pin must float, so do not pull to a power rail. When the battery charger is not enabled this pin may float to a low undefined voltage. Any DC connection increases current consumption of the device. Connection to capacitive components such as diodes, FETs and ESD protection are permitted.

The battery charger is designed to operate with a permanently connected battery. If the application enables the charger input connection while the battery is disconnected, then the BAT_P pin voltage could become unstable and cause damage to the internal switch-mode regulator. Connecting a 470µF capacitor to BAT_P limits these oscillations and prevents damage.

The BC6145 QFN supports an external boost charge feature to provide up to 240mA fast charge current. For more information contact CSR.

Note:

Support for the external boost charge feature is available when using updated configuration as described in the BC6145 QFN software release note, see www.csrsupport.com.

9.8 LED Drivers

BC6145 QFN includes 2 pads dedicated to driving LED indicators. Firmware controls both terminals, while the battery charger can also set LED[0].

The terminals are open-drain outputs. Connect the LED from a positive supply rail to the pad in series with a current-limiting resistor.

CSR recommends that the 2 pads, LED[0] or LED[1] pins, operate with a pad voltage below 0.5V. In this case, the pad is like a resistor, R_{ON}. The resistance together with the external series resistor sets the current, I_{LED}, in the LED. The current also depends on the external voltage, VDD, as Figure 9.2 shows.

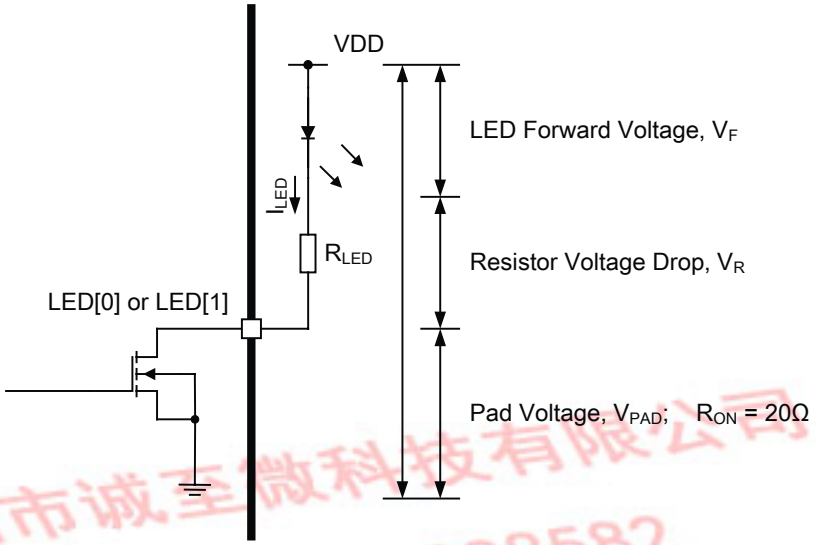


Figure 9.2: LED Equivalent Circuit

From Figure 9.2 it is possible to derive Equation 9.1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then calculate the value of R_{LED}.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 9.1: LED Current

For the LED[0] or LED[1] pad to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, V_R, keeps V_{PAD} below 0.5V. Equation 9.2 also applies.

$$VDD = V_F + V_R + V_{PAD}$$

Equation 9.2: LED PAD Voltage

Note:

The LED current adds to the overall current. Conservative LED selection extends battery life.

9.9 Reset, RST#

BC6145 QFN is reset from several sources:

- RST# pin
- Power-on reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5ms and 4.0ms following RST# being active. CSR recommends applying RST# for a period greater than 5ms.

The power-on reset occurs when the VDD_CORE supply falls below typically 1.25V and is released when VDD_CORE rises above typically 1.30V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate. Following a reset, BC6145 QFN assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BC6145 QFN is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BC6145 QFN free runs, again at a safe frequency.

9.9.1 Digital Pin States on Reset

Table 9.2 shows the pin states of BC6145 QFN on reset. PU and PD default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
UART_RX	Digital input with PD	PD	PD
UART_TX	Digital bidirectional with PU	PD	PD
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK	Digital bidirectional with PD	PD	PD
SPI_CS#	Digital bidirectional with PD	PD	PD
SPI_MISO	Digital tristate output with PD	PD	PD
SPI_DEBUG_EN	Digital input with PD	PD	PD
RST#	Digital input with PU	PU	PU
TEST_EN	Digital input with strong PD	PD	PD
PIO[11,3:0] PIO[8:6]	Digital bidirectional with PU/ PD	PD	PD

Table 9.2: Pin States on Reset

9.9.2 Status after Reset

The status of BC6145 QFN after a reset is:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available

10 Example Application Schematic

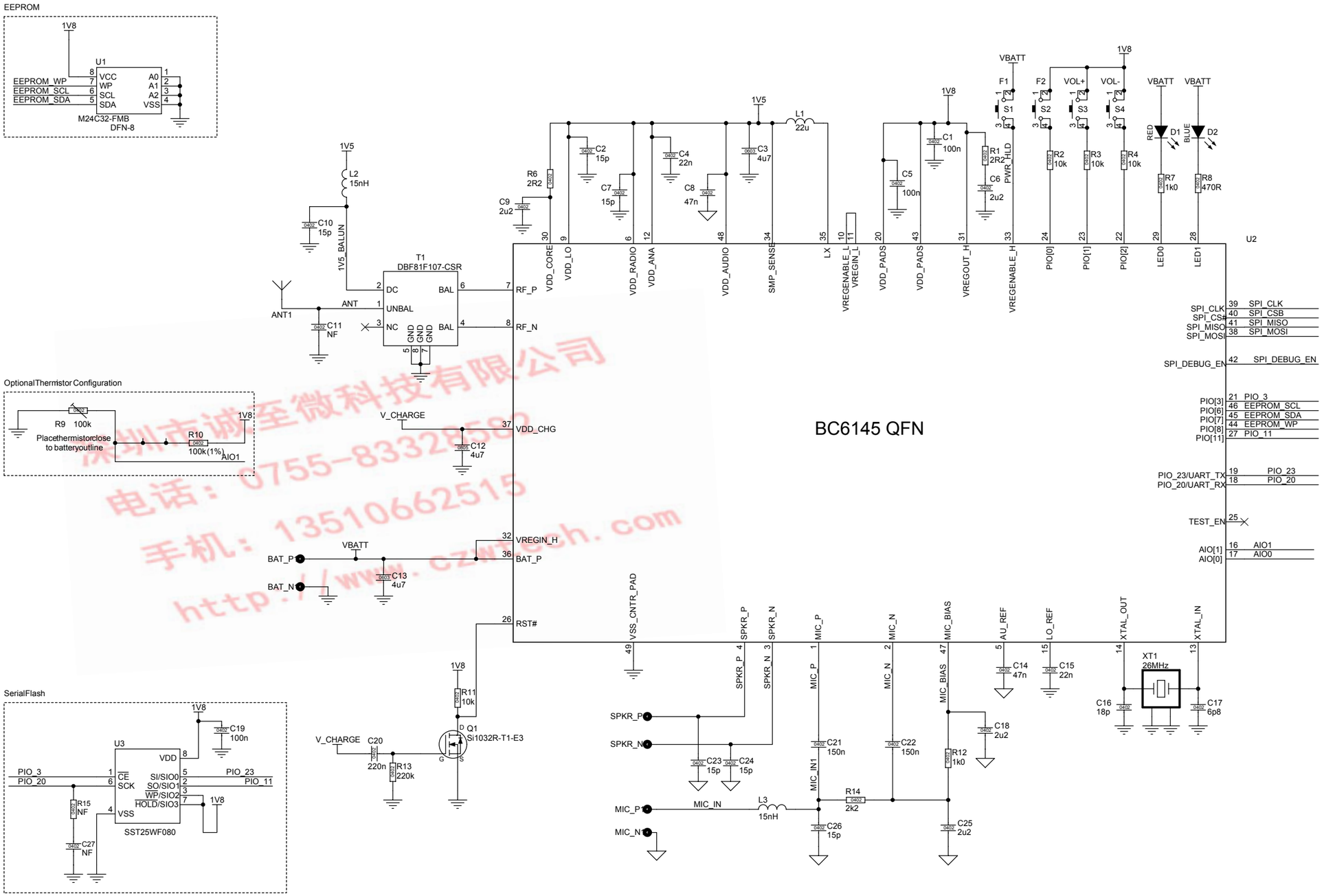


Figure 10.1: Example Application Schematic

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	105	°C
Core Supply Voltage	VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO	-0.4	1.65	V
I/O Voltage	VDD_PADS[1:0]	-0.4	3.6	V
Supply Voltage	VREGIN_L	-0.4	2.7	V
	VREGIN_H, VREGENABLE_H and VREGENABLE_L	-0.4	4.9	V
	BAT_P	-0.4	4.4	V
	LED[1:0]	-0.4	4.4	V
	VDD_CHG	-0.4	6.5	V
Other Terminal Voltages		VSS - 0.4	VDD + 0.4	V

11.2 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range[a]		-20	20	70	°C
Core Supply Voltage	VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO	1.42	1.50	1.57	V
I/O Supply Voltage	VDD_PADS[1:0]	1.7	3.3	3.6	V

[a] For radio performance over temperature refer to *BC6145 QFN Performance Specification*.

11.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO at 1.5V unless shown otherwise.
- VDD_PADS[1:0] at 3.3V unless shown otherwise.
- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

11.3.1 High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.7	-	4.9	V
Output voltage (I_{load} = 25mA / VREGIN_H = 3.0V)	1.80	1.90	2.05	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 25mA), ΔV_{out}	-	-	5	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	25	mA
Minimum load current	5	-	-	µA
Quiescent current (excluding load, I_{load} < 1mA)	30	50	60	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	11	15	21	µA

[a] The regulator output is connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 25mA pulsed load

[d] The regulator is in low-power mode when the IC is in deep sleep mode, or in reset

11.3.2 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.7	-	4.4	V
Output voltage (I_{load} = 70mA)	1.42	1.50	1.57	V
Temperature coefficient	-250	-	250	ppm/°C
Normal Operation				
Output ripple	-	-	10	mV rms
Transient settling time[a]	-	-	50	µs
Maximum load current	200	-	-	mA
Conversion efficiency (I_{load} = 70mA)	-	90	-	%
Switching frequency[b]	-	1.333	-	MHz
Start-up current limit[c]	30	50	80	mA
Low-power Mode [d]				
Output ripple	-	-	1	mV rms
Transient settling time[e]	-	-	700	µs
Maximum load current	5	-	-	mA
Minimum load current	1	-	-	µA
Conversion efficiency (I_{load} = 1mA)	-	80	-	%
Switching frequency[f]	50	-	150	kHz

[a] For step changes in load of 30 to 80mA and 80 to 30mA

[b] Locked to crystal frequency

[c] The current is limited on start-up to prevent excessive stored energy in the filter inductor.

[d] The regulator is in low-power mode when the IC is in deep sleep mode, or in reset.

[e] 100µA to 1mA pulsed load

[f] Defines the minimum period between pulses. Pulses are skipped at low current loads.

Note:

The external inductor connected to the switch-mode regulator must have an ESR in the range 0.3Ω to 0.7Ω:

- Low ESR < 0.3Ω causes instability.
- High ESR > 0.7Ω derates the maximum current.

11.3.3 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.80	2.00	2.70	V
Output voltage (I_{load} = 70mA / VREGIN_L = 1.7V)	1.42	1.50	1.57	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 90mA), ΔV_{out}	-	-	5	mV
Load regulation (100µA < I_{load} < 115mA), ΔV_{out}	-	-	25	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	115	mA
Minimum load current	5	-	100	µA
Quiescent current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	5	8	15	µA

[a] The regulator output is connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 115mA pulsed load

[d] The regulator is in low-power mode when the IC is in deep sleep mode, or in reset

11.3.4 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage	4.5	-	6.5	V

Charging Mode (BAT_P rising to 4.2V)		Min	Typ	Max	Unit
Supply current[a]		-	4.5	6	mA
Battery trickle charge current[b] [c]		-	4	-	mA
Maximum battery fast charge current (I-CTRL = 15)[c] [d]	Headroom[e] > 0.7V	-	150	-	mA
	Headroom = 0.3V	-	120	-	mA
Minimum battery fast charge current (I-CTRL = 0)[c] [d]	Headroom > 0.7V	-	40	-	mA
	Headroom = 0.3V	-	35	-	mA
Fast charge step size (I-CTRL = 0 to 15)	Spread ±17%	-	6.3	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set), V_{FLOAT} [f]		4.17	4.2	4.23	V
Float voltage trim step size[f]		-	50	-	mV
Battery charge termination current, % of fast charge current		5	10	20	%

[a] Current into VDD_CHG; does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] BAT_P < Float voltage

[c] The charge current is set in 16 equally spaced steps

[d] Trickle charge threshold < BAT_P < Float voltage

[e] Where headroom = VDD_CHG - BAT_P

[f] The float voltage is adjusted in 15 steps. The trim setting is determined in production test and must be loaded into the battery charger by firmware during the boot-up sequence.

Standby Mode (BAT_P falling from 4.2V)	Min	Typ	Max	Unit
Supply current[a]	-	1.5	2	mA
Battery current	-	-5	-	µA
Battery recharge hysteresis[b]	100	-	200	mV

[a] Current into VDD_CHG; does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] Hysteresis of (V_{FLOAT} - BAT_P) for charging to restart

Shutdown Mode (VDD_CHG too low or disabled by firmware)		Min	Typ	Max	Unit
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.90	-	V
	VDD_CHG falling	-	3.70	-	V
VDD_CHG - BAT_P lockout threshold	VDD_CHG rising	-	0.22	-	V
	VDD_CHG falling	-	0.17	-	V
Supply current		-	1.5	2	mA
Battery current		-1	-	0	µA

11.3.5 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.25	1.30	V
VDD_CORE rising threshold	1.20	1.30	1.35	V
Hysteresis	0.05	0.10	0.15	V

11.3.6 Regulator Enable

Switching Threshold	Min	Typ	Max	Unit
VREGENABLE_H				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V
VREGENABLE_L				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V

11.3.7 Digital Terminals

Supply Voltage Levels		Min	Typ	Max	Unit
VDD_{PRE}	Pre-driver supply voltage	1.4	1.5	1.6	V
VDD I/O supply voltage (post-driver)	Full specification	3.0	3.3	3.6	V
	Reduced specification	1.7	-	3.0	V

Input Voltage Levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-0.3	-	0.25 x VDD	V
V_{IH} input logic level high	0.625 x VDD	-	VDD + 0.3	V
$V_{SCHMITT}$ Schmitt voltage	0.25 x VDD	-	0.625 x VDD	V

Output Voltage Levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 4.0mA	0	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD	-	VDD	V

Input and Tristate Currents	Min	Typ	Max	Unit
I_i input leakage current at V_{in} = VDD or 0V	-100	0	100	nA
I_{oz} tristate output leakage current at V_o = VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	µA
With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	-0.2	1.0	5.0	µA
C_I input capacitance	1.0	-	5.0	pF

Resistive Strength	Min	Typ	Max	Unit
R_{puw} weak pull-up strength at VDD - 0.2V	0.5	-	2	MΩ
R_{pdw} weak pull-down strength at 0.2V	0.5	-	2	MΩ
R_{pus} strong pull-up strength at VDD - 0.2V	10	-	50	kΩ
R_{pds} strong pull-down strength at 0.2V	10	-	50	kΩ

11.3.8 LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Off current		-	1	2	µA
On resistance	V_{PAD} < 0.5V	-	20	33	Ω
On resistance, pad enabled by battery charger	V_{PAD} < 0.5V	-	20	50	Ω

11.3.9 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range[a]		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[b]		-	-	700	Samples/s

[a] LSB size = VDD_ANA/1023

[b] The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

11.3.10 Mono Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	32	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% 150mV_{pk-pk} input	**F_{sample}**				
		8kHz	-	79	-	dB
		11.025kHz	-	77	-	dB
		16kHz	-	76	-	dB
		22.050kHz	-	76	-	dB
		32kHz	-	75	-	dB
Digital Gain	Digital Gain Resolution = 1/32		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-3	-3	42	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kΩ
THD+N (microphone input) @ 30mV rms input			-	0.04	-	%

11.3.11 Mono Codec: Digital to Analogue Converter

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	16	Bits
Output Sample Rate, F_{sample}	-		8	-	32	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.01% 0dBFS signal Load = 100kΩ	**F_{sample}**				
		8kHz	-	95	-	dB
		11.025kHz	-	95	-	dB
		16kHz	-	95	-	dB
		22.050kHz	-	95	-	dB
		32kHz	-	95	-	dB
Digital Gain	Digital Gain Resolution = 1/32		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full-scale swing (differential)			-	750	-	mV rms
Allowed Load		Resistive	16(8)	-	O.C.[a]	Ω
		Capacitive	-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
THD+N 16Ω load			-	-	0.1	%
SNR (Load = 16Ω, 0dBFS input relative to digital silence)			-	95	-	dB

[a] CSR recommends 100Ω as a practical maximum allowed load

11.3.12 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[a]	16	26	26	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω

[a] Integer multiple of 250kHz

[b] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[c] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

11.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 11.1 shows the ESD handling maximum ratings.

Condition	Note	Class	Max Rating
Human Body Model Contact Discharge per JEDEC EIA/JESD22-A114	ESD_HAND_HBM	2	2000V (all pins)
Machine Model Contact Discharge per JEDEC EIA/JESD22-A115	ESD_HAND_MM	B	200V (all pins)
Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	ESD_HAND_CDM	II	200V (all pins)

Table 11.1: ESD Handling Ratings

12 Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	SCO		HV3	30	9.8	mA
Slave	eSCO		EV3	30	11.3	mA
Slave	eSCO		2EV3	60	7.9	mA
Slave	eSCO		2EV3	30	11	mA
Slave	SCO	1-mic CVC	HV3	30	12.3	mA
Slave	eSCO	1-mic CVC	2EV3	60	10.4	mA
Slave	eSCO	1-mic CVC	2EV3	30	13.6	mA
Slave	ACL	Sniff = 100ms	-	-	0.59	mA
Slave	ACL	Sniff = 500ms	-	-	0.25	mA
Slave	ACL	Sniff = 1280ms	-	-	0.16	mA
Slave	SBC low quality, no sniff		-	-	11.4	mA
Slave	SBC low quality, sniff = 62.5ms		-	-	7.9	mA
Slave	SBC high quality, no sniff		-	-	13	mA
Slave	SBC high quality, sniff = 62.5ms		-	-	10	mA
Master	SCO		HV3	30	9.9	mA
Master	eSCO		EV3	30	10.2	mA
Master	eSCO		2EV3	60	7.5	mA
Master	eSCO		2EV3	30	9.7	mA
Master	SCO	1-mic CVC	HV3	30	12.5	mA
Master	eSCO	1-mic CVC	2EV3	60	10	mA
Master	eSCO	1-mic CVC	2EV3	30	12.2	mA
Master	ACL	Sniff = 100ms	-	-	0.71	mA

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Master	ACL	Sniff = 500ms	-	-	0.26	mA
Master	ACL	Sniff = 1280ms	-	-	0.16	mA
Master	SBC low quality, no sniff		-	-	10	mA
Master	SBC low quality, sniff = 62.5ms		-	-	8	mA
Master	SBC high quality, no sniff		-	-	12.8	mA
Master	SBC high quality, sniff = 62.5ms		-	-	10.1	mA

Note:

Current consumption values are taken with:

- BAT_P pin for switch-mode regulator = 3.7V
- RF TX power set to 0dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected, with internal microphone bias circuit set to minimum current level
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected

13 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction on Hazardous Substances directive guidelines in the EU RoHS Directive 2002/95/EC. This includes compliance with the requirements for Deca BDE, as per removal of exemption, implementation date 01-Jul-08

  EU REACH, Regulation (EC) No 1907/2006:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - Substances identified on candidate list as Substances of Very High Concern (SVHC), 38 substances as per update published 18 June 2010.
- EU Commission Decision 2009/251/EC
  - Products containing dimethylfumarate (DMF) are not placed or made available on the market.
- EU Packaging and Packaging Waste, Directive 94/62/EC
- Montreal Protocol on substances that deplete the ozone layer

Additionally, as shown in Table 13.1, CSR Green semiconductor products are free from bromine, chlorine or antimony trioxide and other hazardous chemicals.

Material	Maximum Allowable Amount
Cadmium (Cd)	100ppm
Lead (Pb)	1000ppm (solder), 100pm (plastic)
Mercury (Hg)	1000ppm
Hexavalent-Chromium (Cr VI)	1000ppm
Polybrominated biphenyls (PBB)	1000ppm
Polybrominated diphenyl ethers (PBDE) - including Decabromodiphenyl ether (Deca BDE)	1000ppm
Bromine, Chlorine	900ppm, <1500ppm combined
Antimony Trioxide (Sb_2O_3)	900ppm
Red phosphorous	1000ppm
Beryllium Oxide	Banned
Chlorinated paraffin (including short chain chlorinated paraffins – carbon chain length 10-13 and medium chain chlorinated paraffins – carbon chain length 14-17)	Banned
Polychlorinated napthalenes (PCN)	Banned
Polychlorinated terphenyls (PCT)	Banned
Polychlorinated biphenyls (PCB)	Banned

Material	Maximum Allowable Amount
Polyvinyl Chloride (PVC)	Banned
Formaldehyde	Banned in wooden products
Asbestos	Not intentionally introduced
Phthalates	Not intentionally introduced
Radioactive substances	Not intentionally introduced - reportable
Tributyl tin (TBT) / Triphenyl tin (TPT) / Tributyl Tin Oxide (TBTO)	Not intentionally introduced

Table 13.1: Chemical Limits for Green Semiconductor Products

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

CSR has defined this Green standard based on current regulatory and customer requirements. For more information contact product.compliance@csr.com.

14 Software

BC6145 QFN:

- Is supplied with on-chip Bluetooth v3.0 specification qualified HCI stack firmware
- Is supplied with on-chip BC6145 QFN DSP Mono Headset Solution, which includes 6th generation 1-mic CVC audio enhancements
- Can be shipped with CSR's BC6145 QFN DSP mono headset solution development kit for BC6145 QFN, order code DK-BC-6145-10037-1A

The BC6145 QFN software architecture enables Bluetooth processing and the application program to run on the internal RISC MCU, and the audio enhancements on the Kalimba DSP.

14.1 BC6145 QFN DSP Mono Headset Solution

The CSR mono headset ROM software supports:

- 6th generation 1-mic CVC audio enhancements
- CSR's *Hear and Be Heard* bidirectional noise reduction feature
- mSBC wideband speech codec
- A2DP v1.2
- HFP v1.5 and HSP v1.2
- Bluetooth v3.0 specification is supported in the ROM software
- Secure simple pairing
- Proximity pairing (headset-initiated pairing) for greatly simplifying the out-of-box pairing process, for more information see Section 14.1.7
- For connection to more than 1 mobile phone, advanced multipoint is supported. This enables a user to take calls from a work and personal phone or a work phone and a VoIP dongle for Skype users. This has minimal impact on power consumption and is easy to configure.
- Most of the CSR mono headset ROM software features are configured on the BC6145 QFN using the Headset Configurator tool available from www.csrsupport.com/MonoHeadsetSolutions. The tool reads and writes headset configurations directly to the EEPROM or alternatively to a PSR file. Configurable headset features include:
  - Bluetooth v3.0 specification features
  - Reconnection policies, e.g. reconnect on power-on
  - Audio features, including default volumes
  - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for last number redial
  - LED indications for states, e.g. headset connected, and events, e.g. power on
  - Indication tones for events and ringtones
  - HFP v1.5 supported features
  - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
  - Advanced Multipoint settings
- The BC6145 QFN DSP mono headset solution has undergone extensive interoperability testing to ensure it works with the majority of phones on the market

14.1.1 Hear and Be Heard

CSR's *Hear and Be Heard* is a bidirectional noise reduction feature that ensures increased speech clarity in preparation for improving intelligibility through spectral enhancement for the user and the person they are speaking to.

14.1.2 A2DP Streaming on a Mono Headset

BC6145 QFN enables an A2DP v1.2 stream connection to the headset while a call is not in progress. This enables high-quality mono music streaming where the left and right stereo streams are mixed.

14.1.3 Advanced Multipoint Support

Advanced Multipoint enables the connection of 2 devices to BC6145 QFN at the same time, examples include:

- 2 phones connected to a BC6145 QFN headset
- Phone and a VoIP dongle connected to a headset

The BC6145 QFN DSP mono headset solution:

- Supports a maximum of 2 connections (either HFP or HSP)
- Enables multiple-call handling from both devices at the same time
- Treats all headset buttons:
  - During a call from 1 device, as if there is 1 device connected
  - During multiple calls (1 on each device), as if there is a single AG with multiple calls in progress (three-way calling)

14.1.4 A2DP Multipoint Support

A2DP multipoint support enables the connection of 2 A2DP source devices to BC6145 QFN at the same time, examples include:

- 2 A2DP-capable phones connected to a BC6145 QFN headset
- A2DP-capable phone and an A2DP-only source device, e.g. a PC or an iPod touch

The BC6145 QFN DSP mono headset solution enables:

- Music streaming from either of the connected A2DP source devices where the music player is controlled on the source device
- Advanced HFP multipoint functions to interrupt music streaming for calls, and resumes music streaming on the completion of the calls

14.1.5 Programmable Audio Prompts

BC6145 QFN enables a user to configure and load pre-programmed audio prompts from:

- An external EEPROM, in this implementation the prompts are stored in the same EEPROM as the PS Keys, see Figure 14.1. A larger EEPROM is necessary for programmable audio prompts. This implementation supports EEPROMs up to 512Kb. An EEPROM of 512Kb enables approximately 15 seconds of audio storage.
- An external SPI flash, in this implementation the prompts are stored in SPI flash and the EEPROM is for PS Keys, see Figure 14.2.

The programmable audio prompts provide a mechanism for higher-quality audio indications to replace standard tone indications. A programmable audio prompt is assigned to any user event in place of a standard tone.

Programmable audio prompts contain either voice prompts to indicate that events have occurred or provide user-defined higher quality ring tones/indications, e.g. custom power on/off tones.

The Headset Configurator tool can generate the content for the programmable audio prompts from standard WAV audio files. The tool also enables the user to configure which prompts are assigned to which user events.

Section 7.3 describes the I²C interface to the external EEPROM and Section 7.4 describes the SPI flash interface.

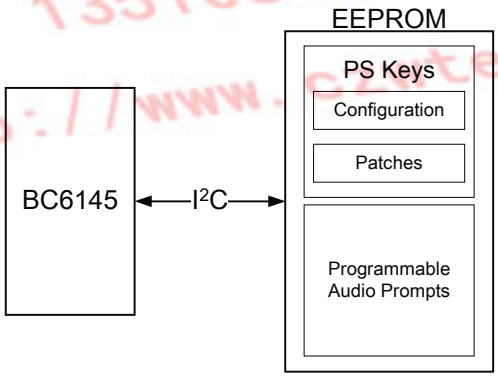


Figure 14.1: Programmable Audio Prompts in External I²C EEPROM

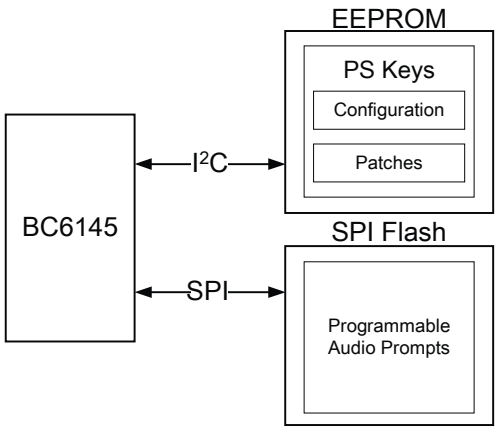


Figure 14.2: Programmable Audio Prompts in External SPI Flash with External I²C EEPROM for PS Keys

14.1.6 CSR's Intelligent Power Management

IPM extends the available talk time of a BC6145 QFN-based headset, by automatically reducing the audio processing performed by CVC at a series of low battery capacity thresholds.

The Headset Configurator tool configures the following IPM features:

- IPM enable/disable
- The battery capacity that engages IPM

A user-action to enable or disable the IPM is also configurable.

If engaged, CVC processing reduces automatically on reaching the preset battery capacity. Once the audio is terminated, the DSP shuts down to achieve maximum power savings before the next call.

IPM resets when recharging the headset. The talk time extension depends on:

- The battery size
- The battery condition
- The threshold capacity configured for the IPM to engage

14.1.7 Proximity Pairing

Proximity pairing is headset-initiated pairing and it simplifies the out-of-box pairing process. Proximity pairing enables the headset to find the closest discoverable phone. The headset then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus to pair with the new headset.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the headset pairing is with a PIN code
- For a Bluetooth v2.1 (or above) phone the headset pairing is without a PIN code

Proximity pairing is based on finding and pairing with the closest phone. To do this, the headset finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and it is defined as the closest device. The headset then attempts to pair with and connect to this device.

Proximity pairing is configurable using the Headset Configurator tool available from www.csrsupport.com/MonoHeadsetSolutions.

14.1.8 Proximity Connection

Proximity connection is an extension to proximity pairing, see Section 14.1.7. It enables the headset-user to take advantage of the proximity of devices each time the headset powers up and not just during a first time pairing event.

Proximity connection enables a user with multiple handsets to easily connect to the closest discoverable phone by comparing the proximity of devices to the headset at power-on to the list of previously paired devices.

Proximity connection speeds up the headset connection process. It requires the headset to initiate a SLC connection to the nearest device first and combines this with the headset's storage of the last 8 paired/connected devices. Using proximity connection means functions like *power on into an incoming call* operate equally well for the most recently paired or connected device, as well as the least recently paired or connected device.

14.2 6th Generation 1-mic CVC Audio Enhancements

1-mic CVC full-duplex voice processing software is a fully integrated and highly optimised set of DSP algorithms developed to ensure easy design and build of echo and noise-cancelling headset products.

CVC enables greater acoustic design flexibility by incorporating software to compensate for cost-optimised microphone-to-speaker coupling and placement. CVC-enabled headsets operate in a wide variety of acoustic environments. Sophisticated noise suppression technology reduces the impact of noise in the transmission channel. Using intelligent volume control and intelligibility improvements, the receive channel is also enhanced based on the acoustic noise in the listener's environment.

The 6th generation CVC provides 3 new major features:

- A high performance Wind Noise Reduction module provides significant reduction of both front and side wind noise. This uses a very low-power algorithm which automatically cuts in only on the detection of wind noise.
- A 16kHz sample rate for full compliance across the suite of DSP algorithms
- Frequency enhanced speech intelligibility

1-mic CVC includes a tuning tool enabling the developer to easily adapt CVC with different audio configurations and tuning parameters. The tool provides real-time system statistics with immediate feedback enabling designers to quickly investigate the effect of changes.

Figure 14.3 shows the functional block diagram of CSR's proprietary 1-mic CVC DSP solution for a single-microphone headset product.

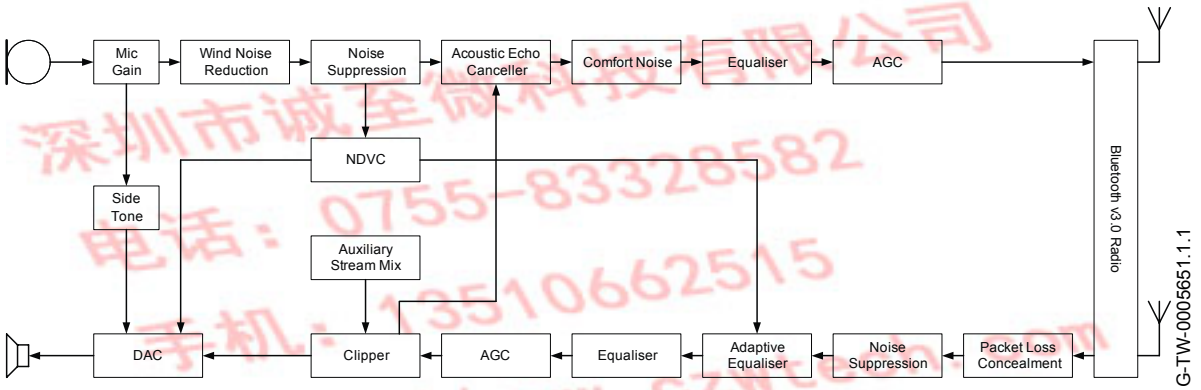


Figure 14.3: 1-mic CVC Block Diagram

Section 14.2.1 to Section 14.2.12 describe the audio processing functions provided within CVC.

14.2.1 Noise Suppression

The noise suppression block is implemented in both signal paths. It is completely independent and is individually tuned. Noise suppression is a sub-band stationary / quasi-stationary noise suppression algorithm that uses the temporal characteristics of speech and noise to remove the noise from the composite signal while maximising speech quality. The current implementation has the capability to improve the SNR by > 20dB.

14.2.2 Wind Noise Reduction

The wind noise algorithm achieves excellent wind noise reduction with very low power overhead, which has a negligible impact on battery life. The wind noise capability operates in the noise suppression block in the transmit path and dynamically detects and engages when wind noise is present. SNR improvements depend on wind direction, speech and microphone placement. Improvements of up to 32dB are achievable using the DSP module.

CVC wind noise performance is further improved by suitable mechanical baffling of the microphone which is optimised during the tuning process.

14.2.3 Acoustic Echo Cancellation

The AEC includes:

- A referenced sub-band adaptive linear filter that models the acoustic path from the receive reference point to the microphone input
- A non-linear processing function that applies narrowband and wideband attenuation adaptively as a result of residual echo present after the linear filter

14.2.4 Comfort Noise Generator

The CNG:

- Creates a spectrally and temporally consistent noise floor for the far-end listener
- Adaptively inserts noise modelled from the noise present at the microphone into gaps introduced when attenuation is applied by the non-linear processing of the AEC

14.2.5 Equalisation

The equalisation filters:

- Have independent equalisation modules provided in the send and receive signal paths:
  - Each module comprises of 5 bands of equalisation using cascaded 2nd order IIR filters
- Are fully configurable using a graphical tuning tool
- Provide static compensation for the frequency response of transducers in the system

14.2.6 Automatic Gain Control

The AGC block attempts to:

- Normalise the amplitude of the incoming audio signal to a desired range to increase perceived loudness
- Reduce distortion due to clipping
- Reduce amplitude variance observed from different users, phones, and networks

Maintaining a consistent long-term loudness for the speech ensures it is more easily heard by the listener and it also provides the subsequent processing block a larger amplitude signal to process. The behaviour of the AGC differs from a dynamic range audio compressor. The convergence time for the AGC is much slower to reduce the non-linear distortion.

14.2.7 Packet Loss Concealment

Bit errors and packet loss can occur in the Bluetooth transmission due to a variety of reasons, e.g. Wi-Fi interference or RF signal degradation due to distance or physical objects. As a result of these errors, the user hears glitches referred to as *pops* and *clicks* in the audio stream. The PLC block improves the receive path audio quality in the presence of bit and packet errors within the Bluetooth link by using a variety of techniques such as pitch-based waveform substitution.

The PLC significantly improves dealing with bit errors, using the BFI output from the firmware. The DSP calculates an average BER and selectively applies the PLC to the incoming data. This optimises audio quality for a variety of bit errors and packet loss conditions. The PLC is enabled in all modes.

14.2.8 Adaptive Equalisation

The adaptive equalisation block improves the intelligibility of the receive path voice signal in the presence of near-end noise by altering the spectral shape of the receive path signal while maintaining the overall power level. The adaptive equaliser can also compensate for variations in voice transmission channels.

14.2.9 Auxiliary Stream Mix

The auxiliary stream mixer enables the system to seamlessly mix audio signals such as tones, beeps and voice prompts with the incoming SCO stream. This avoids any interruption to the SCO stream and as a result prevents any speech from being lost.

14.2.10 Clipper

The clipper block intentionally limits the amplitude of the receive signal prior to the reference input of the AEC to more accurately model the behaviour of the post reference input blocks such as the DAC, power amplifier, and the loudspeaker. This processing block can significantly improve the echo performance in cost-optimised loudspeakers.

14.2.11 Noise Dependent Volume Control

The NDVC block improves the intelligibility of the receive path signal by increasing the analogue DAC gain value based on the send noise estimate from the send path noise suppression block. As the send noise estimate increases, the NDVC algorithm increases the analogue DAC gain value. The NDVC uses hysteresis to minimise the artefacts generated by rapidly adjusting the DAC gain due to the fluctuation in the environmental noise.

14.2.12 Fixed Gains

There are fixed gain controls at all inputs and outputs to the system so that levels are set according to hardware constraints and industry standards.

14.2.13 Frequency Enhanced Speech Intelligibility

Frequency enhanced speech intelligibility on the BC6145 QFN works with the adaptive equalisation module, see Section 14.2.8, and the NDVC module, see Section 14.2.11, to enhance intelligibility in the presence of noise. This combination of functions creates higher frequency information, which in the presence of noise, makes it much easier for the listener to differentiate between consonant pairs, therefore improving intelligibility. This also reduces listener fatigue as it requires less concentration effort from the user. This can lead to improved dual-tasking performance.

14.3 BC6145 QFN DSP Mono Headset Solution Development Kit

The development kit includes an evaluation board, music and voice dongle, and necessary interface adapters and cables. In conjunction with other supporting utilities, the development kit provides support for the evaluation and development of a BC6145 QFN mono headset solution.

15 Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
BC6145 QFN DSP Mono Headset Solution	QFN 48-lead (Green)	7 x 7 x 0.9mm, 0.5mm pitch	Tape and reel	BC6145A04-IQQB-R

Note:

BC6145 QFN is a ROM-based device where the product code has the form BC6145Axx. Axx is the specific ROM-variant, A04 is the ROM-variant for BC6145 QFN DSP Mono Headset Solution.

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts.

15.1 Development Kit Ordering Information

Description	Order Number
BC6145 QFN DSP Mono Headset Solution Development Kit	DK-BC-6145-10037-1A

16 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

16.1 Tape Orientation

Figure 16.1 shows the BC6145 QFN packing tape orientation.

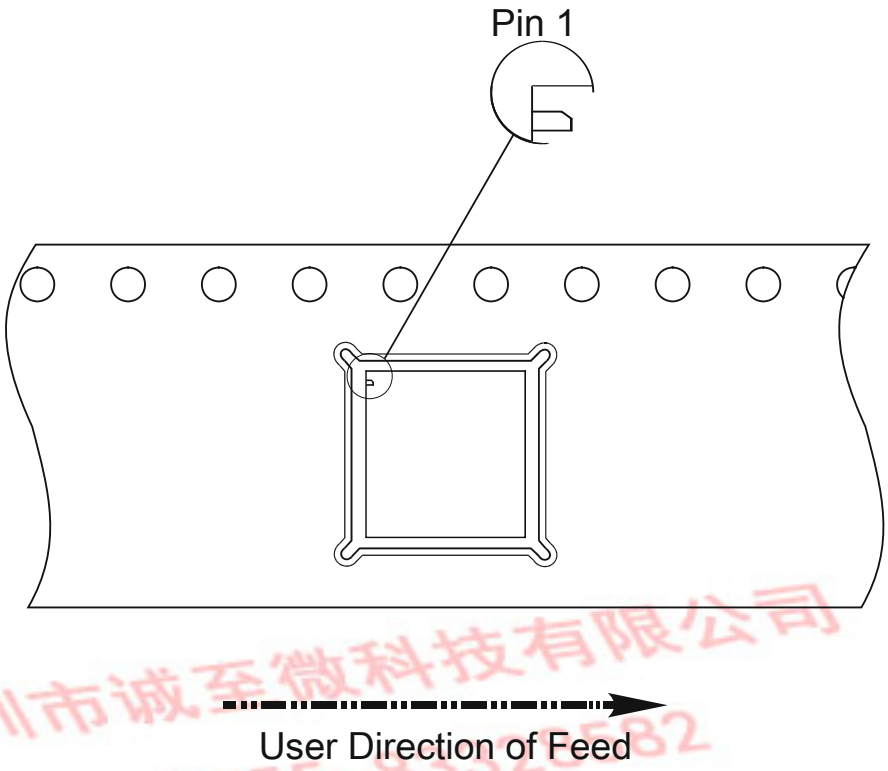


Figure 16.1: Tape Orientation

G-TW-0002812.2.2

16.2 Tape Dimensions

Figure 16.2 shows the dimensions of the tape for the BC6145 QFN.

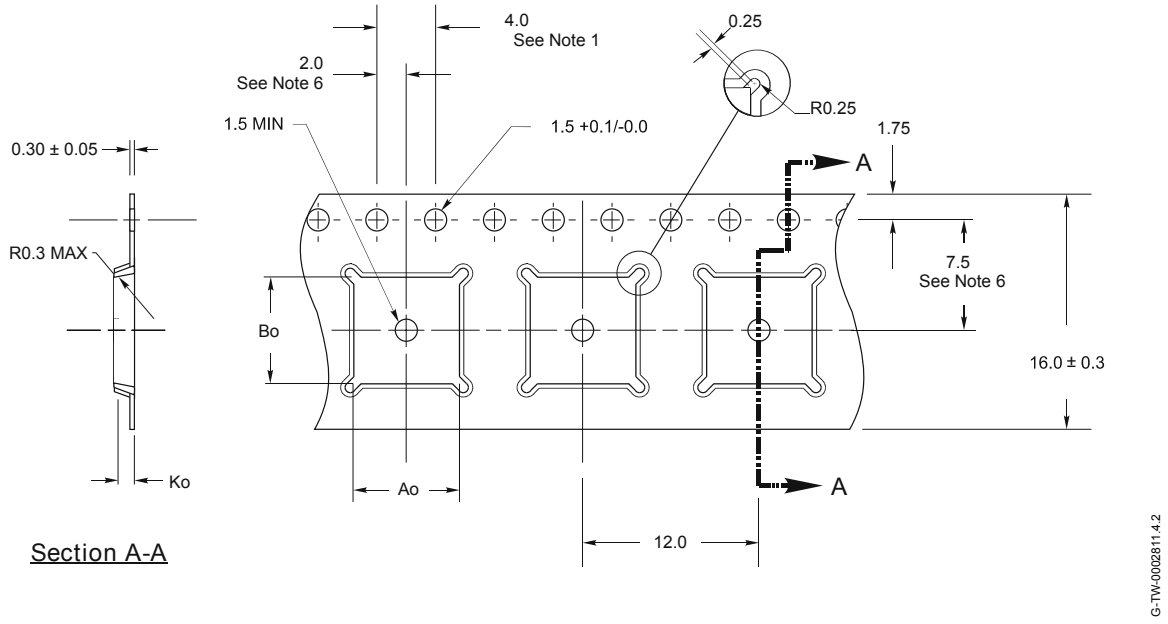


Figure 16.2: Tape Dimensions

A_0	B_0	K_0	Unit	Notes
7.25	7.25	1.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Camber not to exceed 1mm in 100mm 3. Material: PS + C 4. A_0 and B_0 measured as indicated 5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier 6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

16.3 Reel Information

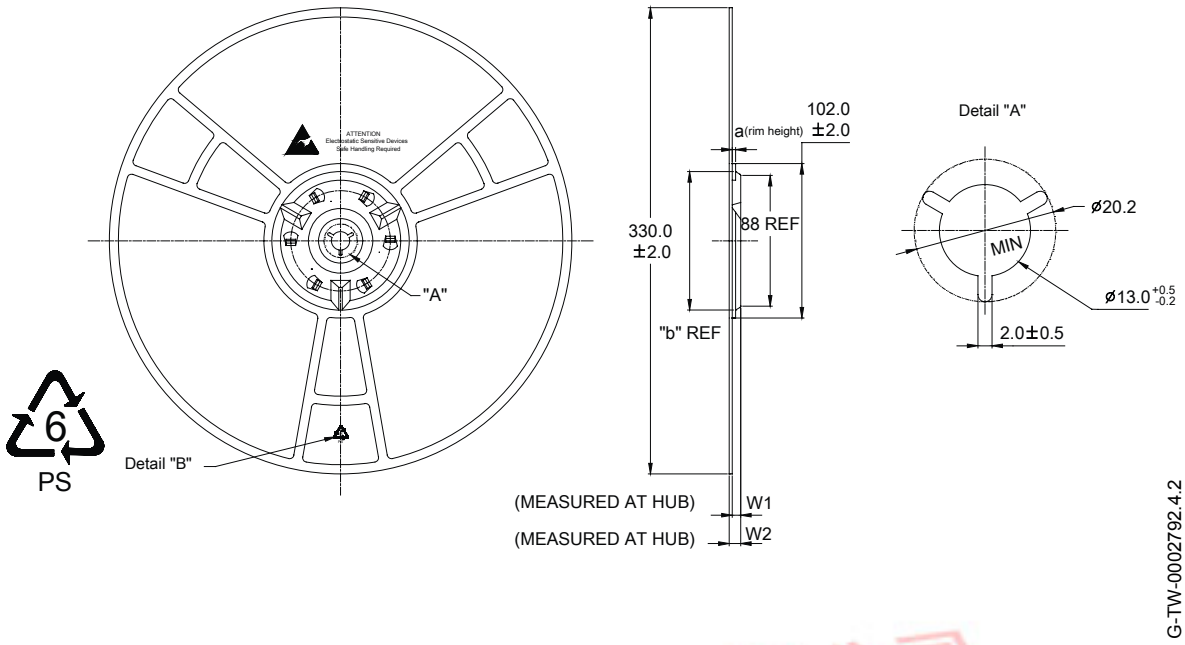


Figure 16.3: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
7 x 7 x 0.9mm QFN	16	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

16.4 Moisture Sensitivity Level

BC6145 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

17 Document References

Document	Reference, Date
BC6145 QFN Performance Specification	CS-204120-SP
BCSW-CVC-HS-4-5-x Product Data Sheet	CS-128313-DS
BlueCore5 Charger Description and Calibration Procedure Application Note	CS-113282-AN
Bluetooth Specification Version 3.0 + HS	Version 3.0 + HS [Vol 0 to Vol 5], 21 April 2009
Enhancing Microphone Bias Performance in Headset Designs using BlueVox2 Application Note	CS-121678-AN
Environmental Compliance Statement for CSR Green Semiconductor Products	CB-001036-ST
IC Packing and Labelling Specification	CS-112584-SP
Selection of I²C EEPROMS for Use with BlueCore	CS-101518-AN
Typical Solder Reflow Profile for Lead-free Device	CS-116434-AN

Terms and Definitions

Term	Definition
μ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
A2DP	Advanced Audio Distribution Profile
AC	Alternating Current
ACL	Asynchronous Connection-oriented
ADC	Analogue to Digital Converter
AEC	Acoustic Echo Cancellation
AFH	Adaptive Frequency Hopping
AG	Audio Gateway
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ALU	Arithmetic logic unit
B/W	BandWidth
BER	Bit Error Rate
BFI	Bad Frame Indicator
BIST	Built-In Self-Test
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CNG	Comfort Noise Generation
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CVC	Clear Voice Capture
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
DNL	Differential Non Linearity (ADC accuracy parameter)
DSP	Digital Signal Processor
DUT	Device Under Test
e.g.	*exempli gratia*, for example
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
EIA	Electronic Industries Alliance
eSCO	Extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FEC	Forward Error Correction
FET	Field Effect Transistor
FSK	Frequency Shift Keying
HCI	Host Controller Interface
HEC	Header Error Check Correction

Term	Definition
HFP	Hands-Free Profile
HSP	HeadSet Profile
I²C	Inter-Integrated Circuit Interface
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response (filter)
INL	Integral Non Linearity (ADC accuracy parameter)
IPC	See www.ipc.org
IPM	Intelligent Power Management
IQ	In-Phase and Quadrature
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression, and file compression / decompression
Kb	Kilobit
LC	An inductor (L) and capacitor (C) network
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
LSB	Least-Significant Bit (or Byte)
MAC	Medium Access Control
MAC	Multiplier and ACcumulator
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MISO	Master In Slave Out
MMU	Memory Management Unit
mSBC	modified Sub-Band Coding
NDVC	Noise Dependent Volume Control
NSMD	Non Solder Mask Defined
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Pull-down
PIN	Personal Identification Number
PIO	Programmable Input/Output, also known as general purpose I/O
PLC	Packet Loss Concealment
plc	Public Limited Company
ppm	parts per million
PS Key	Persistent Store Key
PSRR	Power Supply Rejection Ratio
PU	Pull-up
QFN	Quad-Flat No-lead
RAM	Random Access Memory

Term	Definition
RC	Resistor Capacitor
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented
SIG	(Bluetooth) Special Interest Group
SLC	Service Level Connection
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
THD+N	Total Harmonic Distortion and Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
VoIP	Voice over Internet Protocol
Wi-Fi®	Wireless Fidelity (IEEE 802.11 wireless networking)
XTAL	Crystal