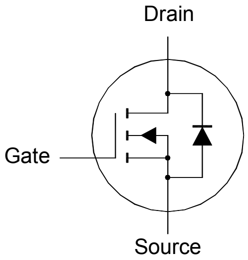
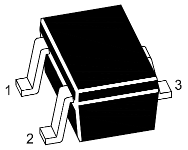
MMBT7002E

N-Channel Enhancement Mode Field Effect Transistor





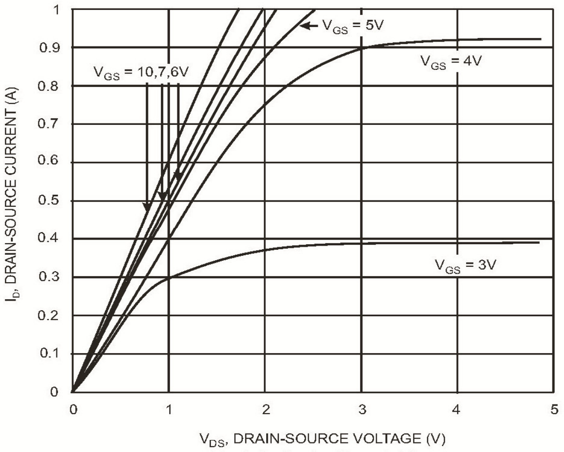
1. Gate 2. Source 3. Drain
SOT-523 Plastic Package

Absolute Maximum Ratings (T_a = 25 °C)

Parameter		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	60	V
Drain Gate Voltage ($R_{GS} \leq 1$ MΩ)		V_{DGR}	60	V
Gate Source Voltage	Continuous Pulsed	V_{GSS}	± 20 ± 40	V
Drain Current	Continuous Pulsed	I_D	115 800	mA
Total Power Dissipation		P_{tot}	150	mW
Thermal Resistance, Junction to Ambient		$R_{\theta JA}$	833	°C/W
Storage Temperature Range		T_j, T_{Stg}	- 55 to + 150	°C

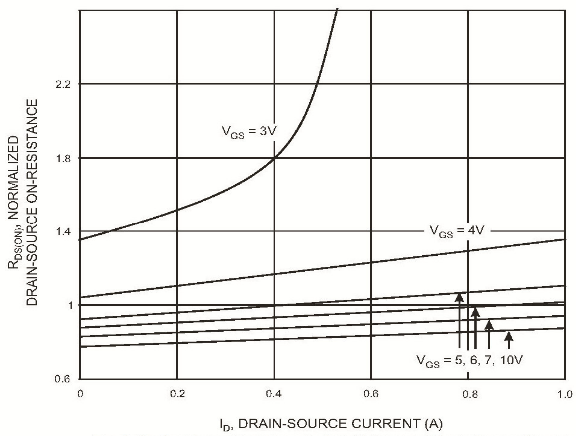
Characteristics at T_a = 25 °C

Parameter	Symbol	Min.	Max.	Unit
Drain Source Breakdown Voltage at I_D = 10 µA	BV_{DSS}	60	-	V
Zero Gate Voltage Drain Current at V_{DS} = 60 V	I_{DSS}	-	1	µA
Gate Source Leakage Current at ± V_{GS} = 20 V	$\pm I_{GSS}$	-	10	nA
Gate Source Threshold Voltage at V_{DS} = V_{GS} = 10 V, I_D = 250 µA	$V_{GS(th)}$	1	2	V
Static Drain Source On Resistance at V_{GS} = 5 V, I_D = 50 mA at V_{GS} = 10 V, I_D = 500 mA	$R_{DS(ON)}$	- -	7.5 13.5	Ω
Drain Source On Voltage at V_{GS} = 5 V, I_D = 50 mA at V_{GS} = 10 V, I_D = 500 mA	$V_{DS(ON)}$	- -	1.5 3.75	V
On-State Drain Current at V_{GS} = 10 V, V_{DS} = 7.5 V	$I_{D(ON)}$	0.5	-	A
Forward Transconductance at V_{DS} = 10 V, I_D = 200 mA	g_{FS}	80	-	mS
Input Capacitance at V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	50	pF
Output Capacitance at V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	25	pF
Reverse Transfer Capacitance at V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	5	pF
Turn On Time at V_{DD} = 30V, R_L = 150Ω, I_D = 0.2A, V_{GS} = 10V, R_{GEN} = 25Ω	t_{on}	-	20	ns
Turn Off Time at V_{DD} = 30V, R_L = 150Ω, I_D = 0.2A, V_{GS} = 10V, R_{GEN} = 25Ω	t_{off}	-	20	ns



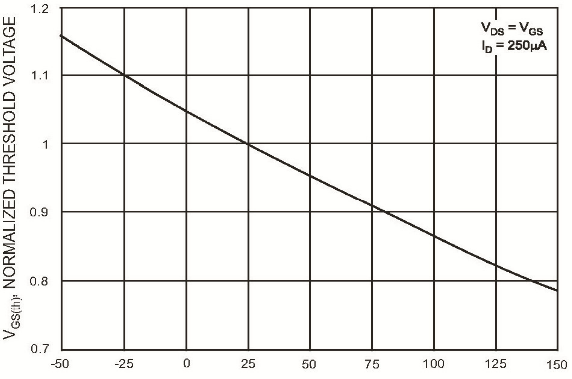
V_{DS}, DRAIN-SOURCE VOLTAGE (V)

Fig. 1 On-Region Characteristics



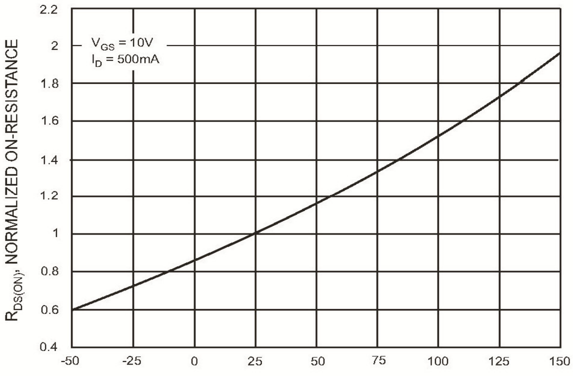
I_D, DRAIN-SOURCE CURRENT (A)

Fig. 2 On-Resistance Variation with Gate Voltage and Drain-Source Current



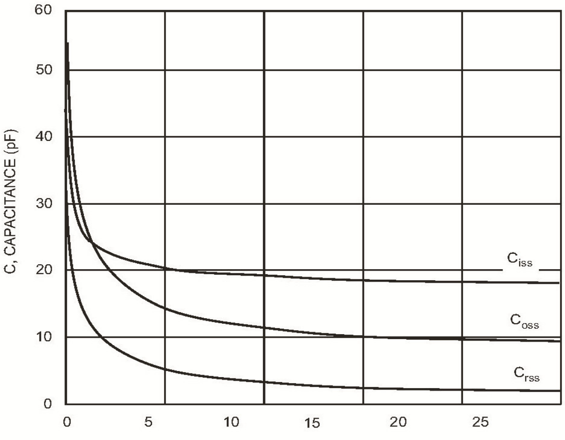
T_J, JUNCTION TEMPERATURE (°C)

Fig. 3 Gate Threshold Variation with Temperature



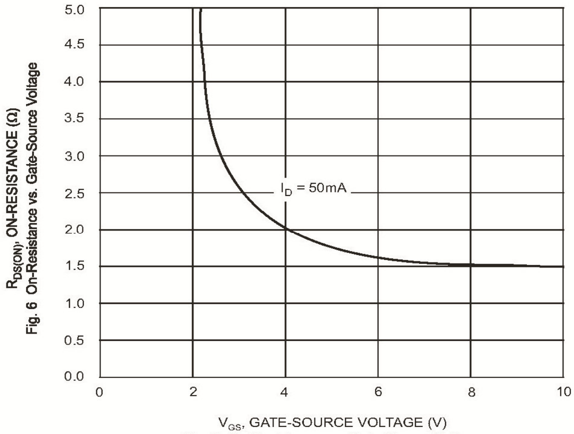
T_J, JUNCTION TEMPERATURE (°C)

Fig. 4 On-Resistance Variation with Temperature



V_{DS}, DRAIN-SOURCE VOLTAGE (V)

Fig. 5 Typical Capacitance



V_{GS}, GATE-SOURCE VOLTAGE (V)

Fig. 6 On-Resistance vs. Gate-Source Voltage