FAIRCHILD

SEMICONDUCTOR™

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CD4099BC
8-Bit Addressable Latch

General Description

The CD4099BC is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D), and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is LOW. Data entry is inhibited when enable ($\overline{E}$) is HIGH.

When clear (CL) and enable ($\overline{E}$) are HIGH, all outputs are LOW. When clear (CL) is HIGH and enable ($\overline{E}$) is LOW, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held LOW. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL: fan out of 2 driving 74L
     compatibility: or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Ordering Code:

| Order Number	Package Number	Package Description
CD4099BCN	N16E	16-Lead Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

Pin Assignments for DIP

Q7	1	16	V_{DD}
C_L	2	15	Q6
D	3	14	Q5
$\overline{E}$	4	13	Q4
A0	5	12	Q3
A1	6	11	Q2
A2	7	10	Q1
V_{SS}	8	9	Q0
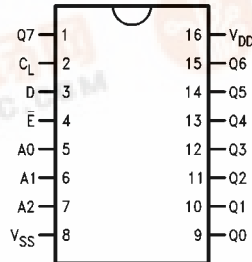
Top View

Truth Table

Mode Selection				
$\overline{E}$	CL	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

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CD4099BC 8-Bit Addressable Latch

Logic Diagram
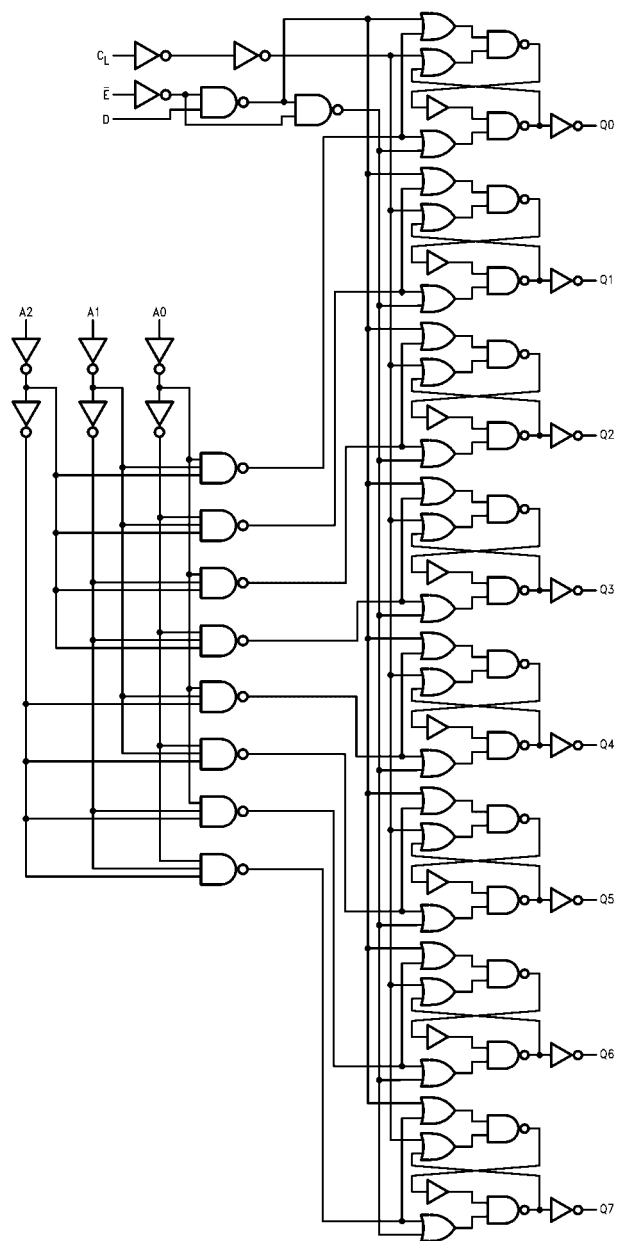
Absolute Maximum Ratings(Note 1)

(Note 2)

DC Supply Voltage (V_DD)	−0.5 to +18 V_DC
Input Voltage (V_IN)	−0.5 to V_DD +0.5 V_DC
Storage Temperature	
Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_DD)	3.0 to 15 V_DC
Input Voltage (V_IN)	0 to V_DD V_DC
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_SS = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Units
I_DD	Quiescent Device	V_DD = 5V, V_IN = V_DD or V_SS		20		0.02	20		150	µA
	Current	V_DD = 10V, V_IN = V_DD or V_SS		40		0.02	40		300	µA
		V_DD = 15V, V_IN = V_DD or V_SS		80		0.02	80		600	µA
V_OL	LOW Level	|I_O| ≤ 1µA								
	Output Voltage	V_DD = 5V		0.05		0	0.05		0.05	V
		V_DD = 10V		0.05		0	0.05		0.05	V
		V_DD = 15V		0.05		0	0.05		0.05	V
V_OH	HIGH Level	|I_O| ≤ 1 µA								
	Output Voltage	V_DD = 5V	4.95		4.95	5		4.95		V
		V_DD = 10V	9.95		9.95	10		9.95		V
		V_DD = 15V	14.95		14.95	15		14.95		V
V_IL	LOW Level	V_DD = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	Input Voltage	V_DD = 10V, V_O = 1.0V or 9.0V		3.0		4.5	3.0		3.0	V
		V_DD = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_IH	HIGH Level	V_DD = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	Input Voltage	V_DD = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_DD = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_OL	LOW Level Output	V_DD = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	Current (Note 3)	V_DD = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_DD = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_OH	HIGH Level Output	V_DD = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	Current (Note 3)	V_DD = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_DD = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_IN	Input Current	V_DD = 15V, V_IN = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_DD = 15V, V_IN = 15V		0.30		10^{-5}	0.30		1.0	µA

Note 3: I_OH and I_OL are tested one output at a time.

CD4099BC

AC Electrical Characteristics (Note 4)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, Input $t_r = t_f = 20$ ns, unless otherwise noted

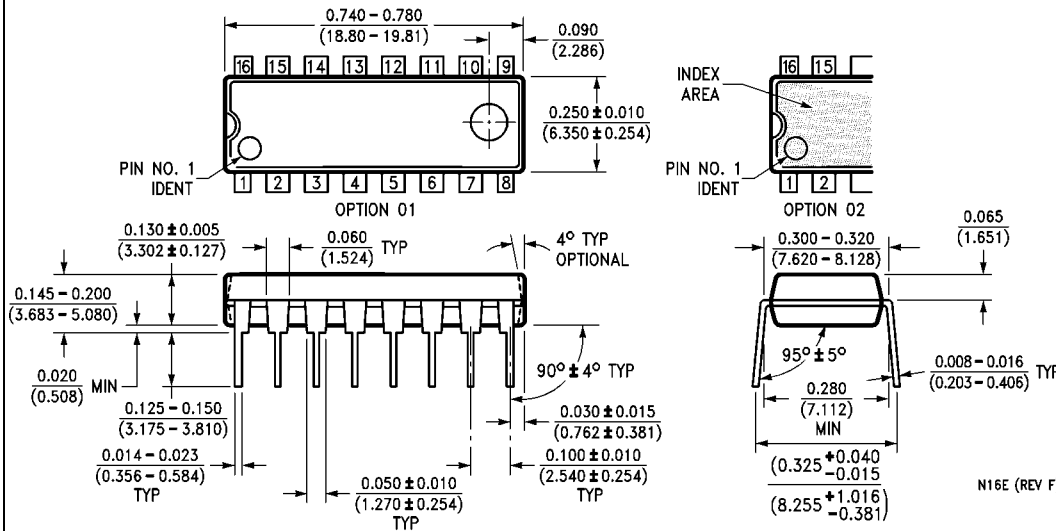| Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		75	150	ns
		$V_{DD} = 15V$		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	$V_{DD} = 5V$		175	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	ns
t_{TLH}, t_{THL}	Propagation Delay Address to Output	$V_{DD} = 5V$		225	450	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
T_{WH}, T_{WL}	Minimum Data Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		65	125	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		40	75	ns
		$V_{DD} = 15V$		25	50	ns
t_{SU}	Minimum Set-Up Time Data to E	$V_{DD} = 5V$		40	80	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_H	Minimum Hold Time Data to E	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{SU}	Minimum Set-Up Time Address to E	$V_{DD} = 5V$		−15	50	ns
		$V_{DD} = 10V$		0	30	ns
		$V_{DD} = 15V$		0	20	ns
t_H	Minimum Hold Time Address to E	$V_{DD} = 5V$		−50	15	ns
		$V_{DD} = 10V$		−20	10	ns
		$V_{DD} = 15V$		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 5)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

Note 5: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

Switching Time Waveforms

CD4099BC 8-Bit Addressable Latch
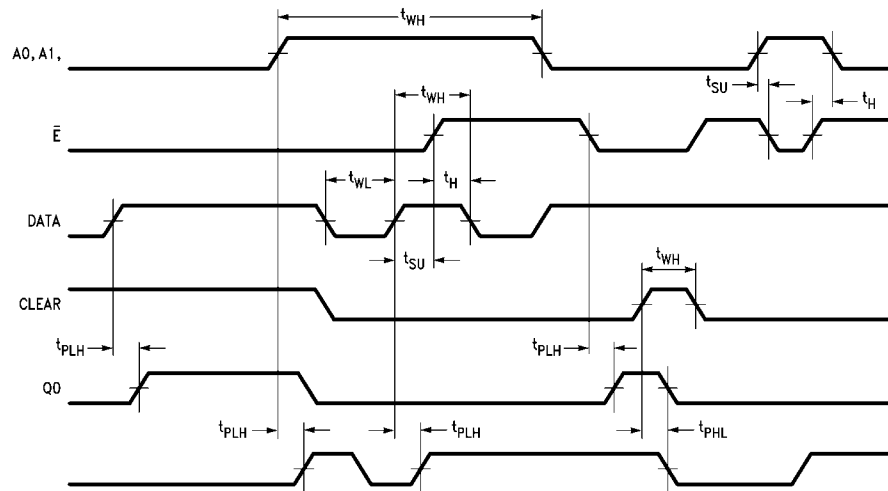
Physical Dimensions inches (millimeters) unless otherwise noted

0.740 − 0.780
(18.80 − 19.81)

0.090
(2.286)

INDEX
AREA

16 15 14 13 12 11 10 9

16 15

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

PIN NO. 1
IDENT

1 2

OPTION 01

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.300 − 0.320
(7.620 − 8.128)

0.145 − 0.200
(3.683 − 5.080)

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.020
(0.508) MIN

90° ± 4° TYP

0.280
(7.112)
MIN

0.125 − 0.150
(3.175 − 3.810)

0.030 ± 0.015
(0.762 ± 0.381)

0.014 − 0.023
(0.356 − 0.584)
TYP

0.050 ± 0.010
(1.270 ± 0.254)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

$(0.325 \begin{smallmatrix} +0.040 \\ -0.015 \end{smallmatrix})$

$(8.255 \begin{smallmatrix} +1.016 \\ -0.381 \end{smallmatrix})$

N16E (REV F

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E